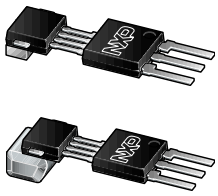


KMI25/2; KMI25/4

High performance rotational speed sensor

Rev. 1 — 29 April 2016 Product data sheet

1. Product profile

1.1 General description

Based on the Anisotropic MagnetoResistive (AMR) effect, the KMI25/2 and the KMI25/4 detect the rotational speed of target wheels. The KMI25/2 is used with active target wheels (multipole encoders) and the KMI25/4 is used with passive target wheels (ferromagnetic gear wheels). This design delivers secure speed information over a wide range of speed, air gap and temperature. It delivers the speed information via a current protocol at the supply pins.

CAUTION

Do not press two or more products together against their magnetic forces and do not let them collide with each other.

1.2 Features and benefits

- System in package
- Two wire current interface
- Rotational direction detection
- Digital output protocol [ArbeitsKreis protocol (AK protocol)]
- Large range of air gap
- Large range of operating terminal voltage
- Wide temperature range
- High ElectroStatic Discharge (ESD) protection
- Very low jitter
- Automotive qualified in accordance with AEC-Q100 Rev-G (grade 0)

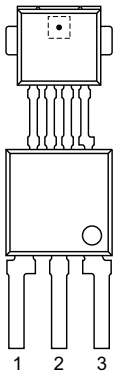
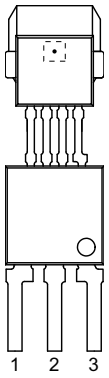
1.3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	normal operation mode; $T_{amb} \leq 170$ °C; referred to pin GND	6.8	-	16	V
T_{amb}	ambient temperature	normal operation mode	–40	-	+150	°C
I_{CCL}	LOW-level supply current		5.88	7.0	8.4	mA
I_{CCM}	MID-level supply current		11.7	14.0	16.8	mA
I_{CCH}	HIGH-level supply current		23.5	28.0	33.6	mA
f_H	magnetic field strength frequency		0	-	2.5	kHz
H_M	peak magnetic field strength	after power-on; speed pulses latest after $N_{cy(H)}$ magnetic cycles; see characteristics in Table 10				
		KMI25/2	150	-	-	A/m
		KMI25/4	190	-	-	A/m

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	
			KMI25/2	KMI25/4
1	V_{CC}	supply pin		
2	DI	digital input pin		
3	GND	ground pin		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
KMI25/2	SIP3	plastic single-ended multi-chip package; magnetized ferrite magnet (3.8 × 2 × 0.8 mm); 4 interconnections; 3 in-line leads	SOT477A
KMI25/4	SIP3	plastic single-ended multi-chip package; magnetized ferrite magnet (5.2 × 4.25 × 2.95 mm); 4 interconnections; 3 in-line leads	SOT477E

4. Functional diagram

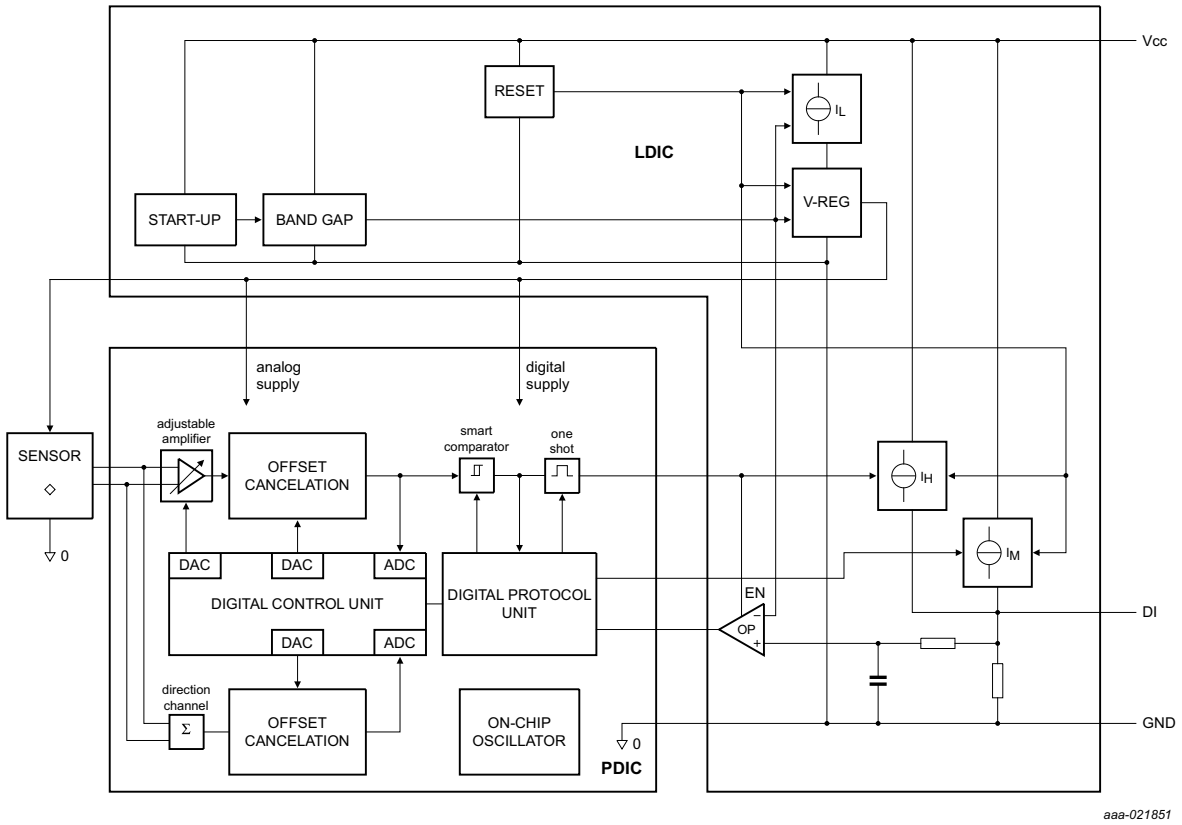


Fig 1. Functional diagram

5. Functional description

The KMI25/2 and the KMI25/4 are high performance AMR speed sensors, which are dedicated to ABS applications. The difference between both product versions is the stimulating element in the application, which is a magnetized multipole encoder (KMI25/2) or a ferromagnetic gear wheel (KMI25/4).

5.1 System architecture

The functional principles of KMI25/2 and KMI25/4 are shown in Figure 2 and Figure 3, respectively. For the KMI25/2, the magnetic poles lead to different magnetic stimuli at the AMR bridge. For the KMI25/4, flux bending at the gear wheel teeth generates different magnetic stimuli at the AMR bridge. In both cases, the electrical output voltage of the AMR bridge depends on the position of the sensor relative to the encoder. As a consequence, a rotating encoder generates a periodic output signal at the AMR bridge. The KMI25/2 and the KMI25/4 are sensitive to movement in the y direction in front of the sensor only. For definition of the coordinate axes, see Figure 4.

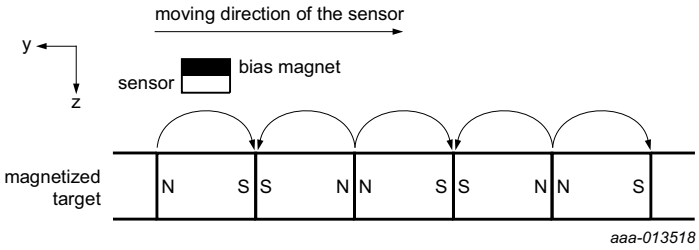


Fig 2. Functional principle of KMI25/2

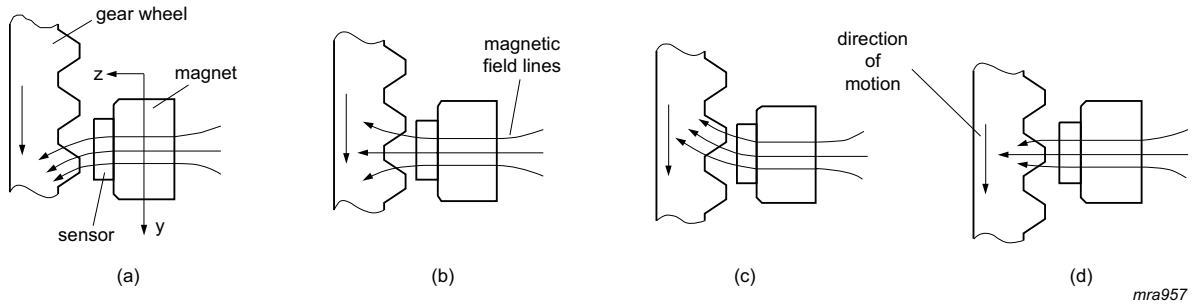
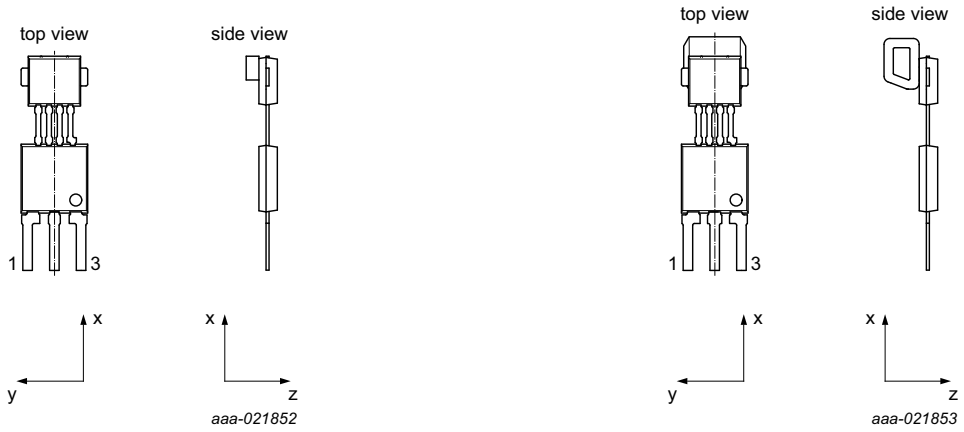


Fig 3. Functional principle of KMI25/4



a. KMI25/2 b. KMI25/4

Fig 4. Definition of coordinate system

The KMI25/2 and the KMI25/4 each comprise an AMR sensor chip, a Position Detector IC (PDIC) and a Line Driver IC (LDIC). The PDIC comprises the signal conditioning circuits, whereas the LDIC comprises the external interface and the supply for PDIC and AMR bridge (see Figure 1). The AMR sensor chip carries four MR elements arranged as a Wheatstone bridge. The AMR bridge converts the magnetic field, generated by the encoder rotation, into an electrical output signal. This signal is nearly sinusoidally with time.

The LDIC chip is fabricated using a robust high-voltage process. This measure shields the other two dies from the harsh electrical environment on the supply line V_{CC}. The constant current source I_L provides the LOW-level output signal of typically 7 mA and delivers the supply current for the whole sensor system. Thus from I_L the supply voltages for the PDIC, the AMR bridge and the current source blocks I_M and I_H are derived. The switchable current source I_M also delivers typically 7 mA. Hence, if I_M is active, the total supply current is at its MID level of typically 14 mA. This current refers to a logic HIGH level at the AK protocol. The switchable current source I_H delivers typically 21 mA. Thus, I_H being active results in a total current of typically 28 mA, which is the level of a speed pulse. With this current interface, safe sensor signal transport to the Electronic Control Unit (ECU) using only a two-wire cable is provided. In addition, the digital input pin DI converts an external resistance into a one-bit signal. This signal is passed on to the PDIC via a level shifter.

Within the PDIC, the differential output voltage of the AMR sensor bridge leads as speed signal into an analog signal chain. It comprises an amplifier with adjustable gain, followed by an offset cancelation stage and finally, a smart comparator having adjustable hysteresis levels. The latter converts the sinusoidal sensor signal into a rectangular output signal. Via a one-shot, the rectangular signal controls the switchable current source I_H on the LDIC. The sensor system outputs HIGH-level speed pulses at each zero-crossing of the magnetic input signal. As a result, the speed pulses occur at a repetition rate of twice the magnetic field strength frequency. This repetition rate allows measuring the rotational speed of the encoder wheel.

A peak detector within the digital control unit on the PDIC measures the amplitude and the offset of the sensor signal. The peak detector has a resolution of 8 bit. This feature allows the digital control unit on one hand, to eliminate the signal offset. This function is realized with a dedicated Digital-to-Analog Converter (DAC). The DAC has a resolution of 12 bits. On the other hand, it allows the digital control unit to optimize amplifier gain and comparator hysteresis settings according to the actual signal amplitude. Due to these measures, the sensor system can handle a wide amplitude range. This amplitude range in turn allows the KMI25/2 and KMI25/4 to handle a wide range of air gaps between sensor and encoder. The hysteresis of the smart comparator prevents erroneous multiple switching due to mechanical vibrations of the encoder wheel. A further important feature of the smart comparator is, that it switches its output level always at the zero-crossing of its input signal. Thus, the phase of its rectangular output signal is independent of its hysteresis setting and independent of the gain setting at the amplifier. For this reason, adjustments of gain and hysteresis in the signal chain avoid the introduction of jitter into the sensor output signal. The whole signal chain works even under DC conditions, therefore having true zero Hertz capability.

The block labeled direction channel in Figure 1 within the PDIC builds the sum of the two AMR half-bridge output signals, which is referred to as direction signal. As already described above, the difference of the two half-bridge signals is processed as speed signal. Due to the displacement of the two half bridges in direction of the y axis, there is a phase shift between their output signals. The sign of this phase difference switches with direction of rotation. As a mathematical fact, the difference and sum signals are phase shifted to each other by either +90° or −90°. The sign of this phase shift also depends on the direction of rotation. Using these relations, the digital control unit detects the direction information by measuring the phase relation between the difference signal and the sum signal. For this purpose, also the offset at the sum signal is eliminated in the respective offset cancelation block.

In order to display it at the AK protocol, the digital protocol unit processes the following information:

- Amplitudes of speed and direction signals
- Detected direction
- Actual operation mode of signal conditioning circuit
- Status of pin DI

5.2 Speed signal conditioning algorithm

The digital control unit (see Figure 1) controls the speed signal conditioning algorithm. The general purpose is, to control the analog blocks in the speed channel to optimize signal conditions at the analog comparator input. Therefore, the algorithm characterizes the sensor input signal, as observed within the digital domain. As a result, the algorithm adjusts the amplifier gain, cancels the signal offset and sets the comparator hysteresis. To fulfill this task, the digital control unit provides switching between different operating modes. Depending on frequency and amplitude of the input signal, one of the following modes is selected:

- Start-up mode
- Adaptation mode
- Normal mode
- Low-speed mode

Figure 5 depicts a flow chart summarizing the most important features of each mode and the conditions for switching between modes. For each transition, all of the listed conditions must be satisfied (logical AND), unless the notation ‘or’ is used. The latter indicates a logical OR connection. In this case, the transition is performed if any of the listed conditions is satisfied.

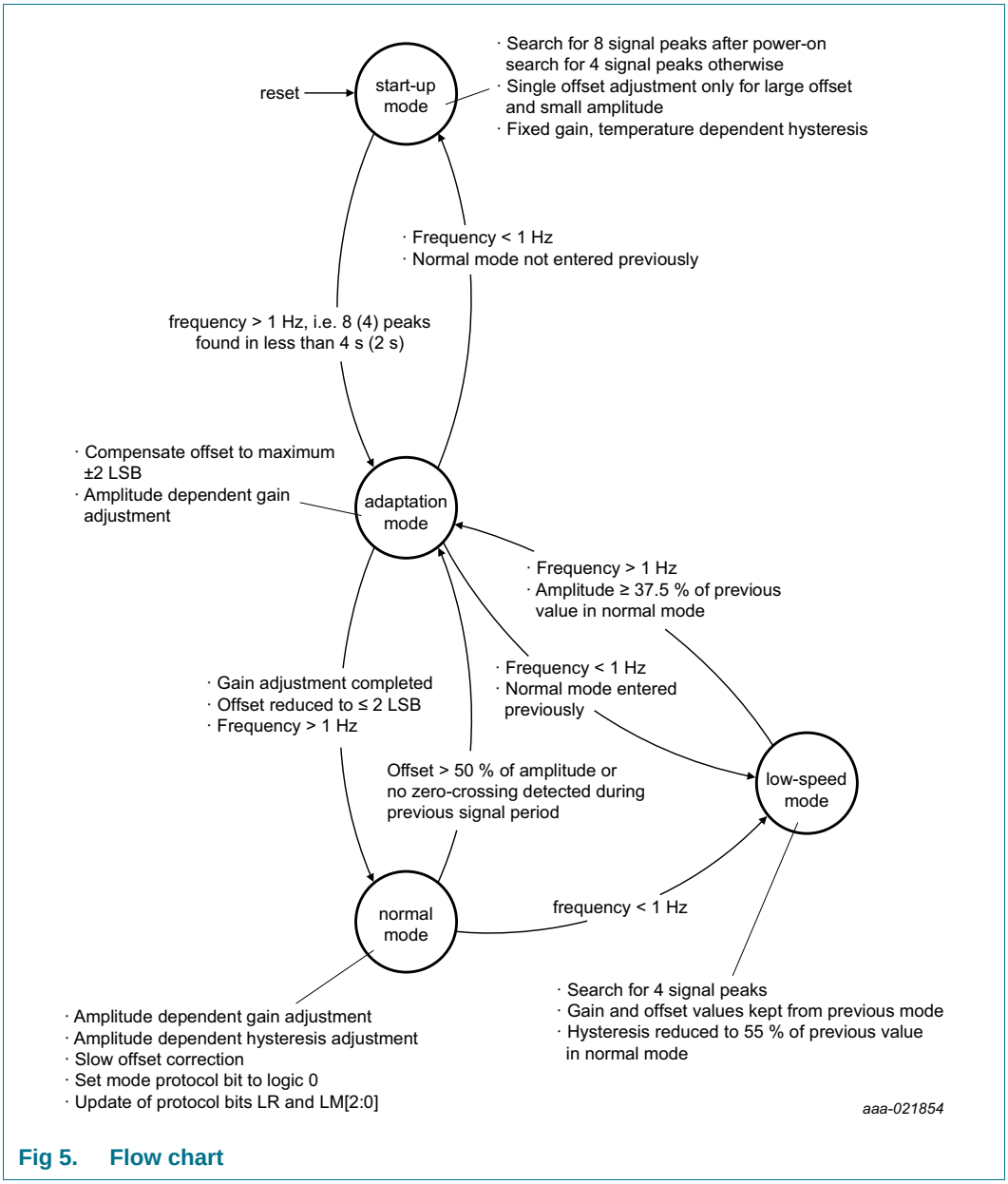


Fig 5. Flow chart

The following sections describe the implemented measurement functions for offset, amplitude and frequency as well as each operation mode.

5.2.1 Peak detector

The peak detector is part of the digital control unit. It samples the AMR input signal with a resolution of 8 bits and detects the positive and negative peak values. From these values, it calculates the signal offset and the signal amplitude. The offset is calculated as half of the sum of opposite signal peaks. The amplitude is calculated as difference of opposite signal peaks. Principally, a peak is detected, where the difference between succeeding signal samples switches its sign. In order to cope with superimposed noise and spurious spikes, the peak detector uses dedicated filter algorithms.

5.2.2 Frequency measurement

As pointed out above, the peak detector calculates the signal offset. This offset level is the ‘zero level’ of the sensor signal. Whenever the sensor signal crosses this ‘zero level’, the comparator switches its state.

If a zero-crossing with a falling edge is detected first, then frequency measurements are always made between falling edges. If a zero-crossing with a rising edge is detected first, then frequency measurements are always made between rising edges. Thus always a complete signal period is used and the result is independent of any duty cycle shifts.

The frequencies occurring in start-up mode and low-speed mode are very low. Thus, an indirect frequency measurement is done here by counting the number of signal peaks within 2 seconds.

5.2.3 Start-up mode

Usually the system enters this mode after power-on reset. At power-on, nothing is known about the input signal properties. The function of the speed control algorithm in start-up mode is to characterize the input signal and produce estimates of its amplitude, offset and frequency. Therefore, once the sensor element has been supplied with voltage, all circuit parts are set into defined initial conditions. These conditions comprise fixed amplifier gain and fixed (but temperature-dependent) comparator hysteresis. Furthermore, there is still no offset cancelation. This procedure may take up to 1 ms. The system starts then applying an appropriate offset correction in the direction channel and then switches to the speed channel. These initial conditions are used to process the sensor bridge signal in the first instant. Thereafter the system is ready to react on the input voltage.

If the first speed signal samples are near the positive or negative signal range limit, a large offset is assumed. In this case, an initial offset correction with a predefined level is executed. This function is applied to speed up the signal recognition in case of small signals superimposed on a large offset.

Generally, the ‘start-up’ performance strongly depends on the signal amplitude and its offset. Because of the possibility of missing the second zero-crossing, the first zero-crossing of the input signal is not used. So under normal conditions (offset is relatively small w.r.t. amplitude), the sensor issues the first speed pulse at its output with the second zero-crossing of the analog input signal. As there is no offset regulation during start-up mode, the speed pulses issued during this mode may be shifted in time w.r.t. the zero-crossings of the sensor signal. As a consequence, the duty cycle of the output signal may not yet fulfill the specification, if an external magnetic offset is present. For small amplitudes and large offsets, no zero-crossings may be detected during start-up mode until offset compensation is performed in adaptation mode.

If the peak detector has found 8 signal peaks within 4 seconds, start-up mode is left and adaptation mode is entered. However, if start-up mode has been entered coming from adaptation mode, then 4 signal peaks within 2 seconds cause reentering adaptation mode.

Even if no zero-crossing is detected, the sensor transmits the output protocol at a rate of typically 150 ms. The output of an artificial speed pulse instead of a real speed pulse indicates this condition (see Section 5.3.3).

5.2.4 Adaptation mode

The main purpose of adaptation mode is to optimize the signal conditions by adjusting gain and offset, based on the estimates made in start-up mode. After standstill or in a sudden change of signal offset, adaptation mode is entered as well.

In adaptation mode, offset compensation and gain setting are applied once per signal cycle. Offset compensation first takes place in correcting $^{7}/_{8}$ of the calculated offset per step. It continues until the residual offset is below a threshold of 2 Least Significant Bit (LSB). An exception occurs, if the remaining offset is larger than five times the signal amplitude. In this case, the correction of that step is limited to the remaining offset level.

In order to avoid the generation of erroneous additional zero-crossings, the activity of the offset compensation depends on the previous signal slope. Therefore, a positive offset is only corrected after a falling slope and a negative offset is only corrected after a rising slope.

If necessary, the amplifier gain is doubled or halfed, until the digital signal amplitude is between 25 % and 75 % of its range. The temperature-dependent hysteresis level at the comparator input is kept at the same percentage level w.r.t. to the signal range as in the previous mode.

The number of steps required for the adaptation process depends on the relation between offset and signal amplitude. Small amplitudes coming with a large offset require a maximum number of steps. In such cases, the first zero-crossing may not be detected in start-up mode, but in adaptation mode. As in start-up mode the second zero-crossing could be missed under certain conditions also in adaptation mode. Therefore, in order to ensure an uninterrupted pulse train, also in adaptation mode the first detected zero-crossing is not used. Hence under normal conditions, the first output signal is issued at the second detected zero-crossing.

The goal of the adaptations is a signal amplitude of 25 % to 75 % and an offset of maximal 2 LSB. If the frequency is greater than 1 Hz, the system then switches from adaptation mode to normal mode. If the frequency falls below 1 Hz, the previous mode is entered again (start-up mode or low-speed mode).

5.2.5 Normal mode

Normal mode is entered when the necessary adjustments to the gain and offset have been completed in adaptation mode. The goal of the normal mode is, to keep duty cycle and jitter of the output signal within specification. If normal mode is active, the mode bit within the AK protocol is set to logic 0. The mode bit is set to logic 1 during all other modes.

During normal mode, amplifier gain is still adapted proportional to signal amplitude as in adaptation mode. Thus, the input signal amplitude is between 25 % and 75 % of the signal range. The hysteresis control, which in start-up mode and adaptation mode is carried out depending on temperature, is now carried out depending on signal amplitude. Applied hysteresis levels are at 23 % to 52 % of the amplitude. Due to this measure, the hysteresis levels are high enough to provide a high level of immunity to noise and signal disturbances. On the other hand, the hysteresis is small enough to maintain continued comparator switching, even when offset jumps occur. For very small amplitudes, the hysteresis is not set below a fixed minimum level and the ratio hysteresis/amplitude can become greater than 52 %.

In adaptation mode, the offset has been reduced down to maximum 2 LSB using few coarse compensation steps. In normal mode however, the goal is to reach and maintain zero offset by using a slow offset correction. For this purpose, the offset compensation level is changed at a limited rate versus time, as long as a residual offset is detected. Due to this slow offset correction, duty cycle deviations and jitter of succeeding output pulses are minimized. If however offset changes at a faster rate than the slow correction can compensate, an increasing residual offset occurs. The residual offset causes a shift of the duty cycle δ_o at the output signal. In order to prevent δ_o from leaving the specified window (see characteristics in Table 10) or even loss of signal, the system switches back to adaptation mode. If the residual offset has become greater than 50 % of the amplitude, the system switches to adaptation mode. In adaptation mode, the remaining offset is minimized again, as described in Section 5.2.4.

If the signal frequency drops below 1 Hz, the system also leaves normal mode and enters low-speed mode.

Only during normal mode, the AK protocol bits which reflect the signal amplitude (LR and LM[2:0]) are updated at each zero-crossing. When switching from normal mode to another mode, the last bit settings from normal mode are kept constant, until the system enters normal mode again.

5.2.6 Low-speed mode

If during adaptation mode or normal mode, the frequency drops below 1 Hz low-speed mode is entered. If the vehicle is stationary, no signal peaks can be detected in order to calculate amplitude and offset. Thus, the algorithms for offset compensation and adaptation of gain and hysteresis cannot be applied. Therefore, low-speed mode acts as a standby mode. In this mode, some of the normal functions of the algorithms are suspended until the frequency returns above 1 Hz.

The previously calculated offset and gain setting are maintained, until the system returns to adaptation mode. The hysteresis thresholds of the comparator are lowered to 55 % of their previous value (if not the lowest hysteresis was already present). This measure allows an amplitude reduction up to 44 % without loss of comparator switching.

A special case is ‘signal clipping’ during low-speed mode. Signal clipping means, that the sensor signal reaches the positive or negative edge of the signal range. In this case, slow offset compensation, similar to normal mode is applied. The goal of this measure is to prevent, that the offset drift moves the full signal outside of the signal range.

The system leaves low-speed mode and enters adaptation mode as soon as the peak detector has found four signal peaks within two seconds. As an additional condition, the signal amplitude must be greater than 37.5 % of the value measured when entering low-speed mode.

If no zero-crossing has been detected for typically 150 ms, an output protocol with an artificial speed pulse is transmitted. Thus, the protocol is transmitted at a rate of at least 150 ms.

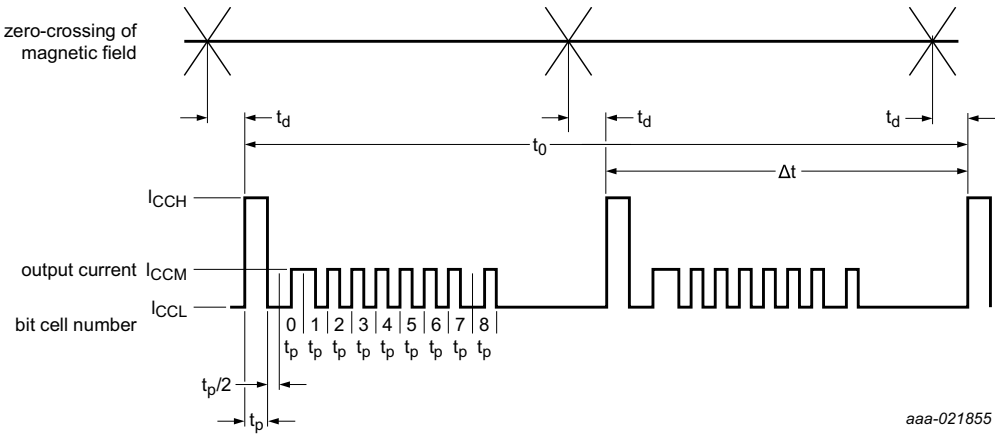
5.3 Output signal

5.3.1 Physical representation of output signal

The output signal is shown in Figure 6. A short speed pulse is transmitted after the delay t_d whenever a zero-crossing of the input signal is detected. After the speed pulse, the digital protocol unit begins to transmit the data protocol bits. Between speed pulse and the first data cell, there is a gap of $t_p/2$.

The data protocol consists of 8 data bits and a parity bit. The meaning of each bit is given in Table 4.

A short pulse at HIGH-level current (typically 28 mA) reflects the gear wheel structure. Pulses at MID-level current of typically 14 mA reflect the subsequent protocol bits.



output duty cycle: $\delta_o = \frac{\Delta t}{t_0} \times 100\ \%$

Fig 6. Timing of output signal to input signal and definition of duty cycle δ_o

Figure 7 shows the physical representation of the protocol data bits. The protocol data bit has a bit length t_p. It is divided into two half-signal parts by the current edge in the middle of the data bit. A rising current edge defines logic 1 whereas a falling current edge defines logic 0. A data bit without current edge in the middle is invalid. This Manchester code transmission is chosen for easy clock recovery.

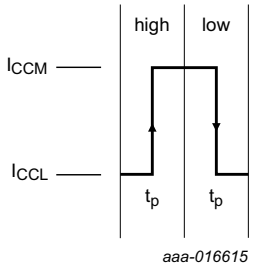


Fig 7. Representation of AK protocol bits

5.3.2 Definition of AK protocol

Table 4 summarizes the information coded by the AK protocol bits.

Table 4. Definition of AK protocol bits

Bit	Symbol	Description	Remark	Bit value directly after power-up
0	LR	field amplitude too small	1 if field amplitude is too low to stay in normal mode; see Table 5	0
1	M	mode state	0 during normal mode, 1 during other modes	1
2	DI	state of digital input	1 if resistance between pin DI and pin GND is lower than minimum value of R_{ext}; 0 if resistance between pin DI and pin GND is higher than maximum value of R_{ext}; see characteristics in Table 10	0
3	VDR	validity of direction recognition	1 if direction bit is valid, normal mode and $f < f_H$ limit for valid direction detection; see characteristics in Table 10	0
4	DR	direction recognition	0 if direction is positive; see Figure 9 and Figure 10	0
5	LM0	field amplitude bit 0, LSB	the field amplitude is divided into 7 segments; see Table 6; valid output only in normal mode	0
6	LM1	field amplitude bit 1		0
7	LM2	field amplitude bit 2, Most Significant Bit (MSB)		0
8	P	parity	1 for even parity: P = XOR (bit 0 to bit 7)	1

Table 5 summarizes the typical magnetic field amplitudes at T_{amb} = 25 °C, below which the LR bit is set to logic 1.

Table 5. Typical magnetic field amplitudes at T_{amb} = 25 °C, below which bit LR is set to logic 1

KMI25/2	KMI25/4	Unit
< 62	< 87	A/m

Table 6 summarizes the switching levels of typical magnetic field amplitudes at T_{amb} = 25 °C, coded by the LM bits.

Table 6. Typical magnetic field amplitudes at T_{amb} = 25 °C, coded by LM bits

LM2	LM1	LM0	KMI25/2	KMI25/4	Unit
0	0	0	< 73	< 104	A/m
0	0	1	> 73	> 104	A/m
0	1	0	> 135	> 191	A/m
0	1	1	> 243	> 345	A/m
1	0	0	> 424	> 603	A/m
1	0	1	> 735	> 1045	A/m
1	1	0	> 1331	> 1893	A/m
1	1	1	> 2447	> 3485	A/m

5.3.3 Operation at low speed

If the last detected zero-crossing of the input signal is older than T_{stop}, the same protocol is transmitted as before. T_{stop} is typically 150 ms, see characteristics in Table 10. It is repeated from there on every T_{stop}, until a new zero-crossing is detected. If no zero-crossing is detected within 1 s or the relevant hysteresis level not passed within 250 ms, the system enters low-speed mode. If the system was in normal mode before, the mode bit is set from logic 0 to logic 1. In the repeated protocol in place of the speed pulse, an artificial speed pulse of amplitude I_{CCM} is transmitted. A special case occurs, if the system detects a new zero-crossing while a repeat transmission is running. In this case, the repeat transmission is terminated, before the new speed pulse is issued. Due to the delay time t_d, the running bit transmission can be finalized correctly. There is a gap of at least $t_p/2$ between the end of the last bit and the new speed pulse.

The situation depicted in Figure 8 shows how a running repeat protocol is terminated because a new zero-crossing is detected. In this example, the bit values are: LR = 0, M = 0, DI = 1, VDR = 1, DR = 1, LM[2:0] = 5 (see Table 4). With M = 0 and existing repeat protocol, the system is operating between 6.67 Hz and 1 Hz.

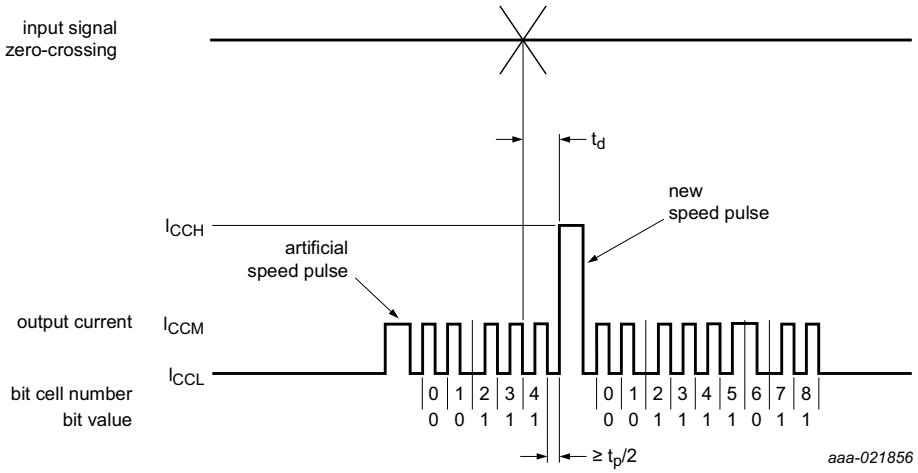


Fig 8. Timing of output signal at low speed

5.3.4 Operation at high speed

The number of data protocol bits transmitted by the digital protocol unit is dependent on the input signal frequency. At high frequencies, not all 9 data bits can be sent between two speed pulses. In that case, some protocol bits are omitted. However each bit, started before a new zero-crossing of the input signal, is correctly finalized. This feature is due to the introduced delay between the zero-crossing of the input signal and the start of the speed pulse. The situation is as shown in Figure 8 except that there is always a speed pulse. The protocol bits that are transmitted can be found in Table 7. Spreads shown are due to the spread of the internal oscillator. The higher its frequency the more bits fit into one signal period. If there is an uncorrected offset, the duty cycle is unequal 50 %. In this case, the first and second half of an input signal cycle might be different.

Table 7. Transmitted protocol bits at high speed

Encoder frequency up to which protocol bits are transmitted					
Bit range	**at 50 % duty cycle**			**inclusive 40 % to 60 % duty cycle variation**	
	minimum signal frequency [Hz]	**typical signal frequency [Hz]**	**maximum signal frequency [Hz]**	**minimum signal frequency [Hz]**	**maximum signal frequency [Hz]**
Bit 0 to bit 8	768	921	1151	614	1382
Bit 0 to bit 7	844	1013	1266	675	1520
Bit 0 to bit 6	983	1125	1407	750	1688
Bit 0 to bit 5	1055	1266	1582	844	1899
Bit 0 to bit 4	1205	1446	1808	964	2169
Bit 0 to bit 3	1406	1687	2108	1124	2530
Bit 0 to bit 2	1686	2023	2529	1349	3034

5.3.5 Definition of positive direction of rotation

If the encoder rotation direction is according to Figure 9 and Figure 10, the direction bit of the AK protocol (bit 4, see Table 4) is at logic 0. In the opposite direction, the direction bit is at logic 1.

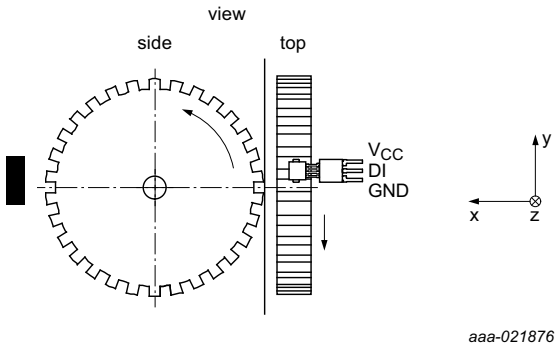


Fig 9. Positive direction of rotation with passive encoder (ferromagnetic gear wheel)

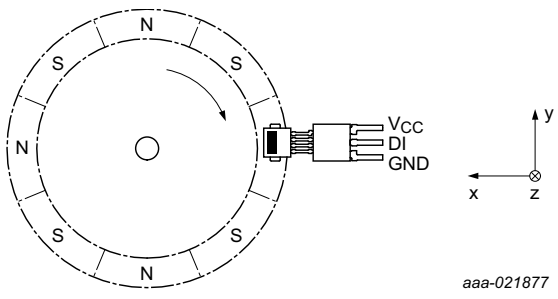


Fig 10. Positive direction of rotation with active encoder (multipole wheel)

5.4 Digital input pin

This pin allows the user to transfer one-bit information to the sensor device for arbitrary diagnostic purposes. Physically, an external resistance R_{ext} between pin DI and pin GND represents this one-bit information. The status of this bit appears as bit DI in the AK protocol (see Table 4). If R_{ext} is lower than a given threshold $R_{ext(min)}$, bit DI outputs logic 1. If R_{ext} is greater than a given threshold $R_{ext(max)}$, bit DI outputs logic 0 (see characteristics in Table 10).

The value of the external resistor is evaluated each time a speed pulse is present. The result of this measurement is then used to update the status of bit DI at the AK protocol transmission which belongs to that speed pulse. After power-on bit DI is set to logic 0 until the first speed pulse is generated. If no speed pulse is generated, i.e. if the supply current is at LOW-level or MID-level, R_{ext} is not measured and bit DI keeps its status. This behavior holds also for the transmission of artificial speed pulses at very low speed or standstill.

The resistance measurement is carried out, while current source I_H is active, i.e. during output of a speed pulse. In this case, a current of typically 21 mA flows through the parallel connection of R_{ext} and the internal resistance R_{int} (see characteristics in Table 10). In order to get the desired one-bit information, the resulting voltage drop is compared to a reference voltage. If the pin DI is left open, the voltage drop V_o appears at this pin. V_o is the voltage drop across R_{int} due to the current of 21 mA (see characteristics in Table 10).

If pin DI is not used, it should be connected to pin GND.

6. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referred to pin GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	normal operation mode			
		$-40\ °C < T_{amb} < +60\ °C$; t < 2 minutes	-	24	V
		$-40\ °C < T_{amb} < +60\ °C$	-	18	V
		$-40\ °C < T_{amb} < +150\ °C$	-	16	V
		$150\ °C < T_{amb} < 175\ °C$; 10 × 10 minutes during total life time; none destructive but no functionality granted	-	16	V
		V_{CC} and GND incidentally swapped	−16.5	-	V
I_{DI}	current on pin DI	$-40\ °C < T_{amb} < +25\ °C$; t < 2 minutes	−80	+80	mA
T_{amb}	ambient temperature		−40	+150	°C
		for 10 × 10 minutes during total life time; $V_{CC} < 16$ V	−40	+175	°C
T_{stg}	storage temperature	no voltage applied	−50	+150	°C
T_{sld}	soldering temperature	for maximum 5 s	-	260	°C
H_{ext}	external magnetic field strength		-	30	kA/m

7. Recommended operating conditions

Table 9. Operating conditions

Voltages are referred to pin GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	normal operation mode; $T_{amb} \leq 175$ °C	6.8	16	V
R_L	load resistance		-	50	Ω
T_{amb}	ambient temperature	normal operation mode	–40	+150	°C
f_H	magnetic field strength frequency		0	2.5	kHz
H_M	peak magnetic field strength	after power-on; speed pulses latest after $N_{cy(H)}$ magnetic cycles; see characteristics in Table 10			
		KMI25/2	150	-	A/m
		KMI25/4	190	-	A/m
		after power-on; valid direction output signal latest after $N_{cy(H)}$ magnetic cycles; see characteristics in Table 10			
		KMI25/2	200	-	A/m
		KMI25/4	210	-	A/m
$\lvert H_{offset(ext)} \rvert$	external magnetic field strength offset (absolute value)	to allow correct start-up after power-on			
		KMI25/2	-	528	A/m
		KMI25/4	-	911	A/m
ΔH_M	peak magnetic field strength variation	allowable sudden change of magnetic signal peak level without loss of speed pulses			
		non-recurring changes	–40	+100	%
		periodic changes	–10	+10	%

8. Characteristics

Table 10. Characteristics

Characteristics are valid for the operating conditions specified in Section 7; voltages are referred to pin GND; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage and current						
$V_{CC(swon)}$	switch-on supply voltage	[1]	5.8	6.3	6.8	V
$t_{d(on)}$	turn-on delay time	[2]	-	-	1	ms
$V_{CC(swoff)}$	switch-off supply voltage	[1]	4.0	4.5	5.0	V
$V_{CC(hys)}$	supply voltage hysteresis	switch-on/switch-off	1.6	1.8	2.8	V
$I_{CC(swoff)}$	switch-off supply current	$V_{CC} < 4$ V	1.0	3.0	3.8	mA
I_{CCL}	LOW-level supply current		5.88	7.0	8.4	mA
I_{CCM}	MID-level supply current		11.7	14.0	16.8	mA
I_{CCH}	HIGH-level supply current		23.5	28.0	33.6	mA
I_{CCM}/I_{CCL}	MID-level supply current to LOW-level supply current ratio		1.8	2.0	-	-

Table 10. Characteristics *…continued*

Characteristics are valid for the operating conditions specified in Section 7; voltages are referred to pin GND; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CCH}/I_{CCL}	HIGH-level supply current to LOW-level supply current ratio		3.6	4.0	-	-
dI_{CC}/dt	rate of change of supply current	I_{CCL} to I_{CCH} and I_{CCL} to I_{CCM} (10 % to 90 % and 90 % to 10 %)	6	-	28	mA/µs
Timing parameters						
t_d	delay time	delay between magnetic zero-crossing and output switching; see Figure 6	70	-	121	µs
t_p	pulse duration	duration of speed pulses and AK protocol bits; see Figure 6	40	50	60	µs
T_{stop}	stop period	stand still period	105	150	195	ms
σ(T)	period jitter	one-sigma value; required peak level of magnetic signal: H_M = 280 A/m (KMI25/2) H_M = 398 A/m (KMI25/4)	–0.1	-	+0.1	%
		one-sigma value; required peak level of magnetic signal: H_M = 55 A/m (KMI25/2) H_M = 78 A/m (KMI25/4)	–0.5	-	+0.5	%
δ_o	output duty cycle	required peak level of magnetic signal: H_M = 55 A/m (KMI25/2) H_M = 78 A/m (KMI25/4) [3]	30	-	70	%
		required peak level of magnetic signal: H_M = 75 A/m (KMI25/2) H_M = 107 A/m (KMI25/4) [3]	40	-	60	%
Digital input						
R_{int}	internal resistance	pin DI to pin GND	-	10	-	Ω
V_o	output voltage	open circuit for pin DI; pin DI to pin GND; only present during output of speed pulse, i.e. $I_{CC} = I_{CCH}$	-	210	-	mV
R_{ext}	external resistance	pin DI to pin GND; AK protocol				
		bit DI = 1	-	-	20	Ω
		bit DI = 0	150	-	-	Ω
Direction detection						
N_{spd}	number of speed pulses	until direction indication is valid after power-on or change in direction	-	-	2	-
f_H	magnetic field strength frequency	limit for valid direction detection	800	1000	-	Hz
		hysteresis for direction detection	28	40	52	Hz
Start-up performance after power-on, if magnetic field amplitude > minimum value of H_M and f_H > 1 Hz						
$N_{cy(H)}$	number of magnetic field cycles	no external magnetic offset; duty cycle within specification	-	-	15	-
		no external magnetic offset; mode bit set to logic 0	-	-	16	-
		maximum allowed external magnetic offset; duty cycle within specification	-	-	23	-
		maximum allowed external magnetic offset; mode bit set to logic 0	-	-	24	-

[1] Once V_{CC} has exceeded $V_{CC(swon)}$, the sensor switches on and current levels and current ratios are maintained until V_{CC} falls below $V_{CC(swoff)}$.

[2] After supplying more than $V_{CC(swon)}$ to the device, it needs a turn-on delay time of $t_{d(on)}$ to reach stable operation. A stable supply current indicates stable operation.

[3] During normal mode; for definition of duty cycle see Figure 6.

9. ElectroMagnetic Compatibility (EMC)

The following tests by an independent and certified test laboratory have verified EMC:

9.1 Emission

- CISPR 25 (2008, third edition), Chapter 6.2: conducted emission, voltage method
- CISPR 25 (2002, second edition), Chapter 6.4: radiated emission, Absorber-Lined Shielded Enclosure (ALSE) method

9.2 Immunity to electrical transients

Tests were carried out with external protection circuit.

- ISO 7637-3: electrical transient transmission by capacitive coupling

9.3 Immunity to radiated disturbances

- ISO 11452-2: antenna in ALSE, including radar pulses
- ISO 11452-4: Bulk Current Injection (BCI)
  - Substitution method
- ISO 11452-5: strip line

10. ElectroStatic Discharge (ESD)

The following tests have verified ESD:

10.1 Human body model (AEC-Q100-002)

±8 kV at external pins (V_{CC}, DI and GND)

±500 V at internal AMR bridge pins

10.2 Machine model (AEC-Q100-003)

±400 V at external pins (V_{CC}, DI and GND)

±100 V at internal AMR bridge pins

10.3 Charged-device model (AEC-Q100-011)

±1 kV at external pins (V_{CC}, DI and GND)

±500 V at internal AMR bridge pins

11. Application information

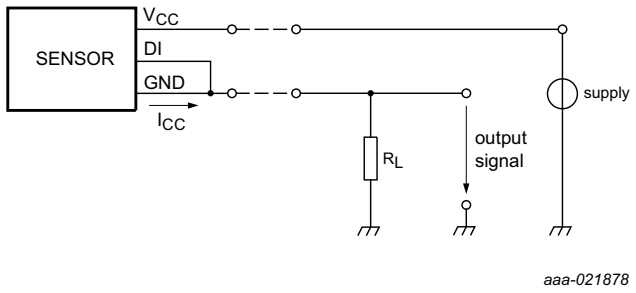


Fig 11. Test and application circuit (pin DI unused)

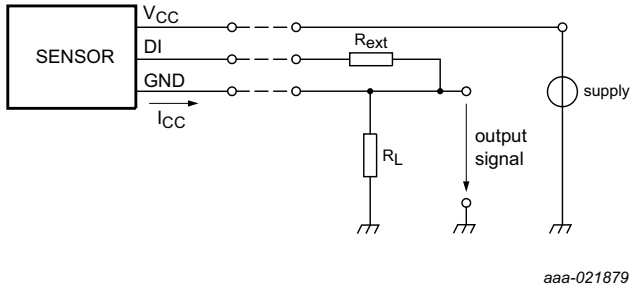


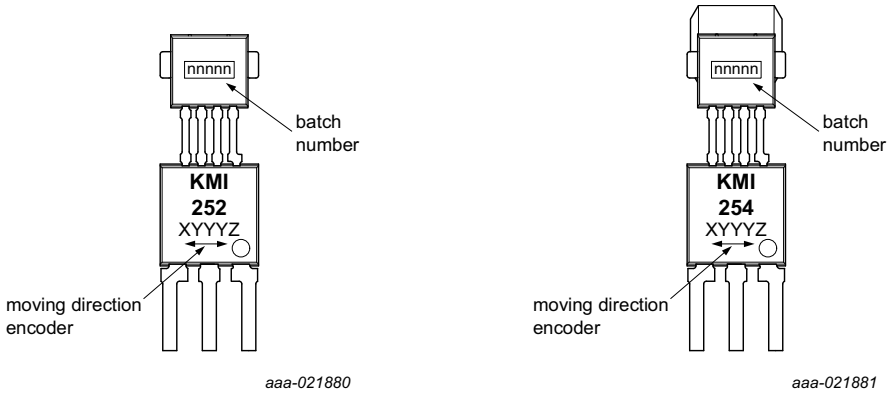
Fig 12. Test and application circuit (pin DI used)

12. Test information

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G (grade 0) - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13. Marking



X: product manufacturing code; m for manufacturing Manila and p for manufacturing Hong Kong

YYY: day of year

Z: year of production (last figure)

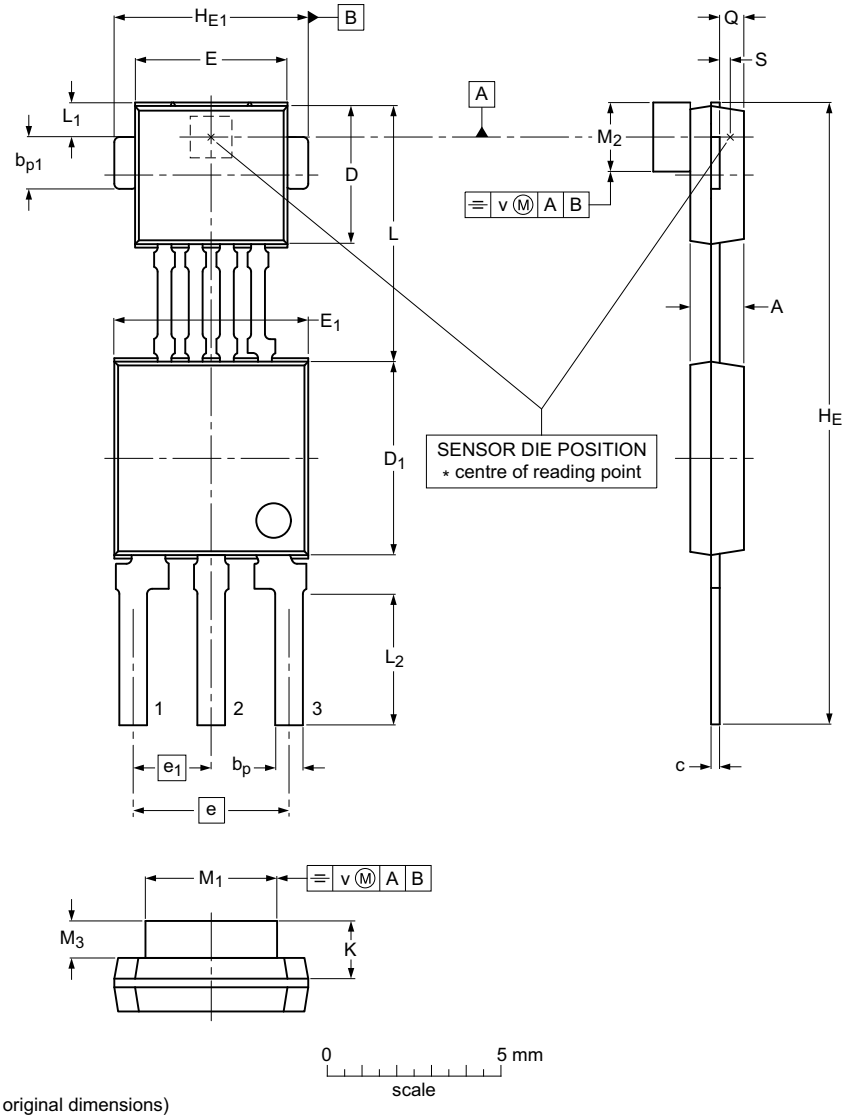
a. KMI25/2

b. KMI25/4

Fig 13. Marking

14. Package outline

Plastic single-ended multi-chip package;
magnetized ferrite magnet (3.8 x 2 x 0.8 mm); 4 interconnections; 3 in-line leads **SOT477A**



Dimensions (mm are the original dimensions)

Unit[1]		A[1]	b_p	b_{p1}	c	D	D_1	E	E_1	e	e_1	H_E	H_{E1}	K	L	L_1	L_2	M_1	M_2	M_3[1]	Q	S	v
mm	max	1.7	0.8	1.57	0.30	4.1	5.7	4.5	5.7	4.6	2.35	18.2	5.6	1.67	7.55	1.2	3.9	3.9	2.1	0.90	0.75	0.48	0.25
	nom																						
	min	1.4	0.7	1.47	0.24	3.9	5.5	4.3	5.5	4.4	2.15	17.8	5.5		7.25	0.9	3.5	3.7	1.9	0.75	0.65	0.28	

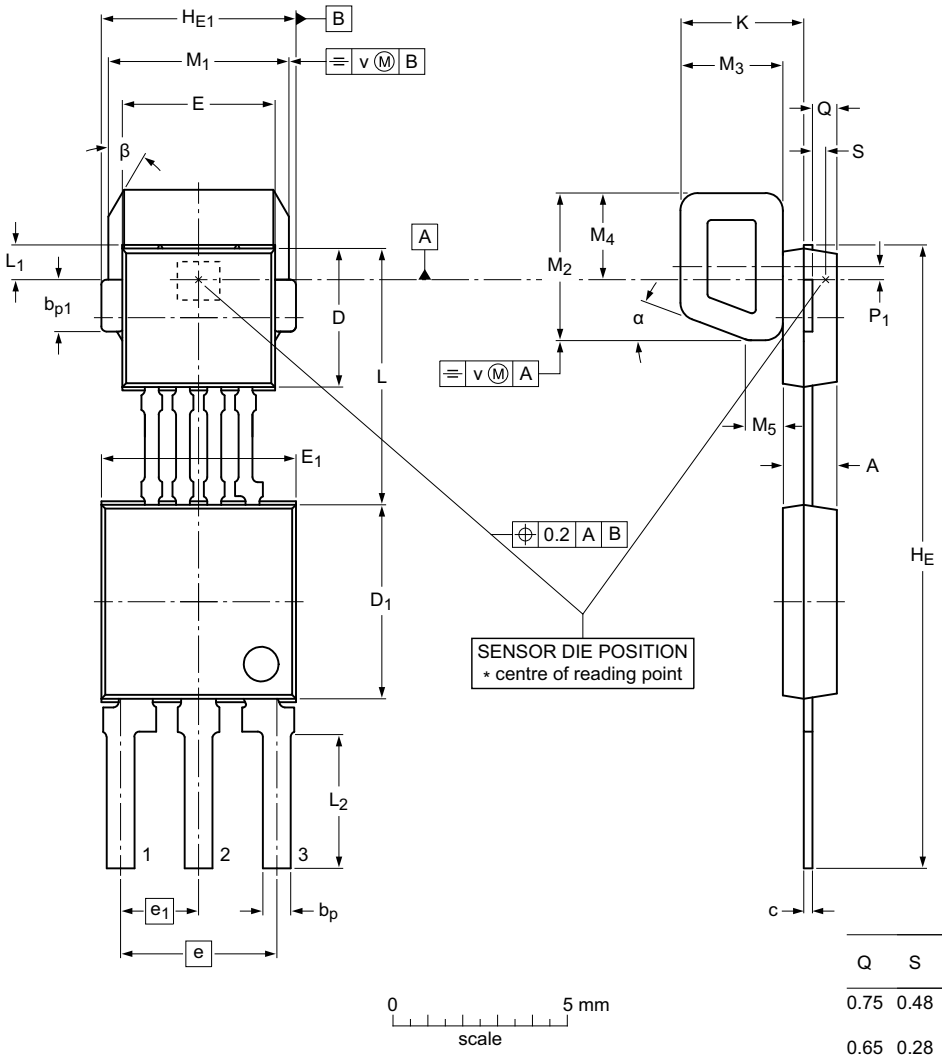
1 mm around the plastic body the lead finish is uncontrolled.
Note
1. Glue thickness not included.

sot477a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT477A						~~16-02-10~~ 16-02-26

Fig 14. Package outline SOT477A (SIP3)

Plastic single-ended multi-chip package;
magnetized ferrite magnet (5.2 x 4.25 x 2.95 mm); 4 interconnections; 3 in-line leads **SOT477E**



Q	S	v	α	β
0.75	0.48	0.25	25°	35°
0.65	0.28		15°	25°

Dimensions

Unit		$A^{(1)}$	b_p	b_{p1}	c	D	D_1	E	E_1	e	e_1	H_E	H_{E1}	K	L	L_1	L_2	M_1	M_2	$M_3^{(1)}$	M_4	M_5	P_1
mm	max	1.7	0.8	1.57	0.3	4.1	5.7	4.5	5.7	4.6	2.35	18.2	5.6	3.77	7.55	1.2	3.9	5.4	4.45	3.05	2.725	1.2	
	nom																						0.375
	min	1.4	0.7	1.47	0.24	3.9	5.5	4.3	5.5	4.4	2.15	17.8	5.5		7.25	0.9	3.5	5.0	4.05	2.85		0.8	

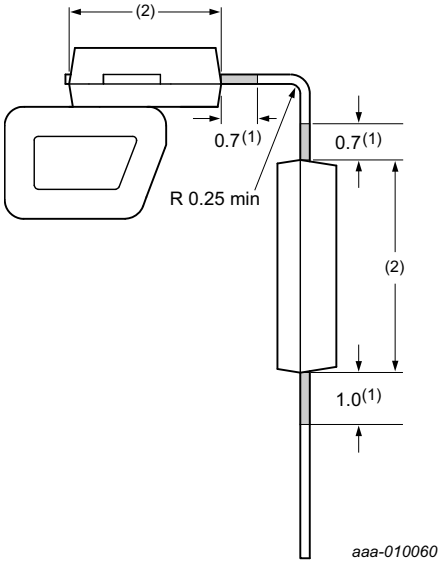
1 mm around the plastic body the lead finish is uncontrolled.
Note
1. Glue thickness not included.

sot477e_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT477E						~~16-02-23~~ 16-02-26

Fig 15. Package outline SOT477E (SIP3)

15. Handling information



Dimensions in mm

(1) No bending allowed.

(2) Plastic body and interface plastic body - leads: application of bending forces not allowed.

Fig 16. Bending recommendation

16. Solderability information

The solderability qualification is according to AEC-Q100 Rev-G. Recommended soldering process for leaded devices is wave soldering. The maximum soldering temperature is 260 °C for maximum 5 s. Device terminals are compatible with laser and electrical welding. The device is reflow capable.

17. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
KMI25_2_4 v.1	20160429	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

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