IA700
Datasheet v1.0

IA700
Ultra-Low Power Audio Edge Processor

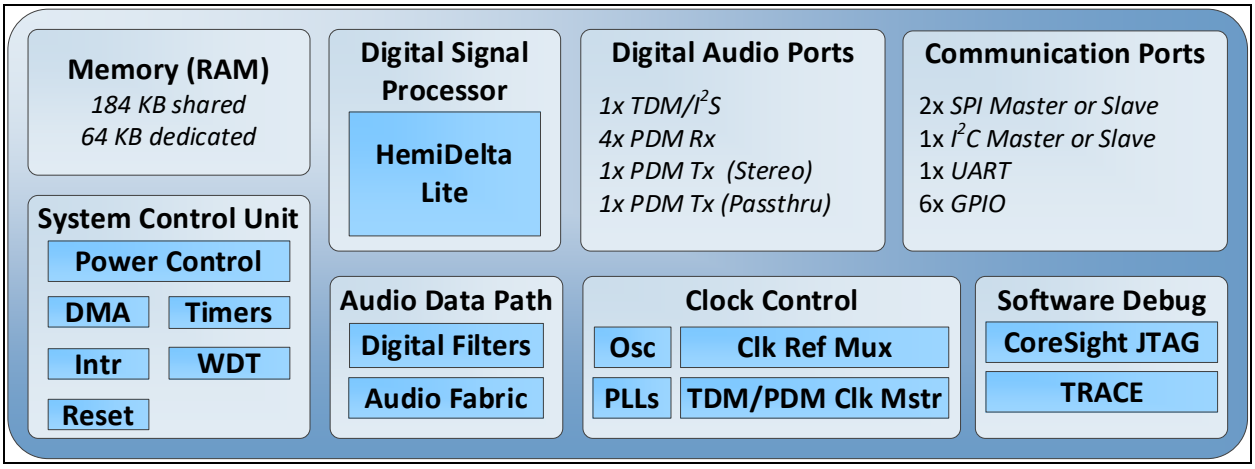
The IA700 is an AiSonic™ Ultra-Low Power Audio Edge Processor featuring Voice Wake and Voice ID keyword detectors and a two-second buffer[1] in a 24-pin QFN package. The IA700 offers flexibility by supporting the most relevant audio and data interfaces. The Audio DSP with 248 Kbytes of RAM is available for customer and third party algorithms, enabling unlimited creativity. The solution pushes system performance to ultra-low power with its custom core design and accelerates time to market with its highly integrated combination of hardware, software, and firmware.

Product Features

- Audio optimized Xtensa 64-bit two-way floating-point Single Instruction Multiple Data (SIMD) DSP core.
- 64 KB on-chip ROM.
- 248 KB on-chip RAM that includes at least 168 KB of user accessible memory for code and data.
- A TDM/I2S Master/Slave port.
- Up to two digital microphone (PDM) input channels and a stereo PDM output.
- Machine learning capability and Tensor Flow Lite (TFLu) support.
- Increased flexibility with I2C/UART/SPI interfaces.
- 24-pin QFN, 0.4mm pitch, 3.5 x 3.5 x 0.75 mm.

Typical Applications

- Remote controls
- Smart home devices
- Headsets and true wireless earbuds
- Near field voice activated controls
- Internet of Things (IoT) Devices
- Edge ML processor



[1] Buffer size varies based on the use-case and algorithm.

Specification Summary

Absolute Maximum Ratings

Parameter	Absolute Maximum Ratings	Units
VDD_IO to Ground	-0.3, +3.3	V
VDD_LDOD/A to Ground	-0.3, +1.5	V
Digital Input to Ground	-0.3, VDD_IO+0.3	V
Input Current (any pin)	±5	mA
Storage Temperature	-55 to +150	ºC

Note: Stresses exceeding these Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under Specifications and Electrical Characteristics is not implied. Exposure beyond those indicated under Specifications and Electrical Characteristics for extended periods can affect device reliability.

Specifications

Test Conditions: VDD_IO = 1.8V, VDD_LDOD/A = 1.1V at TA =25 ºC, PDM + SPI mode, 3.072 MHz clock, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Supply Voltage	VDD_IO	-	1.71	1.8	1.98	V
	VDD_LDOD	-	1.05	1.1	1.15	V
	VDD_LDOA	-	1.05	1.1	1.15	V
Supply Current	-	Retention Sleep Mode	-	TBD	-	-
		Voice Wake AAD Mode (stage 0)	-	TBD	-	
		Voice Wake Keyword Detect Mode (stage 1)	-	TBD	-	
		Voice Wake Burst Mode (stage 2)	-	TBD	-	
Operational Ambient Temperature	T_A	-	-20	25	85	ºC

Table of Contents

Chapter 1: Product Description

1.1 Overview

The Knowles IA700 Audio Edge Processor is a flexible, ultra-low power, and highly integrated voice and audio processor for battery-powered applications. The IA700 includes the following:

- An advanced, Knowles audio-optimized DSP subsystem that:
  - Runs compute-intensive audio processing algorithms with very low power consumption
  - Provides an efficient interface between custom software and the digital audio stream data.
- A System Control Unit (SCU) that handles booting, resetting, and power management states such as deep-sleep mode, stage 0 and stage 1 Voice Wake activity.
- A flexible internal clock generation and routing system.
- Integrated interfaces for PDM and I^2S/TDM digital audio data.
- A variety of control interfaces, including UART, SPI slave, or I^2C slave. All have a control messaging and audio streaming capability.

Optimize IA700 for low power operation in a wide array of applications, including IoT devices.

The IA700 includes a set of reference drivers for common operating systems and platforms, allowing for easy integration and quick time-to-market. It allows communication/data transmission through the system interfaces listed in Table 1.

Table 1 System Interfaces

Control Messages	Audio Ports	Audio Upload
I2C	I2S	I2S
UART	I2S	I2S
SPI	PDM	SPI
UART	PDM	UART
I2C	PDM	I2C

Note: A user can only use one control interface at a time. For more information, see Chapter 5:.

1.2 Key Features

- Voice Wake
  - Ultra-low power.
  - Always listening in keyword detection mode.
  - Detection of either programmed (OEM) or user-trained keyword (Voice ID).
  - Continuous Voice Wake (CVQ) for a seamless transition from Voice Wake to the command phrase that follows.
- SPI Slave interface for fast code download and control.
- OpenDSP (ODSP): Low power operation, DSP clock rate up to 100 MHz, 248 kB total on-chip RAM, 168 kB RAM available for algorithms.
- Support for up to two PDM microphones for dual-mic processing such as beamforming.

1.3 AuViD Firmware Build Tool

Knowles offers AuViD, a comprehensive tool for firmware development and testing, as well as IA700 system configuration.

Engineers can use AuViD to configure, debug, and design. The system capabilities include audio streaming, system and route configuration; which performs either of the following:

- Offline sysconfig configuration and audio stream decoding.
- Connected to the host directly for run-time debugging using a host interface (I2C, UART, or SPI)

1.4 Typical Application Block Diagrams

Figure 1 and Figure 2 shows typical block diagrams for a host system using the IA700. (For pin configuration per boot mode, see Table 9 and Table 1.)

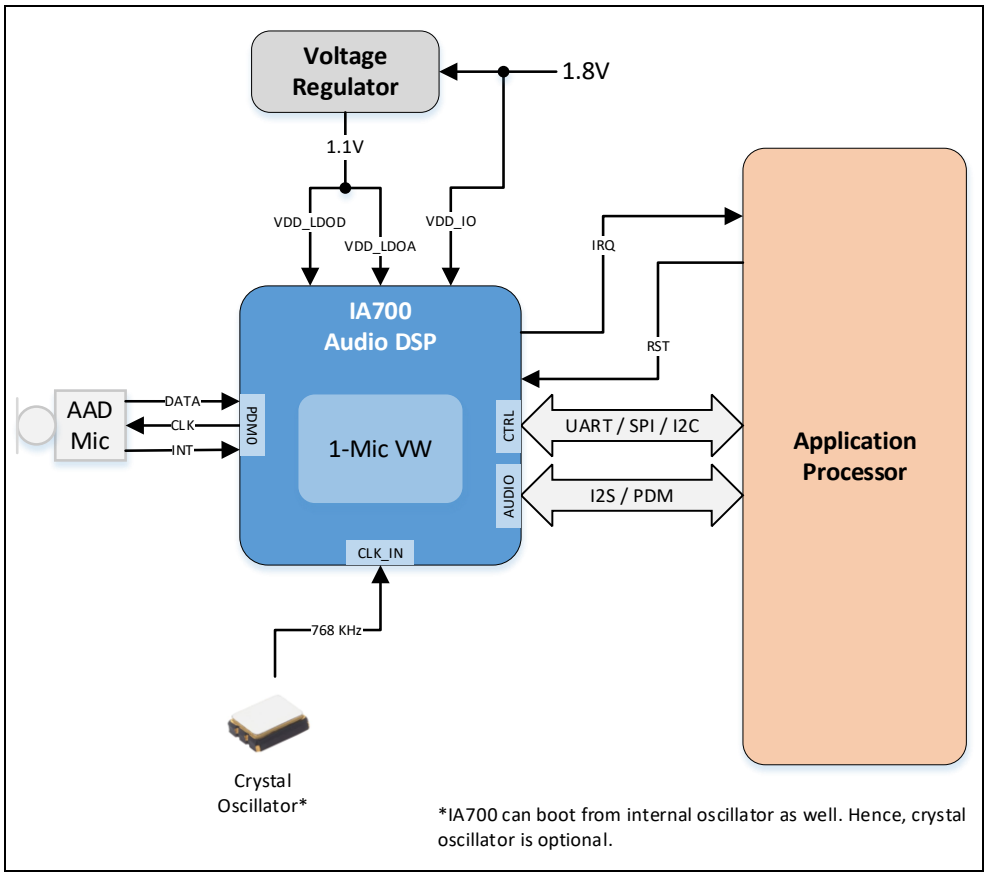


Figure 1 Application Schematic for a 1-mic Voice Wake with HW AAD (e.g. Remote Control)

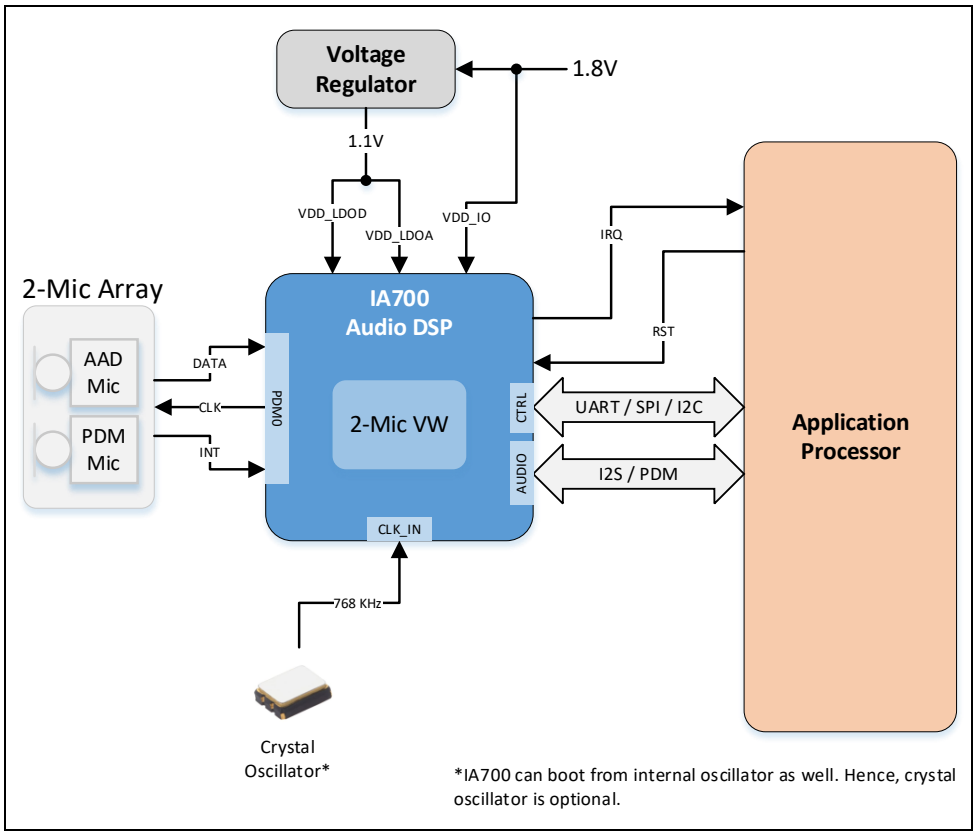


Figure 2 Application Schematic for a 2-mic Voice Wake with HW AAD

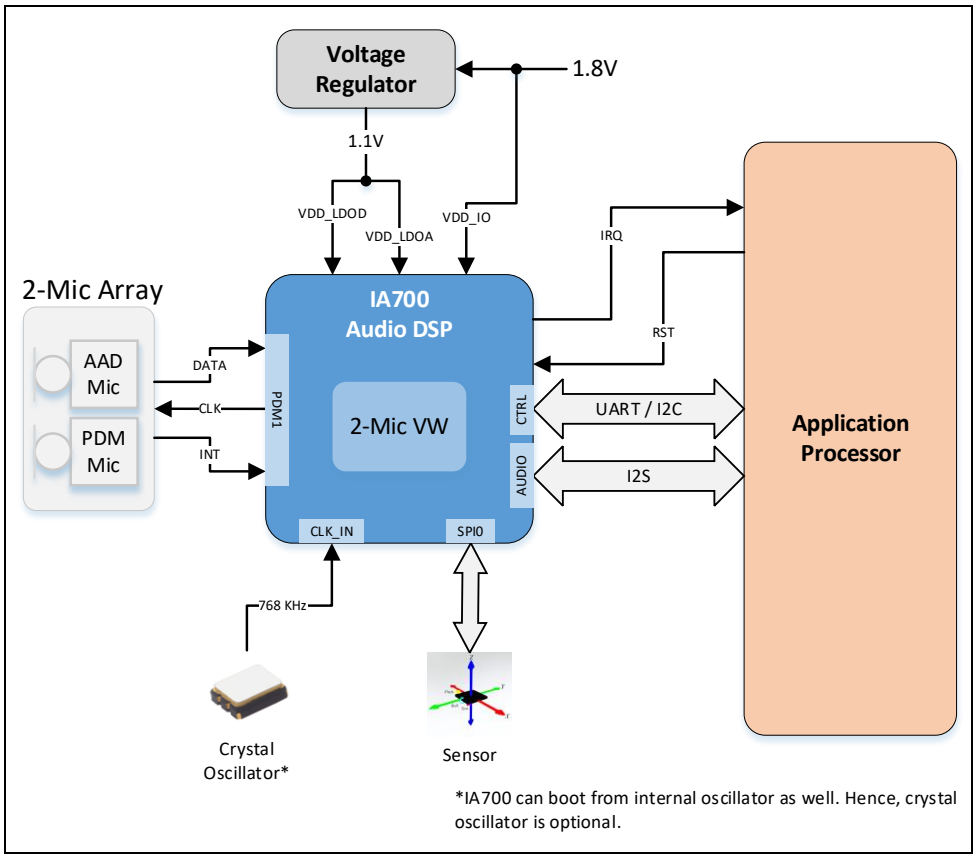


Figure 3 Application Schematic for a 2-mic Voice Wake with a Sensor

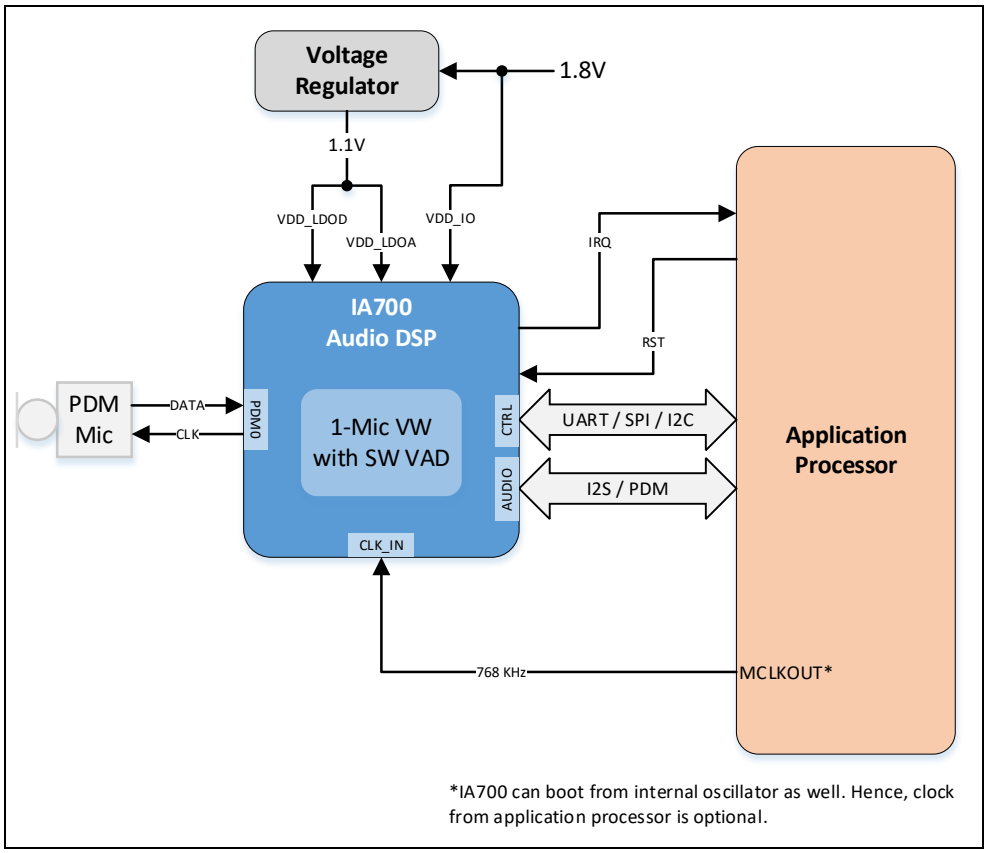


Figure 4 Application Schematic for a 1-mic Voice Wake with SW VAD, CLK_IN from AP

Chapter 2: Chip Description

The following are the major modules of the IA700 as shown in Figure 5:

- Ultra-low power and high-performance DSP sub-system.
- A Digital Audio Interface module that provides configurable serial digital audio ports capable of streaming a wide variety of data formats such as PDM, I2S, or TDM.
- SPI, UART, and I²C Host Interfaces that includes:
  - Communication with the host.
  - A channel for high-speed firmware downloads.
  - Audio data bursting for Voice Wake or diagnostic purposes.
- The System Control Unit (SCU) that handles booting, resetting, and power management states such as deep-sleep mode.
- An internal clock control module that generates internal clock signals and masters output clocks; it also locks internal time bases to externally provided clocks.
- System interrupt module, which provides:
  - Interrupt to host for keyword detection events.
  - Event handling to IA700 for host wakeup.

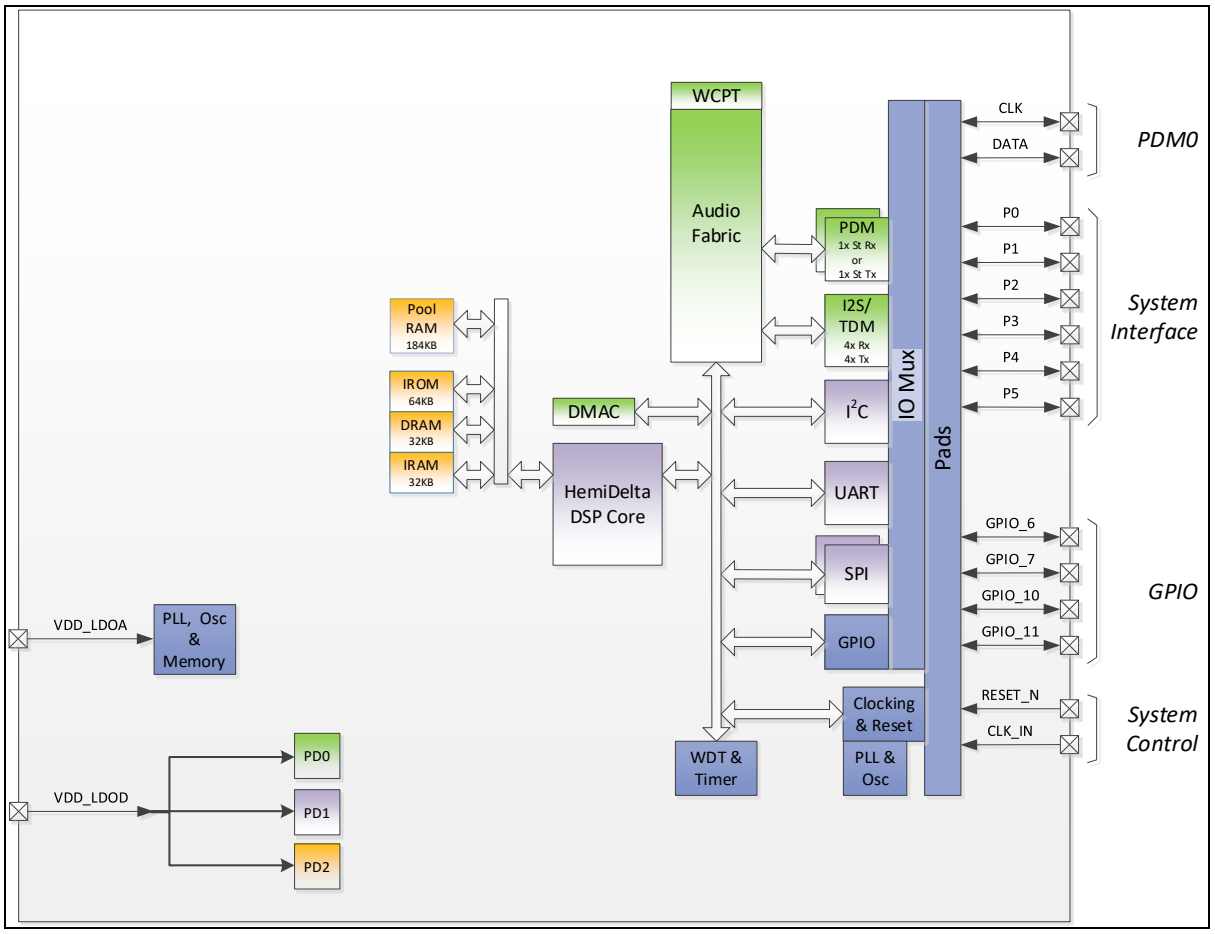


Figure 5 IA700 Block Diagram

2.1 DSP Subsystem

The DSP subsystem consists of the following:

1. A Hemi Delta (HMD) processor
2. Digital filter
3. Audio fabric
4. Memory

2.1.1 Hemi Delta Processor

The HMD is a low power DSP with frame-based processing capabilities, and includes the following features:

- 64-bit instruction memory access (maximum instruction size is 64 bits).
- 64-bit data memory access (maximum register width is 64 bits).
- Main data type: 32-bit float (AFLOAT).
- Main vector register file: 16 vector registers (two 32-bit lanes each).
- Permutation registers to support load/store, permute, and arithmetic instructions.
- Dual issue instruction bundles.
- Vector and scalar instructions.
- Four MACs (real and complex arithmetic support).
- Nonlinear functions: arc tangent, cosine, sine, log, exponential, inverse, inverse square root, and sigmoid (exponential approximation).
- Added acceleration
  - FFT
  - Peak finding
  - DNNs (eight 8-bit x 8-bit fixed-point MACs)
  - TFLu (Tensor flow light for Microcontroller)

2.1.2 Digital Filters

The IA700 digital filters allow the use of Pulse Density Modulation (PDM) audio data. There are four receive decimation filter chains, and two transmit interpolation filter chains. The decimation filters support one-bit PDM input oversampled audio data from digital microphones and codec interfaces. The interpolation filters generate oversampled one-bit PDM output audio data that routes to a speaker or codec.

2.1.3 Audio Fabric

The Audio Fabric is a memory-mapped interface that allows the processor to access data efficiently from the various audio interfaces supported by the chip, such as I^2S/TDM, or PDM. Each audio interface converts input data into a common 32-bit integer format that synchronizes into the processor clock domain from the native audio clock before multiplexing into generic N-channel logical streams of audio data in the Audio Fabric. Similarly, each audio interface can convert 32-bit integer format data into the encoding required for transmission. The audio fabric supports a low-latency path and connects to the wall clock/presentation timer's unit to capture timestamps of audio data.

2.1.5 Memory

The IA700 has 248 kB of RAM, which is divided as following:

- 32 kB dedicated IRAM.
- 32 kB dedicated DRAM.
- 184 kB memory pool, consisting of five 32 kB blocks, one 16 kB block, and one 8 kB block.
- 168 kB of the total 248 kB memory is reserved for custom algorithm use.

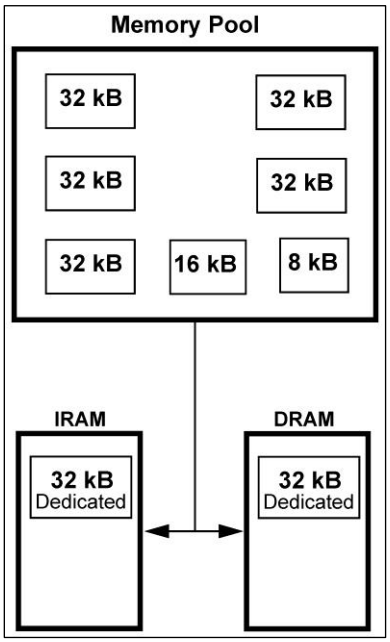


Figure 6 Memory Pool Structure

2.1.6 Audio Interfaces

The IA700 audio processor supports the following audio data transfers:

- Four PDM input channels
- Two PDM output channels
- Master/Slave I2S/TDM

2.1.6.1 *Digital Microphone PDM Input Interface*

The user can configure IA700 to support Pulse Density Modulation (PDM) digital microphone interface to receive audio data from external PDM microphone(s). Depending on the configuration, IA700 can be either a PDM Master or a PDM Slave.

- PDM Master – IA700 generates PDM clock by internal audio PLL.
- PDM Slave – IA700 receives PDM clock by external codec or other source.

The user can configure PDM_CLK signal either as input or as output; it supports up to 4.8 MHz frequencies.

The IA700 can support up to two digital microphones in a stereo configuration.

The dual channel PDM carries encoded data, therefore, the IA700 PDMx_DI input clocks the left channel data at the falling edge of PDM_CLK and the right channel data at the rising edge of PDM_CLK. After driving the data input signal (PDMx_DI) high or low in the appropriate half frame of the PDM_CLK signal, the input device must tristate the signal. In this way, two microphones, one set to the left channel and the other to the right, can drive a single DATA line.

2.1.6.2 *Digital Microphone PDM Output Interface*

The IA700 has a single PDM output signal used to transmit two audio channels. Each clock edge transmits data for one of the two audio channels, as shown in Figure 7. The clock can be set to input (slave) or output (master) in PDM output mode. Table 2 lists the supported frequency ranges, if the user programs frequency ranges as an input. When the clock is set to output, the default output frequency is 3.072 MHz. For more information on flexibility of using PDM clock as an output, see *IA700 API Guide.*

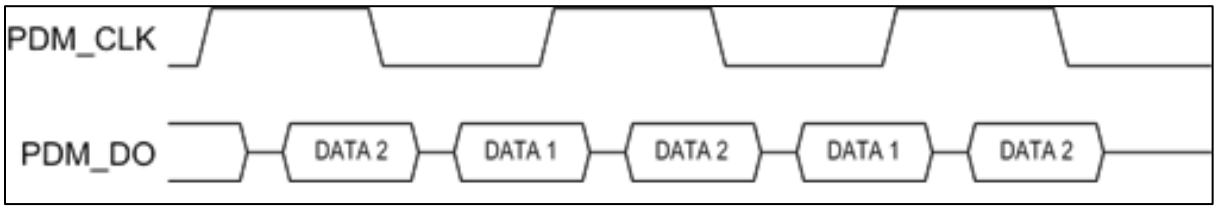


Figure 7 PDM Two-Channel Output Timing

Table 2 Supported PDM Clock Rates

PDM Clock (KHz)	Recommended Max Bandwidth of Audio Signal (KHz)
512	8
768	8
1024	10.66
1536	16
2048	21.33
2400	25
3072	32
4608	48
4800	50

2.1.6.3 *I²S/TDM Digital Audio Port*

When in I²S + I²C or I²S + UART mode, the IA700 can transfer audio data through I²S or TDM protocol with an external host or codec device. (Table 9 and Table 1 lists the pin configuration in these modes.) The user can configure IA700 to operate either in slave or master mode using API commands.

I²S transfers have the following features.

- Bit clock (I2S_CLK) up to 24.576 MHz.
- Sampling clock (I2S_WS) up to 192 KHz.
- There must be exactly two slots, Left (I2S_WS low) and Right (I2S_WS high).
- There must be an equal number of I2S_CLK periods in each half I2S_WS period.
- Support for 8 to 32 audio data bits per slot (channel).

Figure 8 shows an example of I²S mode.

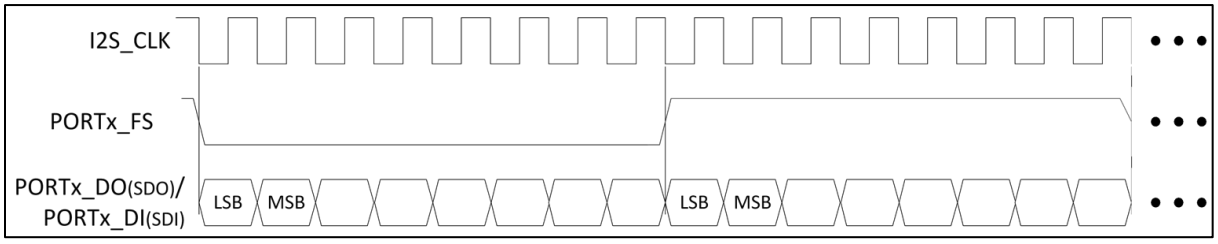


Figure 8 I²S Mode

TDM transfers have the following features:

- Bit clock (I2S_CLK) up to 24.576 MHz.
- Sampling rates of up to 192 KHz.
- Frame Sync pulse (I2S_WS) must be at least one-bit clock wide.
- Support for up to four active slots (channels) out of 32. Slots do not have to be consecutive. In master mode, the master clock generator supports up to 256 clocks per frame, however slave TDM operation supports up to 32 slots with 32 data bits per slot and is not limited by clocks per frame.
- Support for 8 to 32 audio data bits per slot (channel).
- Support for output transmission on either the rising or falling bit clock edge.
- Support for input sampling on either the rising or falling bit clock edge.
- The transmitting and sampling edges must be of opposite polarity.
- Support for both MSB-first and LSB-first transmission modes.

Figure 9 shows an example of TDM mode.

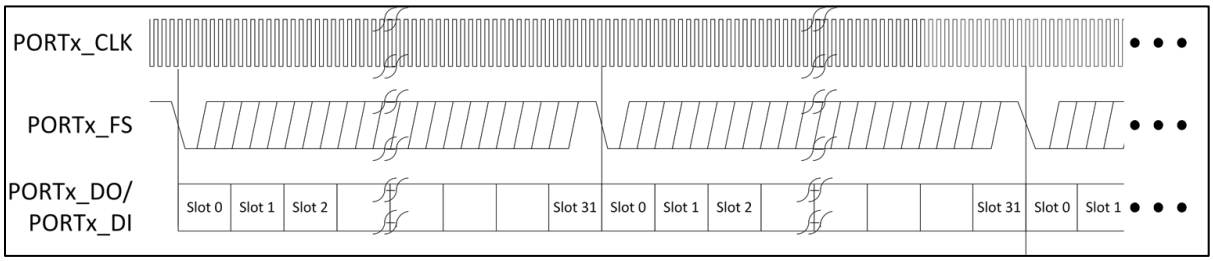


Figure 9 TDM Mode

2.1.7 Host Interfaces

2.1.7.1 *Firmware download, Command and Control*

The IA700 audio processor supports command and control over SPI, UART, and I2C interfaces. It also supports firmware download on all three interfaces selected at boot time by a Host.

Table 3 Supported interface speed

Control Interfaces	Firmware download Interface Speed with Internal Oscillator	Firmware download Interface Speed with external CLK_IN
SPI	4.5 MHz	13 MHz
UART	1.152 Mbps	2.048 Mbps
I2C	1 MHz	1 MHz

2.1.7.2 *SPI*

The IA700 supports a four-wire Serial Peripheral Interface (SPI) protocol with a frequency range of up to 13 MHz. The user can download a firmware image and send API control and data to the IA700 through the SPI slave port.

2.1.7.3 *UART*

The IA700 supports a two-wire UART (UART_TX, UART_RX). The UART is required to download a firmware image onto the IA700, and a UART connection to the host is required for streaming as an alternative to ID tapping. The interface can detect the baud rate automatically up to 115 KHz; it also supports baud rates of 0.4608, 0.9216, 1.000, 1.024, 1.152, 2.000, and 2.048 MHz as configured by the host using the Bootloader UART baud rate change API command or by the firmware after the binary file download.

2.1.7.4 *I²C*

The IA700 supports a Slave I²C bus as the host interface with a 7-bit address range. The I²C address can be set through the data output Latch-On Reset (LOR) configuration pin, as described in Section 4.1. A firmware image is downloaded to the IA700 using the I²C interface.

2.1.7.5 *Debug*

The SPI, UART, and I²C interfaces all support the collection of diagnostic data streams. This requires the ability to collect synchronized input/output streams using any of the interfaces.

Debug is supported either by a virtual connection over ADB to an Android Proxy running on the host processor, or by a direct physical connection to test-points on the system PCB, with no-load resistors connected to the SPI, UART, I2C I/O pins for the IA700.

2.2 Control Subsystem

2.2.1 Boot Control

When the user turns on the VDD, the IA700 goes through a power-up initialization process. During this time, the IA700 does not respond to host requests. The IA700 then enters a control interfaces auto-detect mode to determine which pin configuration to use for operation. For more information on the start-up sequence, see Section 4.2 and for more information on the auto-detect sequence, refer *IA700 API Guide*.

2.2.2 Reset Control

There are two types of Resets:

1. External Hard Reset
2. Soft Reset

2.2.2.1 *External Hard Reset*

The System Reset Input pin (RESET_N) is an active low asynchronous reset input that provides a global reset for the IA700. When reset asserts, the digital output pins are tri-stated, or pulled-up or pulled-down by internal resistors, and the default values for all the internal registers are restored. RESET_N must drive high from the system printed circuit board.

Note: Do not share the RESET_N pin of IA700 with any other reset pin on printed circuit board.

2.2.2.2 *Soft Reset*

The one watchdog timer of the IA700 resets the processor when it expires.

2.2.4 Power Management

Figure 5 shows a color-coded block diagram of the IA700's different power domains. There are two primary power domains: one to supply the core analog signal path circuitry and one to supply the core DSP subsystem. The DSP core subsystem has three subordinate power domains; controlled independently to optimize power in various use cases. This section provides further details around the primary ASIC power domains.

Table 4 Power Supply Pins

Name	Voltage	Max Current	Power Direction	Comment
GND	0 V	25mA	-	
VDD_IO	1.8V	25mA	Input	IO supply
VDD_LDOD/A	1.1V	23mA	Input	Core supply

Where:

- GND is the common ground pin for all IA700.
- VDD_IO supply provides power to all I/Os.
- VDD_LDOD/A supply provides power to the DSP subsystem, including the processor, memory, Audio Fabric, and core logic.

IA700 supports various sleep modes to save power. For more details, refer Section 3.5.

2.3 Clock Subsystem

2.3.1 CLK_IN

The IA700 has an option to receive clock from extern source on CLK_IN pin. The supported frequencies for CLK_IN are 0.768MHz and 1.536MHz.

2.3.2 PLL

The IA700 has an integrated, high-performance Phase Lock Loop (PLL) that provides clocks for the processors, memory, and related circuits as well as oversampling clocks that drive the serial control communications interfaces. Table 11 details the performance of PLL.

2.3.3 Internal Oscillators

The IA700 has an integrated non-calibrated silicon oscillator optimized for accuracy and system flexibility. The host can calibrate this internal oscillator by providing a reference clock with a factor of 43.008MHz and running appropriate commands. After calibration, the internal oscillator output frequency is set to 43.008MHz. This output frequency divides within the IA700 for use by various internal modules, or as a master output clock. For more information on the performance of the oscillator, see Section 6.3.

2.4 Interrupts

The IA700 provides an interrupt request to the host for a keyword detection event through the HOST_IRQ function, as well as a wakeup event from the host through the WAKE function.

Based on the configuration, the HOST_IRQ and WAKE function map to a specific pin. For more information, see Table 9, Table 1, and *IA700 API Guide*.

Chapter 3: Operating Modes

The IA700 can operate in one of the following modes:

- **Bootloader Auto-Detect Mode:** After power up, the IA700 detects the host control interface and waits for firmware download.
- **Software Pass-Through Mode:** The IA700 supports software pass-through mode for PDM-to-PCM/I2S.
- **Hardware Pass-Through Mode:** The IA700 supports hardware pass-through PDM-to-PDM.
- **Retention Sleep Mode:** The IA700 is in low power mode retaining memory.

3.1 Bootloader Mode (SBL)

Upon system power-up, or after deep-sleep mode, the IA700 is in Bootloader Mode and waits for either an API command to determine the host control interface, or a PDM clock to enter HW Bypass Mode. Once the control interface is determined, download firmware and configure IA700 to operate in one of the other modes listed. For more information on auto-detecting the control interface, firmware download, and mode switching, refer *IA700 API Guide*.

3.2 OpenDSP

248 KB of total on-chip RAM enables third-party algorithms, with dynamic audio filtering and keyword detection as examples. Knowles provides a Software Development Kit (SDK) to enable third-party developers to create DSP algorithms on the IA700 Audio Processor platform.

Contact Knowles to obtain access to the SDK and associated Developer's Guide.

3.3 Software Pass-Through

Host can configure the IA700 to run in software pass-through mode. In this mode, PDM0 is an input port and PCM/I2S is an output port. The Software Pass-Through mode supports only after firmware download.

3.4 Hardware Pass-Through

The Hardware Pass-Through mode allows the host to put the IA700 into a low power digital audio pass-through mode to bypass processing. In this mode, the IA700 reads data from external microphone connected to PDM0 and sends it to the Host on PDMO0 port.

3.5 Retention Sleep/Use Case Sleep Mode

IA700 can enter into a retention sleep mode after the firmware download. The chip enters into normal sleep mode retaining the memory content. A wakeup signal from retention sleep mode is required to bring the chip into firmware mode. A firmware download is not required after waking up from retention sleep mode. Exiting retention sleep mode restarts any internal hardware blocks that were off due to the sleep command.

Similar to retention sleep mode, IA700 can enter into use-case sleep mode after sending appropriate sleep command depends on the use-case.

Chapter 4: Design Considerations

4.1 Latch-On Reset Configuration Pins

4.1.1 Boot clock selection

The IA700 has a Latch-On Reset (LOR) P1 pin to select the boot time clock source. The pin is in latched state when the power is on and stable. An internal pull-down resistor pulls this pin low (0) when not connected. To set this pin to the logical value of 1, connect the pin to the same power supply that powers the IA700 with an external 10 kΩ pull-up resistor.

Table 5 Latch on reset configuration for boot clock

LOR_1 (P1 pin)	Description
0	Boot from CLK_IN
1	Boot from internal oscillator

4.1.2 I2C Address Pins

The IA700 contains two Latch-On Reset (LOR) address pins (P2 and P3 pins) that set the I^2C slave address when in I^2C mode. The address pins are in latched state when the power is on and stable. An internal pull-down resistor pulls the address pins low (0) when not connected. To set the address pin to a logical value of 1, connect the LOR pin to the same power supply that powers the IA700 with an external 10 kΩ pull-up resistor.

Table 6 shows the configuration of the address pins and the resulting I^2C address.

Table 6 Latch On Reset Configuration for I^2C Address

ADDR1 (P2 pin)	ADDR2 (P3 pin)	Description
0	0	7 bit, address 0x3E (default)
0	1	7 bit, address 0x38
1	0	7 bit, address 0x3F
1	1	7 bit, address 0x39

4.2 Start-Up Sequencing

Figure 10 shows a complete start-up sequence, including system power and the host bus.

After LOR, the IA700 wakes up in the Auto-detect state, where it determines the control interface and awaits command communication or firmware download from the host.

Note: The host interface pins must be floating or driven to ground during VDD power up so that they are never exceed VDD+0.3 V.

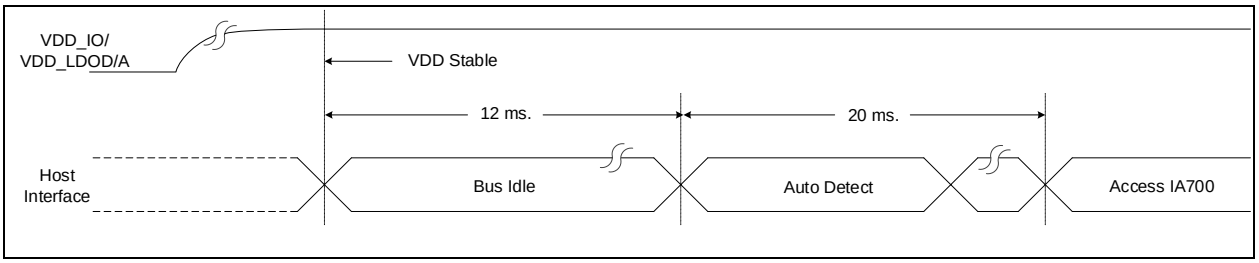


Figure 10 Start-up Sequence

The host must follow a defined sequence to download program code into the IA700. The program code download sequences over the various interfaces are described in detail in the *IA700 API Guide* describes

4.3 Sleep and Wake-up Sequence

The IA700 can be set to an ultra-low-power sleep state to minimize power consumption. During sleep, the host can continue to access other devices connected to the host interface buses.

Figure 11, Figure 12, and **Error! Reference source not found.** provide a general overview of the sleep and wake-up process and their timings. The *IA700 API Guide* provides a detailed description of the sleep and wake-up sequences.

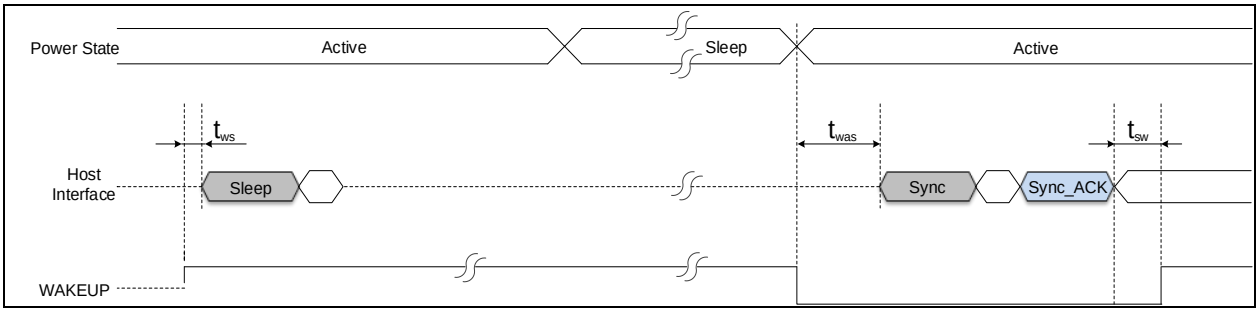


Figure 11 Sleep and Wake-Up Sequence for Waking Up the IA700 Using the WAKEUP Input

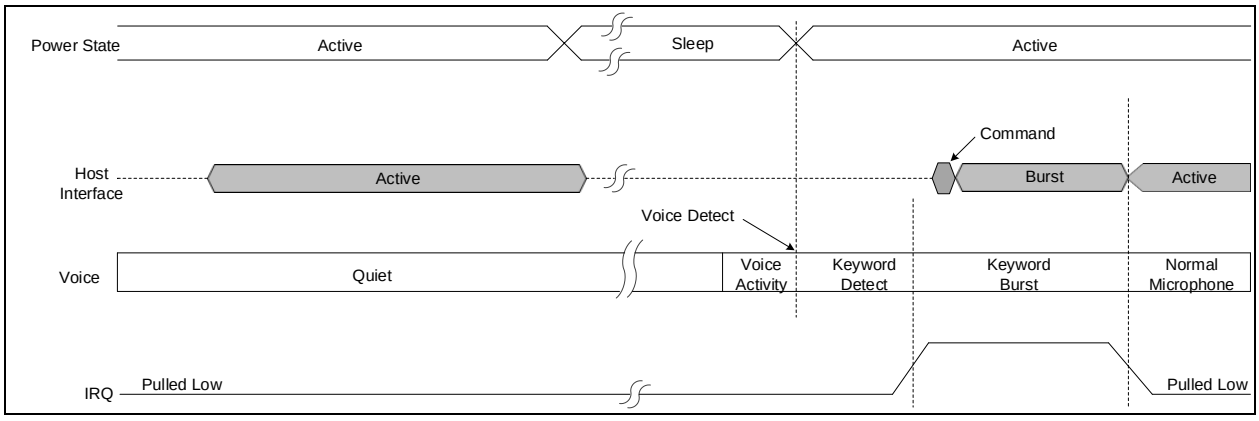


Figure 12 Sleep and Wake-up Sequence for Voice Wake mode with external AAD enabled microphone

Table 7 Sleep and Wake-up Sequence Timings

Parameter	Symbol	Min	Typical	Max	Units
Time from WAKEUP deasserted to SLEEP command write	t_{ws}	30	-	-	ms
Time from WAKEUP asserted to SYNC command write	t_{was}	30	-	-	ms
Time from SYNC _ACK read to WAKEUP deasserted	t_{sw}	0	-	-	ms

4.4 State Diagram

Figure 13 shows the IA700 state diagram.

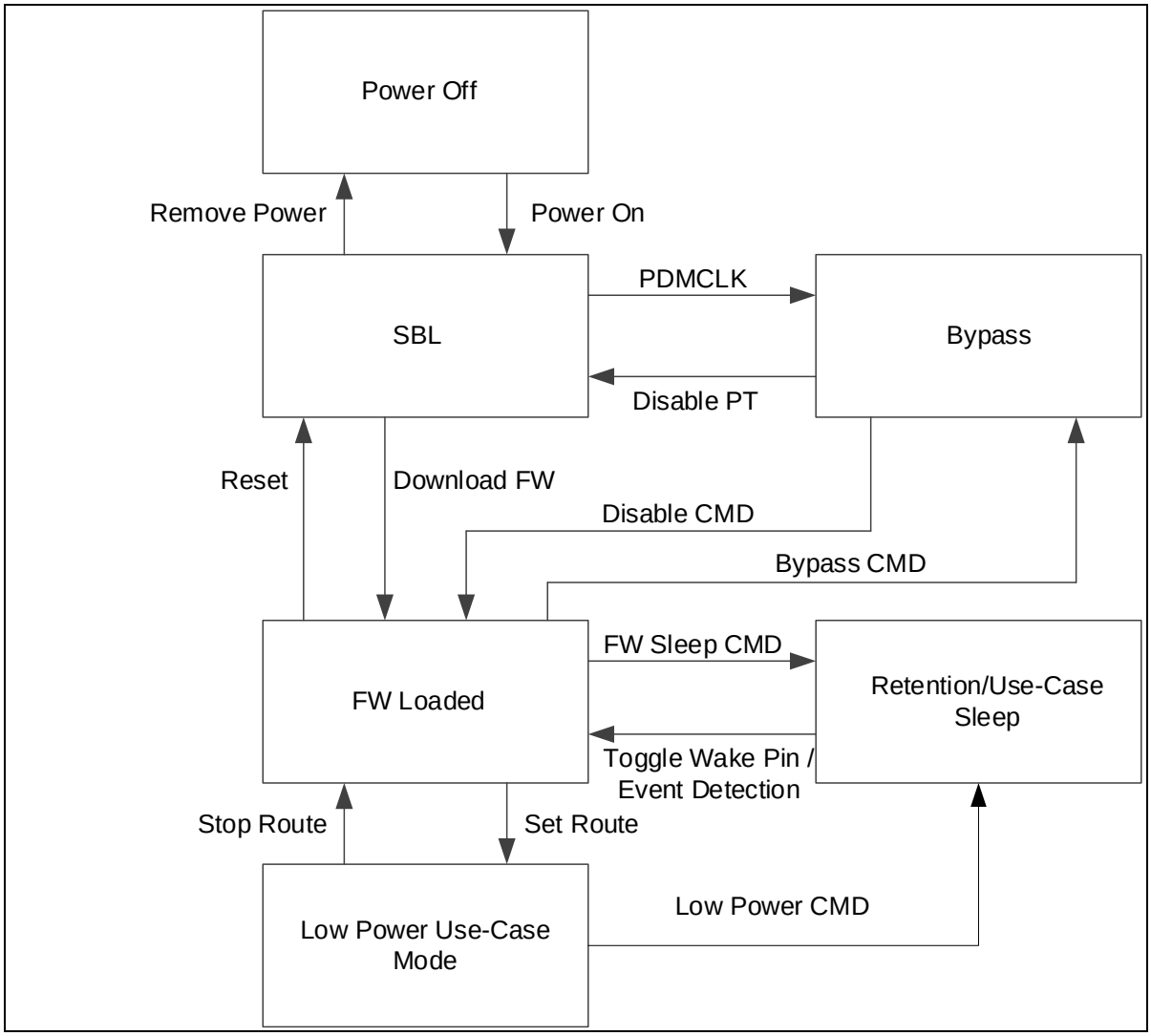


Figure 13 IA700 State Diagram

Chapter 5: Pin Descriptions

5.1 Pinout Diagram

Figure 14 shows the pinouts for the IA700CQ QFN24 package.

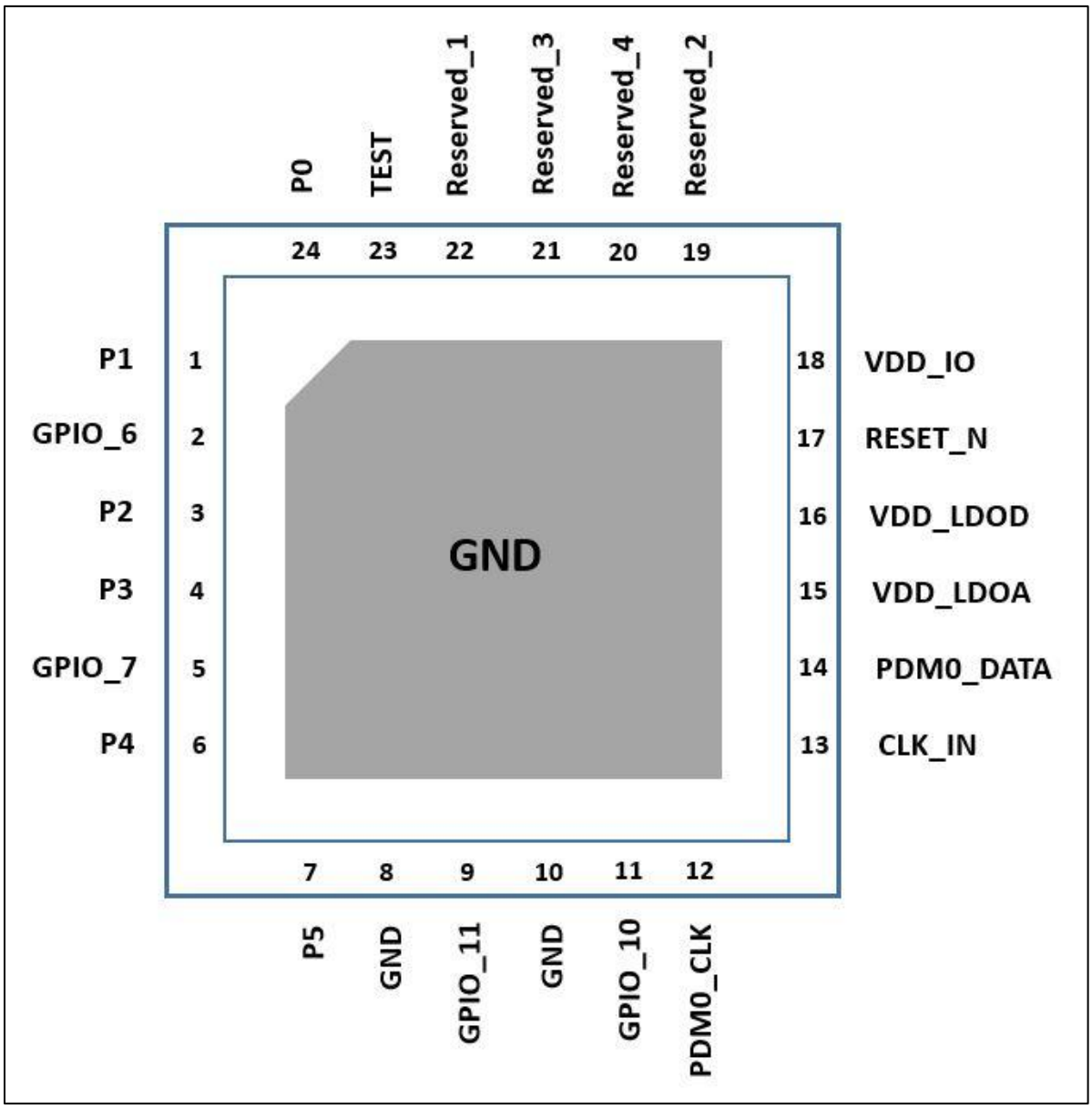


Figure 14 IA700CQ QFN24 Pin Assignments (Top View)

5.3 Pinout Table

Table 8 shows a list of the IA700 pins and the signals associated with them. In active mode, the firmware sets the pin state depending on the mode. Firmware can configure a pin to be an input or an output, and enables internal pull-ups or pull-downs if they are available.

Table 8 Pin Descriptions

Pin#	Name	Type	Description
1	P1	Digital I/O	P1 I/O
2	GPIO_6	Digital I/O	General purpose I/O
3	P2	Digital I/O	P2 I/O
4	P3	Digital I/O	P3 I/O
5	GPIO_7	Digital I/O	General purpose I/O
6	P4	Digital I/O	P4 I/O
7	P5	Digital I/O	P5 I/O
8	GND	Power	Ground
9	GPIO_11	Digital I/O	General purpose I/O
10	GND	Power	Ground
11	GPIO_10	Digital I/O	General purpose I/O
12	PDM0_CLK	Digital I/O	PDM microphone clock
13	CLK_IN	Digital I/O	Clock input
14	PDM0_DATA	Digital I/O	PDM microphone data
15	VDD_LDOA	Power	Power supply for core
16	VDD_LDOD	Power	Power supply for core
17	RESET_N	Input	Reset, Active Low
18	VDD_IO	Power	Power supply for IO
19	RESERVED_2	Not Applicable	Reserved pin – No connect
20	RESERVED_4	Not Applicable	Reserved pin – No connect
21	RESERVED_3	Not Applicable	Reserved pin – No connect
22	RESERVED_1	Not Applicable	Reserved pin – No connect
23	TEST	Not Applicable	Test pin. Must connect it with Ground.
24	P0	Digital I/O	P0 I/O
25	GND	Power	Ground paddle (TAB)

Table 9 Pin Configuration Per Boot Mode

Mode	P0	P1	P2	P3	P4	P5
PDM + I^2C	PDM_CLK	PDM_SDO	I2C_ADDR1	I2C_ADDR2	I2C_SCLK	I2C_SDA
PDM + UART	PDM_CLK	PDM_SDO	NA	IRQ	UART_RX	UART_TX
PDM + SPI	PDM_CLK	PDM_SDO	SPI_SCLK	SPI_MISO	SPI_SS	SPI_MOSI
I^2S + I^2C	I2S_WS	I2S_CLK	I2S_SDI I2C_ADDR1	I2S_SDO I2C_ADDR2	I2C_SCLK	I2C_SDA
I^2S + UART	I2S_WS	I2S_CLK	I2S_SDI	I2S_SDO	UART_RX	UART_TX

Chapter 6: Electrical Characteristics

6.1 General Electrical Characteristics

Table 10 Electrical Characteristics

Test conditions: VDD_IO = 1.8V at T_A =25° C, unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Units
Digital Input High-Level Voltage	V_{IH}	0.65 * VDD_IO			V
Digital Input Low-Level Voltage	V_{IL}	-0.2		0.35 * VDD_IO	V
Digital Output High-Level Voltage	V_{OH}	0.65 * VDD_IO			V
Digital Output Low-Level Voltage	V_{OL}			0.35 * VDD_IO	V
Programmable Digital Input Internal Pull-Down Resistor	R_{PD}	35	61	114	kΩ
Programmable Digital Input Internal Pull-Up Resistor	R_{PU}	39	71	138	kΩ
I/O drive strength		2		12	mA
Capacitance To Ground of I/O Pins	C	9		18	pF

Note:

1. The maximum output current source or sink drive by any I/O pin is programmable in four steps. The default is 4 mA nominal. For more information and settings, refer *IA700 API Guide*.
2. External I/O loading and drive strength have a direct effect on voltage V_{IH} and V_{IL} transition times. For timing critical signals, adjust the values of any external R and C components connected to the I/O pins based on the application.

6.2 PLL Characteristics

Table 11 lists the PLL operation parameters. The PLL has two frequency ranges of operation, set through the software API. The Phase-Frequency Detector (PFD) on the PLL receives a divided-down version of the reference clock.

Table 11 PLL Characteristics

Test conditions: VDD = 1.8V at T_A =25° C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reference Frequency	f_{PLL_IN}		0.768	-	24.576	MHz
PFD Frequency	f_{PLL_PFD}	Low Range	0.768	-	35[1]	MHz
		High Range	0.768	-	75[2]	MHz
VCO Frequency	f_{PLL_VCO}	Low Range	28	-	140	MHz
		High Range	120	-	600	MHz
Output Frequency	f_{PLL_OUT}	-	0.11	-	98.304	MHz
Lock Time	t_{PLL_LOCK}	-		500	1000	PFD cycles
Feedback Divider	n_{PLL_FBDIV}	-	4	-	781	integer
Loop Bandwidth	f_{PLL_BW}	-		fPLL_PFD/ 25		MHz
Period Jitter (random)[3]	$t_{PLL\_JIT\_RND}$	-	1.73	-	239.38	pS (RMS)
Period Jitter Power Supply Noise Sensitivity	$t_{PLL\_JIT\_PS}$	-		1.5	-	pS/mV
Period Jitter from reference spur	$t_{PLL\_JIT\_REF}$	-		1%	-	Output clock cycle
Integrated Long-Term Jitter[4]	tPLL_JIT_LT	-	14.37	-	657.38	pS (RMS)

[1]For Low Range Maximum PFD Frequency $f_{PLL\_PFD} = f_{PLL\_VCO} \div 4$

[2]For High Range Maximum PFD Frequency $f_{PLL\_PFD} = f_{PLL\_VCO} \div 8$

[3]Formula to calculate Period Jitter (random) $t_{PLL\_JIT\_RND}$ = 0.7 pS × sqrt (600 MHz ÷ f_{PLL_VCO}) × sqrt (600 MHz ÷ f_{PLL_OUT})

[4]Formula to calculate Integrated Long-Term Jitter $t_{PLL\_JIT\_LT}$ = 100 pS × sqrt (6 MHz ÷ f_{PLL_PFD}) × sqrt (128 MHz ÷ f_{PLL_VCO})

6.3 Oscillator Characteristics

The non-calibrated on-chip silicon oscillator has the characteristics listed in Table 12. The following frequency ranges are after oscillator calibration. There are two operational ranges, set by an internal register through the software API.

Table 12 Oscillator Characteristics

Test conditions: VDD = 1.8V at TA =25 o C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Output Frequency	f_{OSC_OUT}	Low Range	-	43.008	-	MHz
		High Range	-	172.032	-	MHz
Output Frequency Temperature Dependence	Δ_{OSC_T}	-10°C to 80°C	-	340	535	ppm/°C
Period Jitter (random)	$t_{OSC\_JIT\_RND}$	Low Range	-	-	44	pS (RMS)
		High Range	-	-	22	
Period Jitter Power Supply Noise Sensitivity	$t_{OSC\_JIT\_PS}$	Low Range	-	0.9	2.2	pS/mV
		High Range				

6.4 Audio Port Interface Characteristics

6.4.1 I²S/TDM Interface Slave Timing

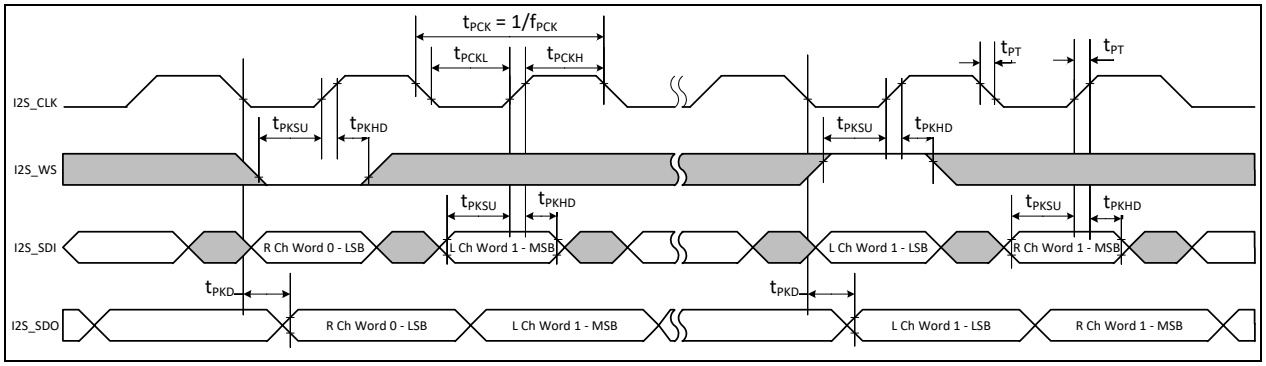


Figure 15 I²S / TDM Interface Slave Timing

In Slave Mode, I2S_CLK and I2S_WS are inputs.

Table 13 I²S / TDM Slave Timing

Test Conditions: VDD = 1.8V, 10pF Load, at T_A =25° C, unless otherwise specified. Measurement levels on waveforms are V_{IH} and V_{IL}. [1]

Parameter	Symbol	Min	Typical	Max	Units
I2S_CLK Clock Frequency	f_{PCK}	-	-	24.576	MHz
I2S_CLK Clock Cycle Time	t_{PCK}	-	$1/f_{PCK}$	-	s
I2S_CLK Clock High Pulse Width	t_{PCKH}	35	-	-	% t_{PCK}
I2S_CLK Clock Low Pulse Width	t_{PCKL}	35	-	-	% t_{PCK}
I²S input transition time	t_{PT}	-	10	-	ns
I2S_SDI and I2S_WS Input Setup Time to CLK ↑ [2]	t_{PKSU}	25	-	-	ns
I2S_SDI and I2S_WS Input Hold Time from CLK ↑ [2]	t_{PKHD}	5.1	-	-	ns
I2S_SDO Data Output Delay from CLK ↓ [3]	t_{PKD}	0	-	15	ns

[1]The design ensures the timing parameters and not by the final test.
[2]The I2S_WS and I2S_SDI inputs sampled at the rising edge of the I2S_CLK.
[3]The I2S_SDO outputs are set to drive at the falling edge of the I2S_CLK.

6.4.3 I²S/TDM Interface Master Timing

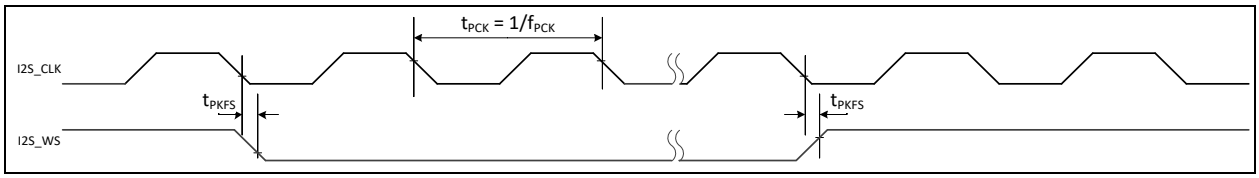


Figure 16 I²S/TDM Interface Master Timing

In Master Mode, I2S_CLK and I2S_WS are outputs, but I2S_SDI and I2S_SDO timing with respect to I2S_CLK are identical to that in Slave mode.

Table 14 I²S/TDM Master Timing

Test Conditions: VDD = 1.8V, 10pF Load, at T_A =25° C, unless otherwise specified. Measurement levels on waveforms are V_{IH} and V_{IL}.[1]

Parameter	Symbol	Min	Typical	Max	Units
I2S_WS Output Delay from CLK ↓ [2]	t_{PKFS}	0	-	25%	t_{PCK}

[1]The design ensures the timing parameters and not by the final test.
[2]The I2S_WS outputs are set to drive at the falling edge of the I2S_CLK. Delay from CLK ↓ to I2S_CLK is determined by an integer number of periods of an internal oversampling clock used to generate both I2S_CLK and I2S_WS.

6.4.4 Audio Port PDM Interface Characteristics

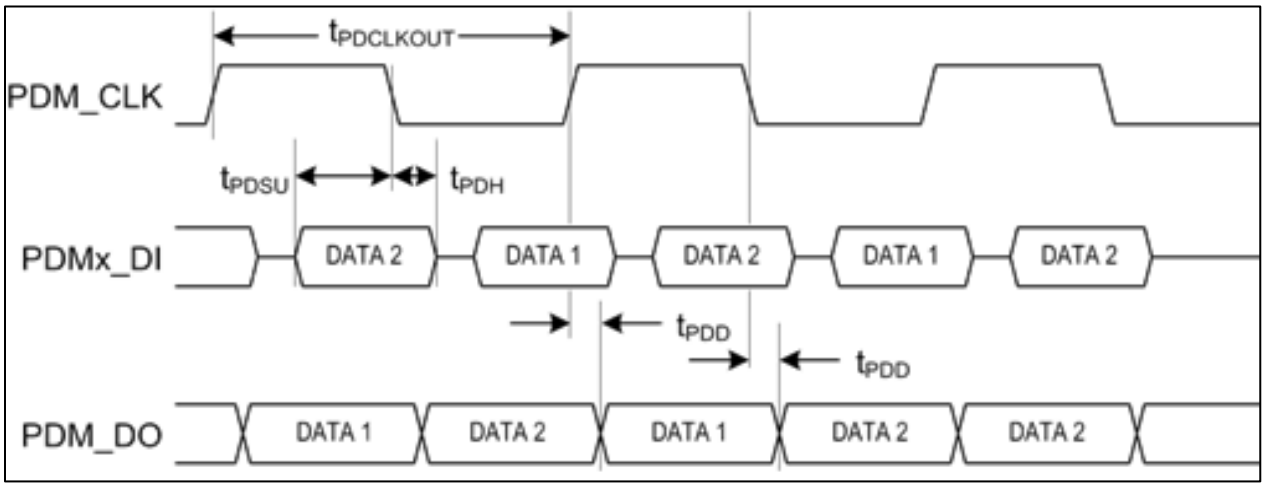


Figure 17 PDM Interface Timing

Table 15 PDM Timing[1]

Test Conditions: VDD = 1.8V, 10pF Load, at T_A =25° C, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Units
PDM_CLK Output Frequency, Operating	$f_{PDCLKOUT}$	0.512	3.072	4.800	MHz
PDM_CLK Output Frequency, Low-power Voice Wake Mode	-	0.512	0.768 Nominal	-	MHz
PDM Data Input Setup Time to Clock Edge	t_{PDSU}	25	-	-	ns
PDM Data Input Hold Time after Clock Edge	t_{PDH}	3	-	-	ns
PDM Data Delay from PDM_CLK Edge[2]	t_{PDD}	6	-	-	ns

[1]The design ensures the timing parameters and not by the final test.
[2]The edge of the clock on which data is output is programmable.

6.5 I²C Slave Interface Characteristics

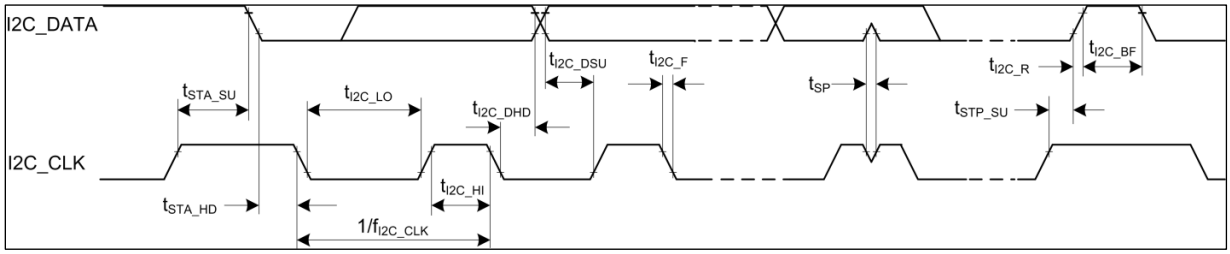


Figure 18 I²C Slave Interface Timing

Table 16 I²C Slave Timing

Test Conditions: VDD = 1.8V, Output Load = 20pF, unless otherwise specified.

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode+		Units
		Min	Max	Min	Max	Min	Max	
I²C Clock Frequency	f_{I2C_CLK}	0	100	0	400	0	1000	KHz
I²C Clock High Period	t_{I2C_HI}	4.0	-	0.6	-	0.26	-	µs
I²C Clock Low Period	t_{I2C_LO}	4.7	-	1.3	-	0.5	-	µs
Start Condition Setup Time	t_{STA_SU}	4.7	-	0.6	-	0.26	-	µs
Start Condition Hold Time	t_{STA_HD}	4.0	-	0.6	-	0.26	-	µs
Stop Condition Setup Time	t_{STP_SU}	4.0	-	0.6	-	0.26	-	µs
Bus Free Time between Stop and Start Conditions	t_{I2C_BF}	4.7	-	1.3	-	0.5	-	µs
I²C Clock and Data Rise Time	t_{I2C_R}	-	1000	20	300	-	120	ns
I²C Clock and Data Fall Time	t_{I2C_F}	-	300	-	300	-	120	ns
I²C Data Setup Time	t_{I2C_DSU}	250	-	100	-	50	-	ns
I²C Data Hold Time	t_{I2C_DHD}	0	202	0	202	0	-	ns
Spike Suppression Period	t_{SP}	0	0	0	50	0	50	ns

6.6 SPI Interface Specifications

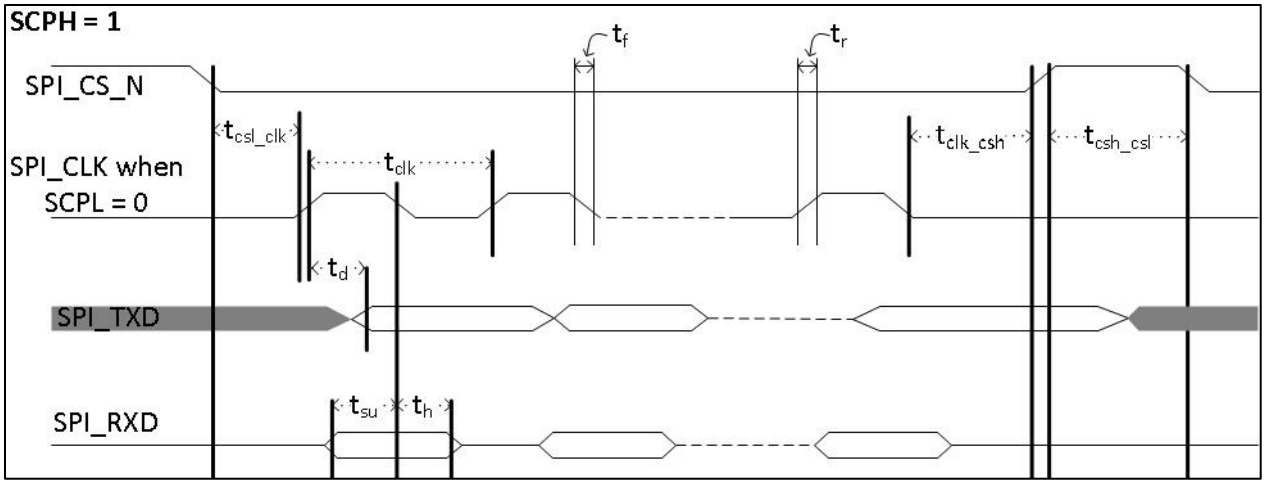


Figure 19 SPI Interface Timing

In bootloader auto-detect mode, the SPI clock phase is set to SCPH = 1, and the clock polarity is set to SCPL = 0 on reset. SPI is 32-bit interface. To enable the SPI interface in bootloader mode, refer IA700 API Guide.

Table 17 SPI Timing SCPH = 1

Test Conditions: VDD = 1.8V, >=6x oversampling, 10pF Load, at T_A = 25° C, unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Units
SPI sample clock frequency	f_{samp}	-	-	43	MHz[1]
SPI sample clock period	T_{samp}	23.25	-	-	ns
SPI clock frequency	f_{clk}	-	-	13	MHz
SPI clock period	t_{clk}	76.92	-	-	ns
Chip select assert to clock edge	t_{csl_clk}	1	-	-	t_{clk}
Clock edge to chip select de-assert	t_{clk_csh}	1	-	-	t_{clk}
Chip select de-assert to chip select assert	t_{csh_csl}	1	-	-	t_{clk}
Tx data valid from clock edge	t_d	-	-	64.125	ns
Rx data setup time	t_{su}	0.5	-	-	t_{samp}
Rx data hold time	t_h	1.5	-	-	t_{samp}
SPI clock rise time	t_r	-	-	10%	t_{clk}
SPI clock fall time	t_f	-	-	10%	t_{clk}

[1]The maximum frequency is available only in certain modes. The internal oversampling clock is set to a minimum of 2.5 times the SPI_CLK frequency by the software API. The values in this table vary, as the internal sampling clock changes. The higher the internal sampling clock frequency, the higher the power consumption.

Chapter 7: PCB Design and Layout Guidelines

7.1 Power Planes

Use low impedance power planes with decoupling capacitors for the design of system power supply.

Place ceramic SMT bypass capacitors (1 µF) next to the IA700 VDD_LDOD and VDD_LDOA power input pins, as well as IA700 VDD_IO pin. The IA700 VDD_LDOD and VDD_LDOA pins can be shorted and can have a 1 µF decoupling capacitor connected to it.

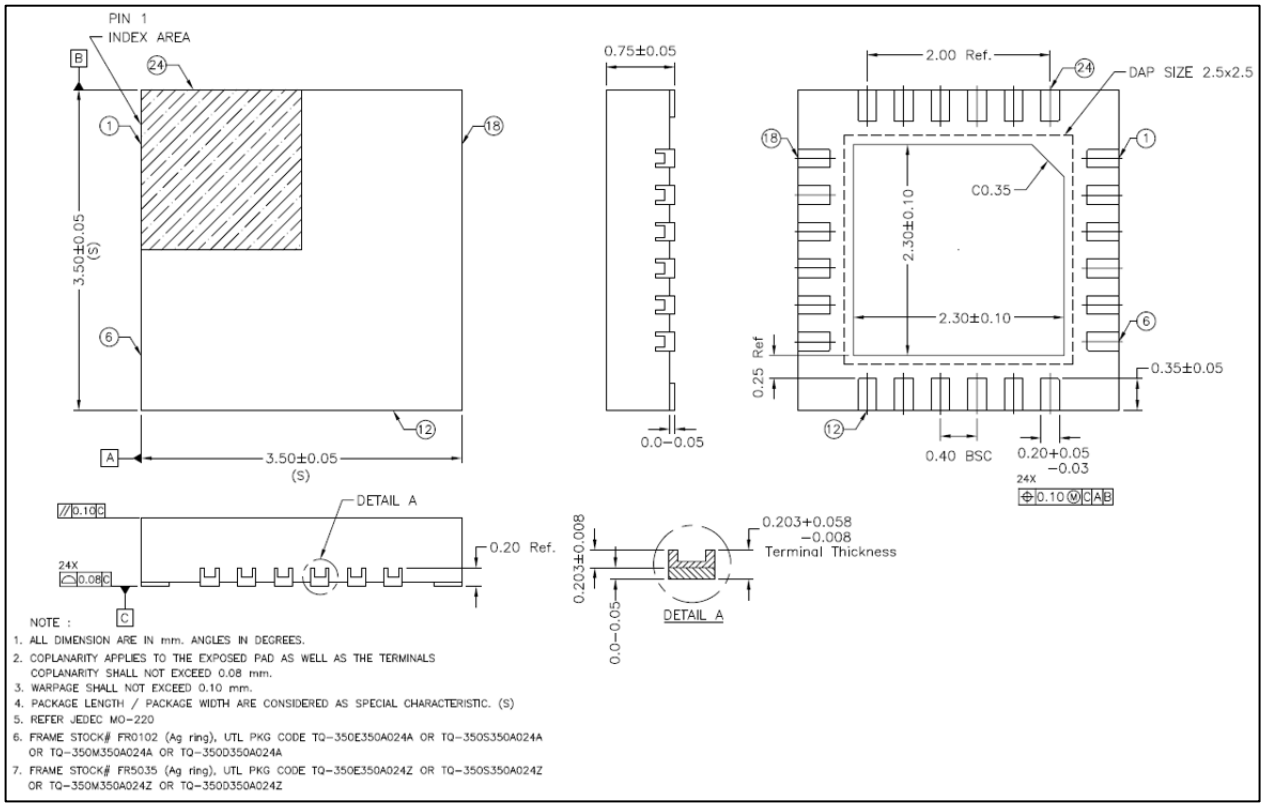
Additional decoupling capacitors (0.1 µF) may be necessary to reduce noise on the power pin. Keep the routing traces for the decoupling capacitors as short as possible. A long trace has an antenna effect that can introduce additional noise into the power supply, which requires additional filtering.

7.2 Digital Signal Routing

Follow good design practices in PCB layout by keeping the digital signal traces as short as possible and away from analog and RF signals.

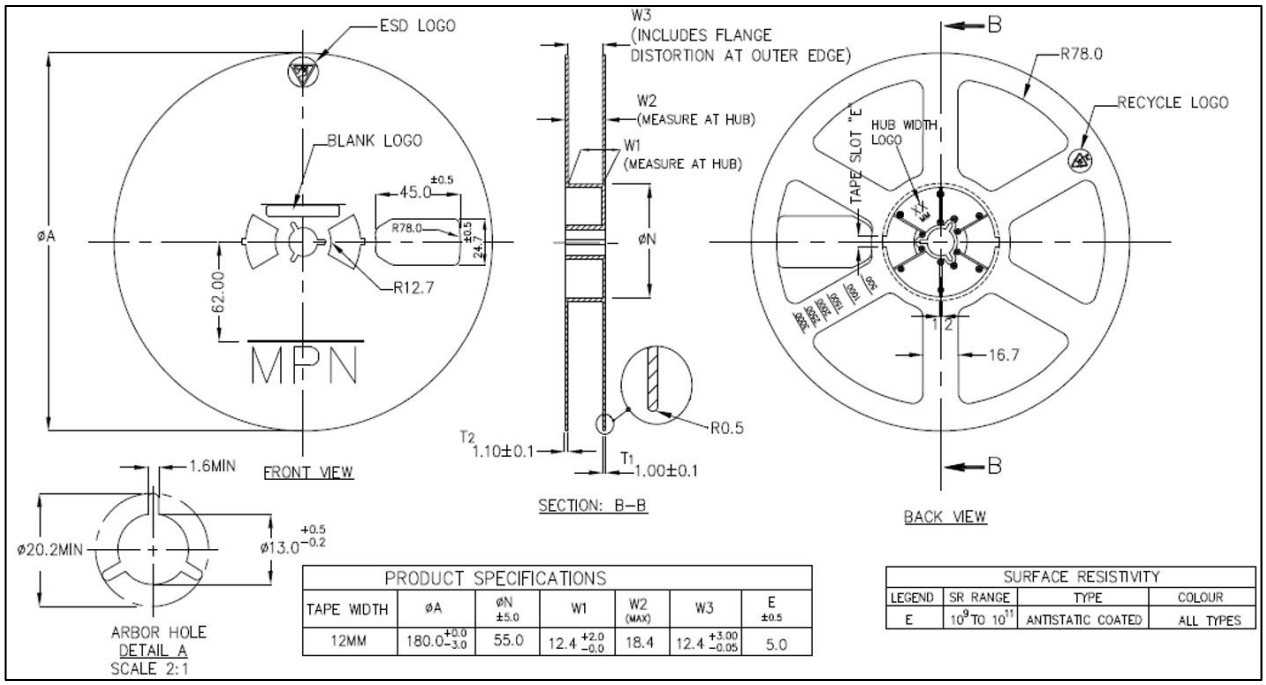
Chapter 8: Mechanical Specifications

8.1 IA700CQ QFN24 Package Dimension



Chapter 9: Packaging and Marking Details

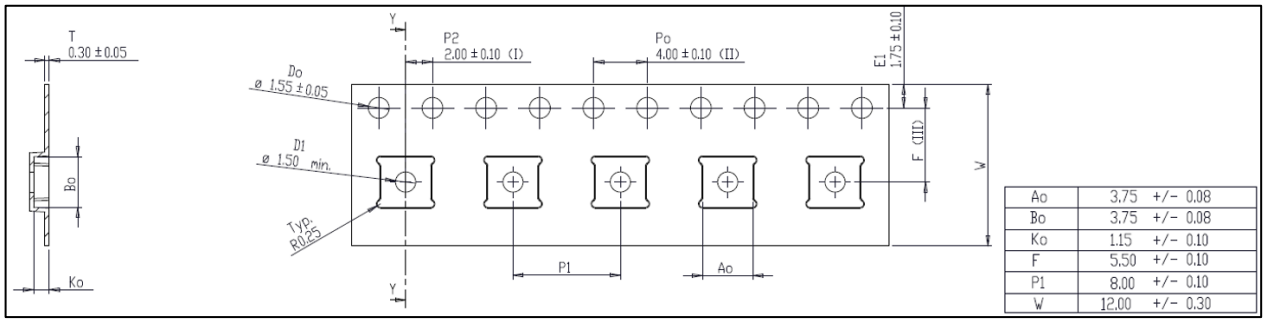
9.1 **Reel**



PRODUCT SPECIFICATIONS						
TAPE WIDTH	ØA	ØN ±5.0	W1	W2 (MAX)	W3	E ±0.5
12MM	180.0 +0.0 −3.0	55.0	12.4 +2.0 −0.0	18.4	12.4 +3.00 −0.05	5.0

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
E	10^9 TO 10^{11}	ANTISTATIC COATED	ALL TYPES

9.2 **Tape**

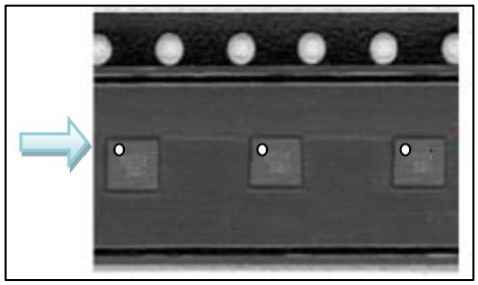


Ao	3.75	+/− 0.08
Bo	3.75	+/− 0.08
Ko	1.15	+/− 0.10
F	5.50	+/− 0.10
P1	8.00	+/− 0.10
W	12.00	+/− 0.30

Note: Dimensions are in millimeters unless otherwise specified.

Table 18 Model and Part Numbers

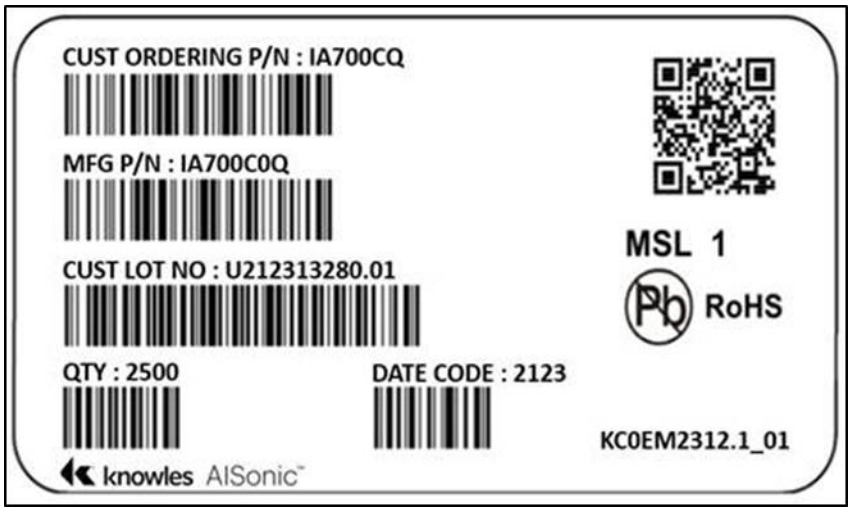
Model Number	Reel Diameter	Quantity Per Reel
IA700CQ	13”	2500



Unit orientation in carrier tape: Pin 1 top left

Product Customer Lot Number – U193545010.00		
Digit	**Description**	**Actual**
1	Vendor ID	U for UTAC
2-3	Year – YY	2 digit
4-5	Workweek – WW	2 digit
6-9	Fab lot ID	1st two and last two digit of the fab lot ID
10	Sequence #	One hexadecimal character (OSAT assigned running character: 0,1,2…9,A,B..X,Y,Z,0,1,…)
11		Dot
12-13	Split/Child Indicator	2 digit
Example: Year 2019, Workweek 35, Fab lot ID UKNT45001.00		

9.3 Packing Details



Customer Ordering PN: IA700CQ
Knowles Manufacturing PN: IA700C0Q

Label Content:

- CUST ORDERING P/N = Knowles Customer Part Number
- MFG P/N = Knowles Manufacturing Part Number
- CUST LOT NO = Lot Number from supplier
- QTY = Unit quantity per reel
- DATE CODE = Manufacturing Date Code in YYWW format
- MSL = Moisture Sensitive Level
- Lead Free and RoHS symbols
- UTL label running number (unique number per label)

Barcode type:

- 1D – code 128 or 3 of 9
- 2D - QR code

2D barcode content:

- P+ (CUST ORDERING P/N) Q+(QTY)T+ (CUST LOT NO) S+ (RUNNING NUMBER) D+ (DATE CODE)
- 2D barcode content example based on data on the label sample:
- P+IA700CQQ+2500T+U212313280.01S+KC0EM2312.1_01D+2123

Note: All barcodes in label sample are for illustration only.

Chapter 10: Recommended Reflow Profile

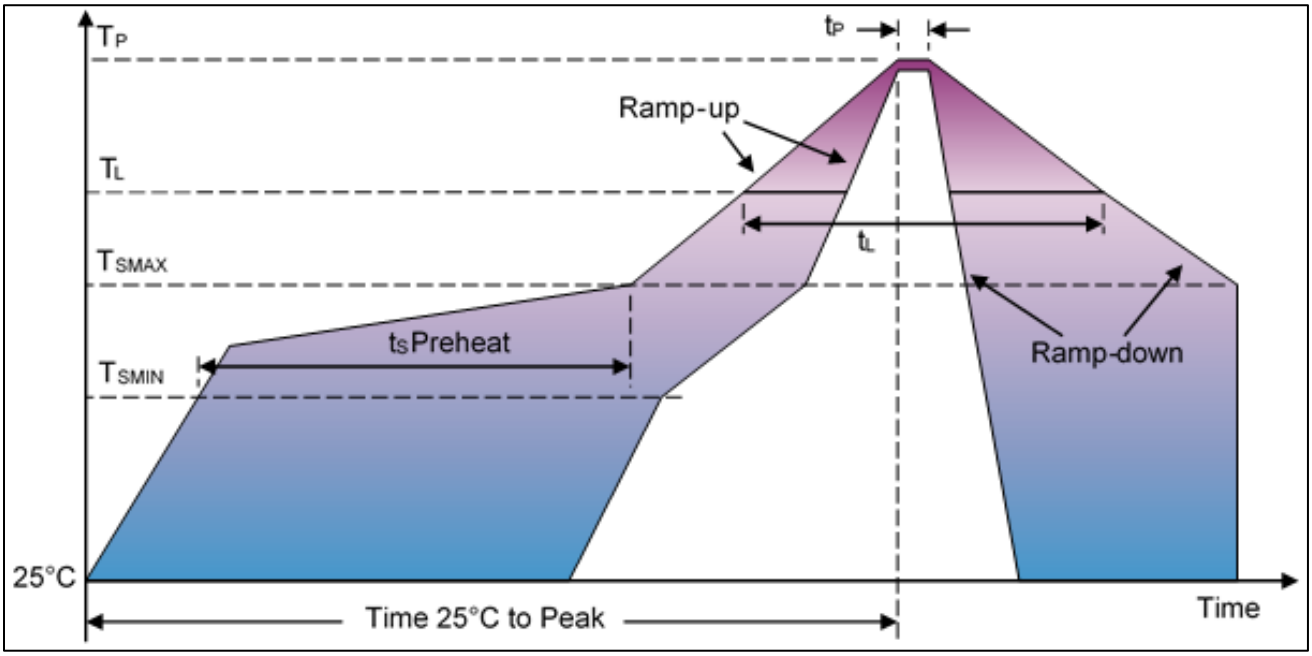


Figure 20 Recommended Reflow Profile

Table 19 Profile Specifications

Profile Feature	Pb-Free
Average Ramp-up rate (TSMAX to TP)	3°C/second max
Preheat - Temperature Min (T_{SMIN}) - Temperature Max (T_{SMAX}) - Time (T_{SMIN} to T_{SMAX}) (t_S)	 150°C 200°C 60-180 seconds
Time maintained above: - Temperature (TL) - Time (tL)	 217°C 60-150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down rate (T_P to T_{SMAX})	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

Note: Based on IPC/JDEC J-STD-020 Revision C.
All temperatures refer to topside of the package, measured on the package body surface.

10.1 Additional Notes

1. MSL (moisture sensitivity level) Class 1.
2. Recommending maximum of three reflow cycles.

Revision History

Revision	Description	Date
1.0	Initial Release	25-08-2021

Knowles Corporation
1151 Maplewood Drive
Itasca, Illinois 60143

Phone: (630) 250-5100
Fax: (630) 250-0575
info@knowles.com

Model/Reference Number:
AUD-ESP-00517, Rev v1.0