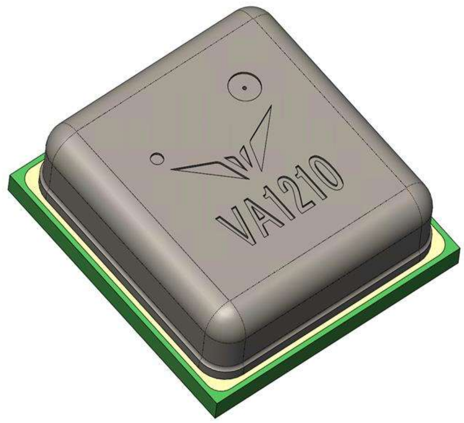
GENERAL DESCRIPTION

The VA1210 is a high performance, low noise differential analog MEMS voice accelerometer (a.k.a bone sensor). It features Vesper's Adaptive ZeroPower Sensing™ that dramatically extends the battery life of always-on systems. Adaptive ZeroPower Sensing™ constantly monitors the background acceleration level to activate the system when pre-configured acceleration threshold (such as the user's voice) is detected. The entire signal chain of the ZeroPower Sensing™ system is in hibernate mode while sensing for voice. When voice is detected, the accelerometer can be switched to a Normal Mode where it will operate as any standard analog low noise accelerometer. The ZeroPower Sensing signal chain can also be used for hardware-based Voice Activity Detect.

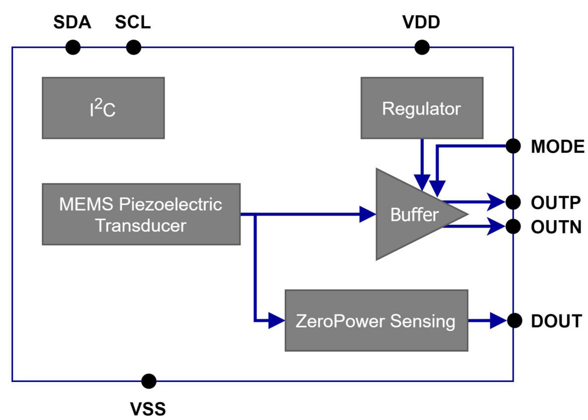
The VA1210 has an ultra-small 2.9 x 2.76 x 0.9mm package. The accelerometer is solder reflow compatible with no sensitivity degradation. Vesper's Piezoelectric MEMS construction also enables operation in environmentally harsh surroundings due to immunity to dust and moisture ingress protection. It is ideal for applications requiring high quality voice call in battery powered consumer devices.



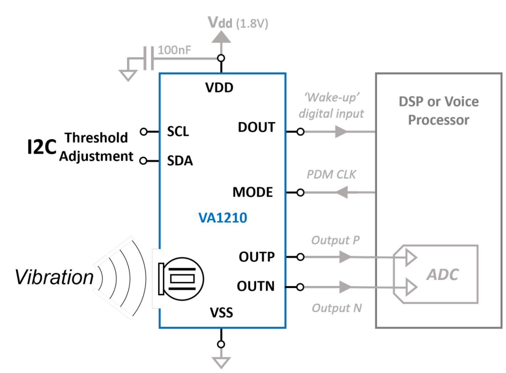
FEATURES

- Adaptive ZeroPower Sensing™ (ZPS) Voice Accelerometer
- Built-in ultra-low power VAD (voice activity detection)
- Dust resistant and moisture resistant
- Differential Analog Output
- Mode selection using Mode pin
- Adaptive ZPL mode configurable through I²C
- Ultra-fast startup in all modes (<200 µSec)
- Soft-start function to prevent pop & click noises
- BIST (Built-In-Self-Test) function
- RFI and EMI robust
- Wide Temperature Range: -40C to 85C
- Small Footprint 2.9 x 2.76mm LGA package footprint

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



APPLICATIONS

- Truly Wireless Stereo (TWS) Earbuds and Headphones
- Background Noise and Wind Noise Suppression
- Hearables
- Wearables
- AutoMute
- Voice Activity Detection and Tap Detection
- Surface Microphone

ORDERING INFORMATION

Product	Package Description	Quantity
VA1210AA	13" Tape and Reel	5,000

See Lid Marking Section for actual product marking

info@vespermems.com

TABLE OF CONTENTS

SPECIFICATIONS

All specifications are at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD		1.6	1.8	3.6	V
Resonance Frequency	Fr	Frequency		4		KHz
Polarity		Acceleration in +Z direction	Increase in output voltage			
Startup Time in ZPL Mode		MODE = HIGH		10		mS
Startup Time Normal Mode		MODE = LOW		2.5		mS
Mode-Transition Time		Transition between ZPS and Normal mode within ±0.5dB of final sensitivity		200		µS
Acoustic Rejection		94dB SPL @ 250Hz, Inverse of acoustic sensitivity		85		dBV/Pa
Sensitive Axis				Z		Axis

The table below shows specifications for **ZeroPower Sensing Mode** (MODE HIGH) at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Current- ZPS Mode (1)		VDD On, MODE HIGH		10	11	µA

Note 1: In very quiet environments where acceleration is < 44mg, the current consumption in ZPS mode will increase from 10 µA to 15 µA

Table below shows specifications for **Normal Mode** (MODE LOW) at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output DC		DC Bias on pins OUTP and OUTM		0.75		V
Output Offset		Voltage offset between OUTP and OUTM		±10		mV
Output Noise		100Hz-2.4kHz, A-weighted Noise		-87		dBV(A)
Equivalent Input Noise	EIN	100Hz to 2.4kHz, A-weighted, Input Referred		0.85		mg rms
Sensitivity	SENS	250Hz, Differential	-29	-28	-27	dBV/g
Signal-to-Noise Ratio	SNR	1grms @ 250Hz 100Hz-2.4kHz, A-weighted Noise		59		dB(A)
Total Harmonic Distortion	THD	1g, 250Hz		0.1		%
Max Input Level	VOP	10.0% THD		8.5		g
Power Supply Rejection Ratio	PSRR	VDD = 1.8V, 250Hz, 100mV$_{PP}$ Sine Wave		-75		dB
Power Supply Rejection	PSR	VDD = 1.8V, 217Hz, 100mV$_{PP}$ square wave, 100 Hz – 2.4kHz, A-weighted		-85		dB(A)
Supply Current- Normal Mode		VDD On, MODE LOW		105	115	µA
Output Impedance	ZOUT	Single-Ended output		400		Ω

DEVICE MODES

MODE	Conditions	OUTP/OUTM Differential Output	DOUT Output	Mode Transition Time	Supply Current
OFF	VDD OFF	NA	NA	NA	NA
ZPS (1)	VDD ON, MODE HIGH	Bias only	ZPS FLAG	200µS	10µA (2)
Normal Mode	VDD ON, MODE LOW	Audio Output	ZPS FLAG	200µS	105µA

Note: 1) The first time VDD is applied, it will take 1sec for the ZPS mode to adapt to the environment and be ready to trigger on vibrations.
2) In very quiet environments where acceleration is < 44mg, the current consumption in ZPS mode will increase from 10µA to 15µA.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage	-0.3 to +3.6	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +150	°C
Mechanical Shock	10,000g per MIL-STD-883 M2002	

RELIABILITY SPECIFICATIONS

Stress Test	Method	Description
Temperature Cycling Test	JESD22-A104 (G)	-40°C to +125°C, 850 cycles
High Temperature Operating Life	JESD22-A108	+125°C, 1000 hours, biased
High Temperature Storage	JESD22-A103	+150C, 1000 hours, unbiased
Temperature Humidity Bias	JESD22-A101	+85°C, 85% RH, 1000 hours, biased
Reflow	J-STD-020 - Level 1	3 reflow cycles with peak temperature of +260°C
ESD-HBM	JS-001	3 discharge, all pins, ± 2kV
ESD-CDM	JS-002	3 discharges, all pins, ± 750V
Mechanical Shock	MIL-STD-883 M2002 (E)	10,000g , 0.2ms
Moisture Sensitivity Level	J-STD-020 - Level 1	Class 1

ACCELEROMETER OPERATION

NORMAL MODE

In Normal Mode, when MODE is LOW, the VA1210 accelerometer will act as a normal analog output accelerometer. The VA1210 senses acceleration and provides a differential output on the OUTP and OUTN pins.

ADAPTIVE ZEROPOWER SENSING™ MODE

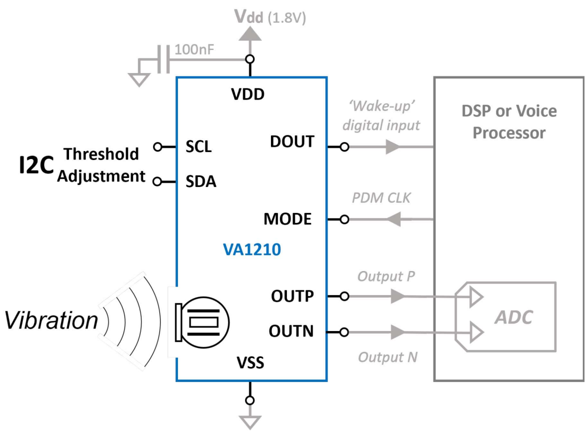
When MODE is HIGH, the device enters ZPS mode. In ZPS mode, DOUT goes high to indicate that the acceleration input has exceeded the set threshold. The typical application circuit for the VA1210 is shown below. Usage of the OUTP/OUTN pins and the DOUT pin for ZPS digital trigger is shown below.

The ZPS threshold automatically adapts to the background acceleration level in the environment. In situations with high background vibration, the threshold increases, so that the accelerometer does not trigger too often. Conversely, in quiet environments with low background vibration, the threshold automatically decreases to trigger on 'quieter' acceleration events. When the incoming vibration (acceleration) exceeds the ZPS threshold, the VA1210 sends an interrupt signal to the external codec or voice processor using a digital output pin (DOUT). The processor then pulls MODE LOW to switch to Normal Mode.

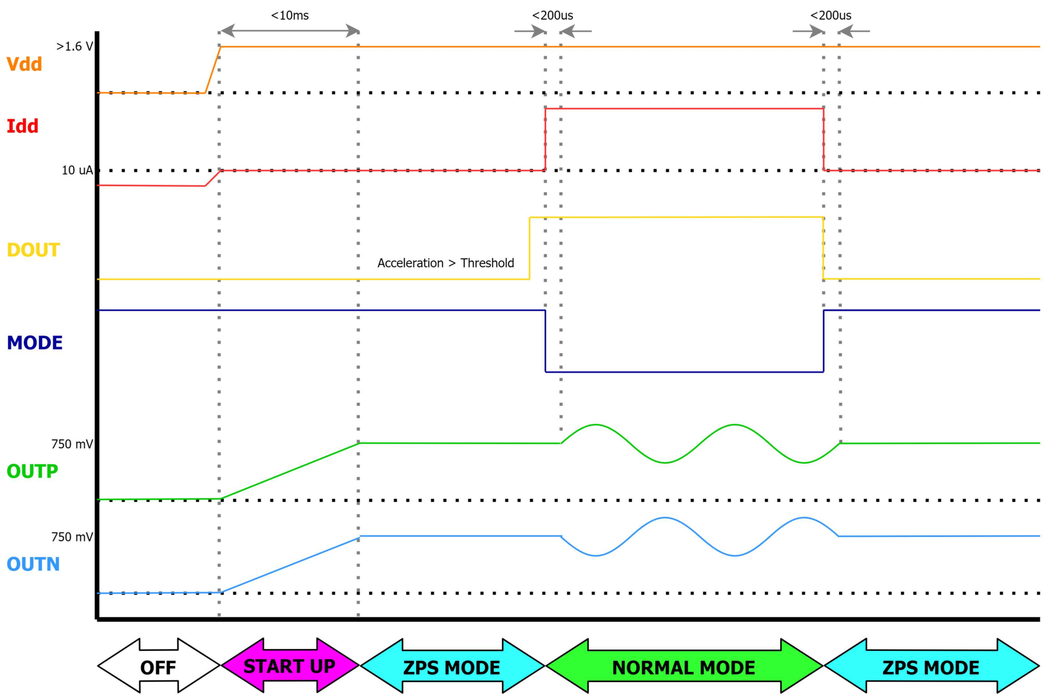
By default, ZPS is configured for TWS applications. The ZPS threshold is set to its lowest setting to trigger DOUT when a user starts talking. To ensure DOUT triggers when a user starts talking, the ZPS adaptive loop is turned off. The threshold acceleration level of a user talking is a static level. The ZPS threshold and ZPS adaptive loop together will ensure DOUT will trigger when a user starts speaking and stay low when they stop.

SOFT START

In order to prevent any pop or click noise, the VA1210 will maintain its outputs at common mode (VCM) while in ZPS mode. This will eliminate large turn-on transients at the VA1210 outputs when transitioning from ZPS to Normal Mode.

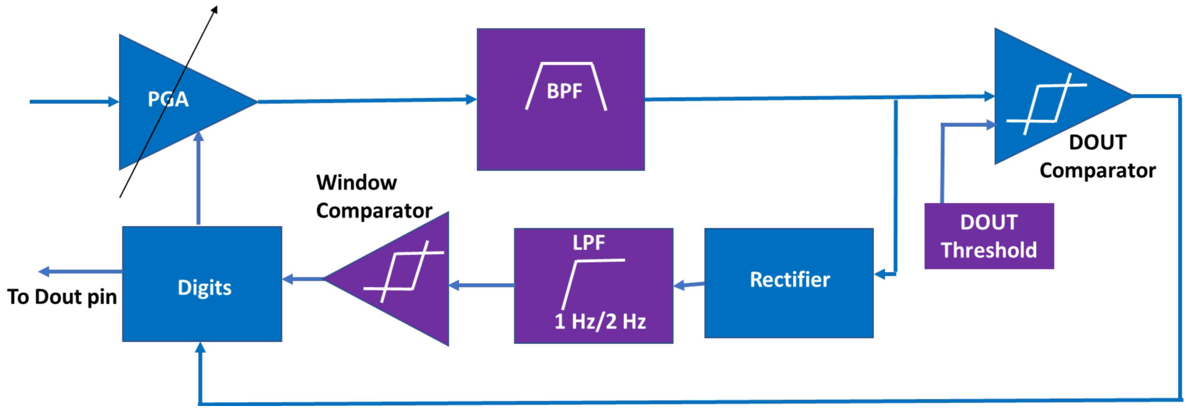


Typical Application Schematic



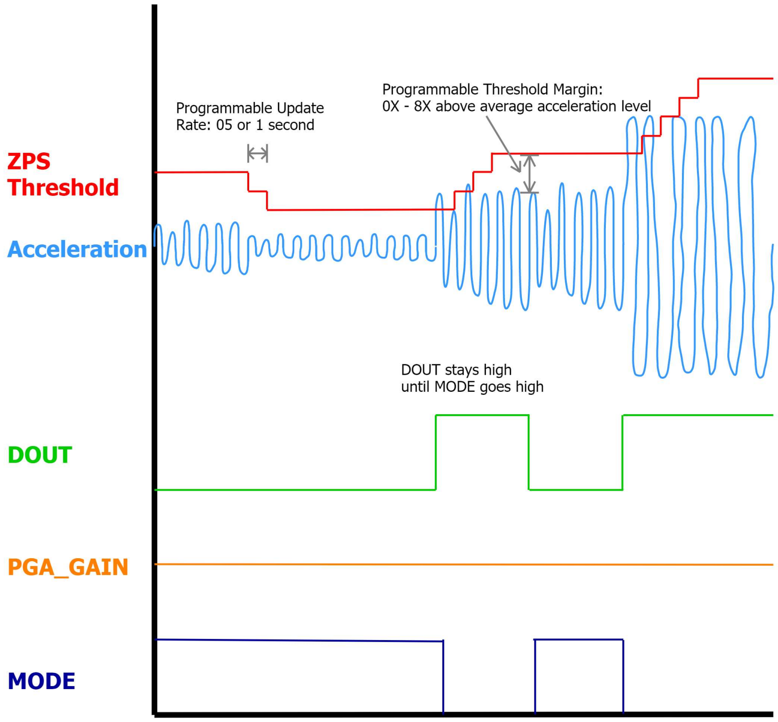
Switching between modes, when DOUT is High, the application processor can switch the VA1210 into Normal Mode. In Normal Mode, the VA1210 will output the analog audio signal.

The VA1210 block diagram with user-programmable blocks is shown below. Blocks shown in purple indicate I2C R/W programmable registers. By default, the feedback loop is turned off. This can be turned on by setting the PGA_GAIN to different values.



Block Diagram of VA1210 with I2C programmable blocks shown in purple

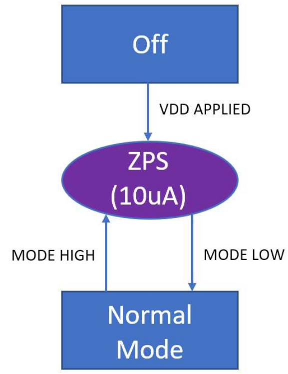
Adaptive Mode automatically senses the average acceleration level of the environment, and adjusts the gain parameter, PGA_GAIN of the programmable gain amplifier (PGA) over time. This is accomplished using a rectifier, low-pass filter (LPF), and window comparator in the feedback path of the ZPS loop. This feedback path tries to keep the input of the DOUT comparator near a fixed amplitude by rectifying the signal and filtering it with a very low corner low-pass filter (1Hz or 2Hz). Filtering with a 1Hz or 2Hz filter gives a slow-moving, long term average representation of the input acceleration level. The adaptive loop converges to the average acceleration input level within 1sec after power up and then slows back down to either 1 Hz to 2 Hz depending on how WOV_RMS bit is set. A visual description of the VA1210 Adaptive ZPA mode is shown below:



VA1210 Functional Description

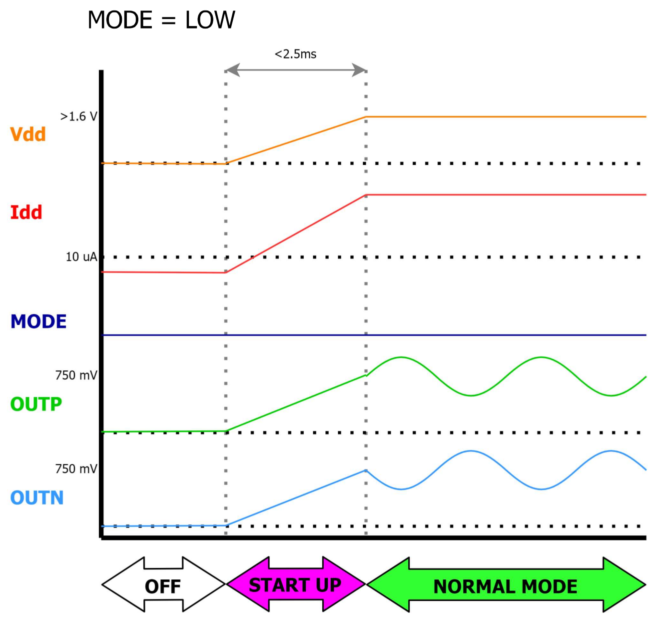
VA1210 STATE DIAGRAM

The state diagram below shows the different modes and the associated current consumption. In order to change modes, the MODE pin needs to be pulled HIGH or LOW.

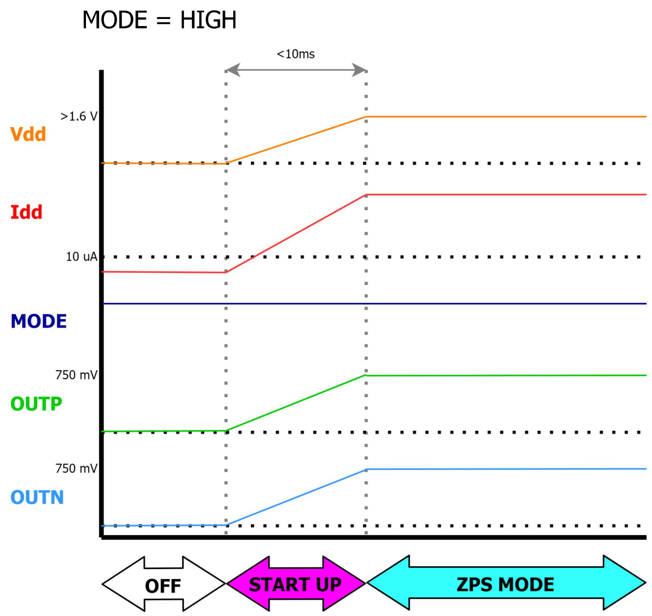


VA1210 State Diagram

POWER UP SEQUENCE



Power Sequence in Normal Mode



Power Sequence in ZPS Mode

The power-up sequence of VA1210 is shown in graphs above. Upon power-up, the part will enter ZPS mode if MODE is HIGH. For the first one second after power-up, the DOUT output will be blanked to allow the ZPS circuitry to power up correctly and settle. After this initial second, the DOUT pin will be free to trigger.

When MODE is applied LOW, the accelerometer will enter Normal Mode. The ZPS lineup will continue to function during Normal Mode and track the acceleration.

A DOUT pin event is not required to enter one of the accelerometer modes, anytime the MODE pin is toggled the part will transition into the required mode.

When the acceleration exceeds the ZPS threshold, the VA1210 will pull the DOUT pin HIGH, and the voice processor will have to pull the MODE pin LOW so that the VA1210 enters Normal Mode. The analog output will reach +/- 0.5 dB sensitivity within 200µs.

Note: during ZPL mode the outputs will be held at common mode to ensure that no big DC shift will take place when transitioning to Normal Mode. This should prevent any pop or click noise.

ELECTRICAL SPECIFICATION FOR I2C

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
LOW-level input voltage [1]	V_{IL}		-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	-0.5	0.3 V_{DD}	V
LOW-level input voltage [1]	V_{IH}		0.7 V_{DD}	[2]	0.7 V_{DD}	[2]	0.7 V_{DD} [1]	[2]	V
Hysteresis of Schmitt trigger inputs	V_{hys}				0.05 V_{DD}		0.05 V_{DD}		V
LOW-level output voltage 1	V_{OL1}	(open-drain or open-collector) at 3mA sink current; V_{DD}>2V	0	0.4	0	0.4	0	0.4	V
LOW-level output voltage 2	V_{OL2}	(open-drain or open-collector) at 2mA sink current [3]; V_{DD}<=2V			0	0.2 V_{DD}	0	0.2 V_{DD}	V
LOW-level output current	I_{OL}	V_{OL} = 0.4 V	3		3		20		mA
		V_{OL} = 0.6 V [4]			6				mA
Output fall time from V_{IHmin} to V_{ILmax}	t_{Of}			250 [5]	20 x (V_{DD} / 5.5 V) [6]	250 [5]	20 x (V_{DD} / 5.5 V) [6]	120 [7]	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}				0	50 [8]	0	50 [8]	ns
Input current each I/O pin	I_i	0.1V_{DD} < V_I < 0.9V_{DDmax}	-10	+10	-10[9]	+10 [9]	-10[9]	+10 [9]	µA
Capacitance for each I/O pin [10]	C_i			10		10		10	pF

Characteristics of the SDA and SCL I/O Stages

[1] Some legacy Standard-mode devices had fixed input levels of V_{IL} = 1.5 V and V_{IH} = 3.0 V. Refer to component datasheets.
[2] Maximum V_{IH} = $V_{DD(max)}$ + 0.5 V or 5.5 V, whichever is lower. See component datasheets.
[3] The same resistor value to drive 3 mA at 3.0 V V_{DD} provides the same RC time constant when using <2 V V_{DD} with a smaller current draw.
[4] To drive a full bus load at 400 kHz, 6 mA I_{OL} is required at 0.6 V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.
[5] The maximum t_{of} for the SDA and SCL bus lines quoted in the table below (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors (R_s) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_{of} .
[6] Necessary to be backward compatible with fast mode.
[7] In fast-mode plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
[8] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
[9] If VDD is switched off, I/O pins of fast-mode and fast-mode plus devices must not obstruct the SDA and SCL lines.
[10] Special purpose devices such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

Parameter	Symbol	Conditions	Standard mode		Fast mode		Fast mode plus		Units
			Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		0[1]	100	0	400	0	1000	kHz
hold time (repeated) START condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	4.0		0.6		0.26		µS
LOW period of the SCL clock	t_{LOW}		4.7		1.3		0.5		µS
HIGH period of the SCL clock	t_{HIGH}		4.0		0.6		0.26		µS
Set-up time for a repeated START	$t_{SU;STA}$		4.7		0.6		0.26		µS
Data hold time [2]	$t_{HD;DAT}$	CBUS compatible masters	5.0						µS
		I2C bus devices	0 [3]	[4]	0 [3]	[4]	0		µS
Data set-up time	$t_{SU;DAT}$		250		100 [5]		50		ns
Rise time of both SDA and SCL signals	t_r			1000	20	300		120	ns
Fall time of both SDA and SCL Signals [3][6][7][8]	t_f			300	20 x (V_{DD} / 5.5V)	300	20 x (V_{DD} / 5.5V) [9]	120 [8]	ns
Set-up time for STOP condition	$t_{SU;STO}$		4.0		0.6		0.26		µS
Bus free time between a STOP and START condition	t_{BUF}		4.7		1.3		0.5		µS
Capacitive load for each bus line [10]	C_b			400		400		550	pF
Data valid time [11]	$t_{VD;DAT}$			3.45 [4]		0.9 [4]		0.45 [4]	µS
Data valid acknowledge time [12]	$t_{VD;ACK}$			3.45 [4]		0.9 [4]		0.45 [4]	µS
Noise margin at the LOW level	V_{nL}	For each connected device (including hysteresis)	0.1 V_{DD}		0.1 V_{DD}		0.1 V_{DD}		V
Noise margin at the HIGH level	V_{nH}	For each connected device (including hysteresis)	0.2 V_{DD}		0.2 V_{DD}		0.2 V_{DD}		V

Characteristics of the SDA and SCL bus lines for Standard, Fast, Fast mode plus I2C bus devices

[1] f_{SCL} = Min frequency of SCL of 0 assumes the WDT is disabled

[2] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission, and the acknowledge.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[4] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[5] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also, the acknowledge timing must meet this set-up time.

[6] If mixed with Hs-mode devices, faster fall times according to the table are allowed.

[7] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[8] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[9] Necessary to be backward compatible to Fast mode.

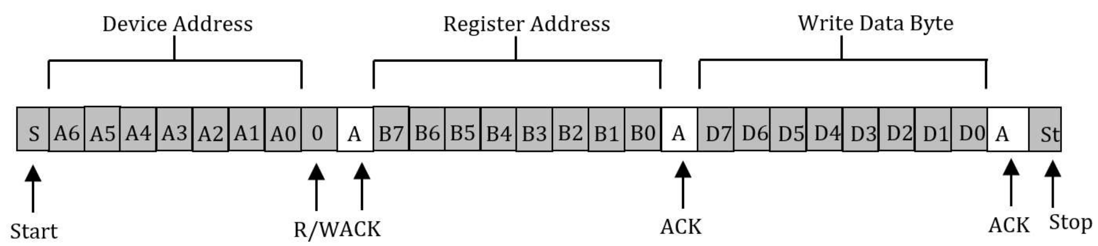
[10] The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application.

[11] $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

[12] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse)

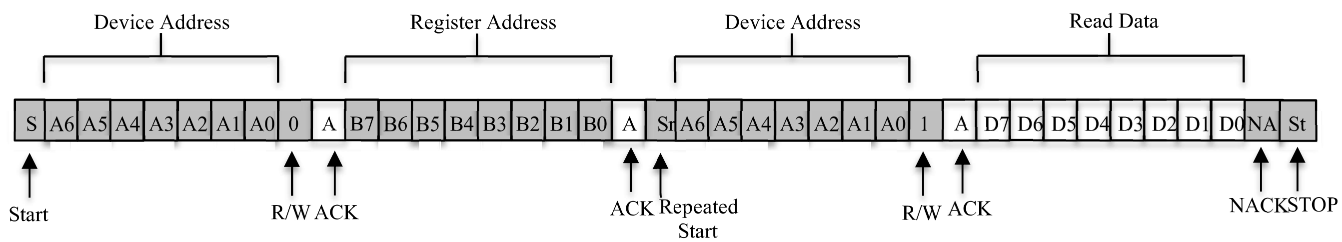
I2C TRANSACTIONS

The I2C write transaction is show below. The device address is transmitted first followed by the Read/Write (R/W) bit, to determine whether the transaction is a read or write transaction followed by the register address and the write data. The 7 bit device address is made up of 7 hard coded bits, A6 thru A0, that are hard coded to 61 hex. In the case of the I2C write transaction the R/W bit is low. The ACK is transmitted by the VA1210's I2C interface by pulling the SDA pin low.



I²C Write Transaction

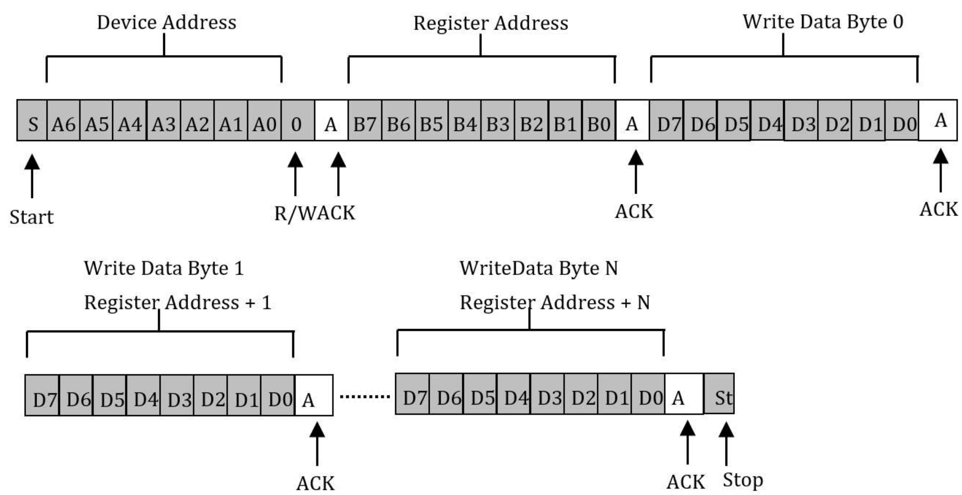
The I2C read transaction starts out the same as the write transaction with device address followed by R/W bit low followed by the register address. The difference is after the register address a repeated start condition is issued following by the device address again. After the device address the R/W bit is transmitted high. Once the I2C slave sees the R/W bit high, the I2C slave will start transmitting the 8 bit data from the register selected by the register address. To end the read transaction the I2C master will issue a NACK followed by a STOP.



I²C Read Transaction

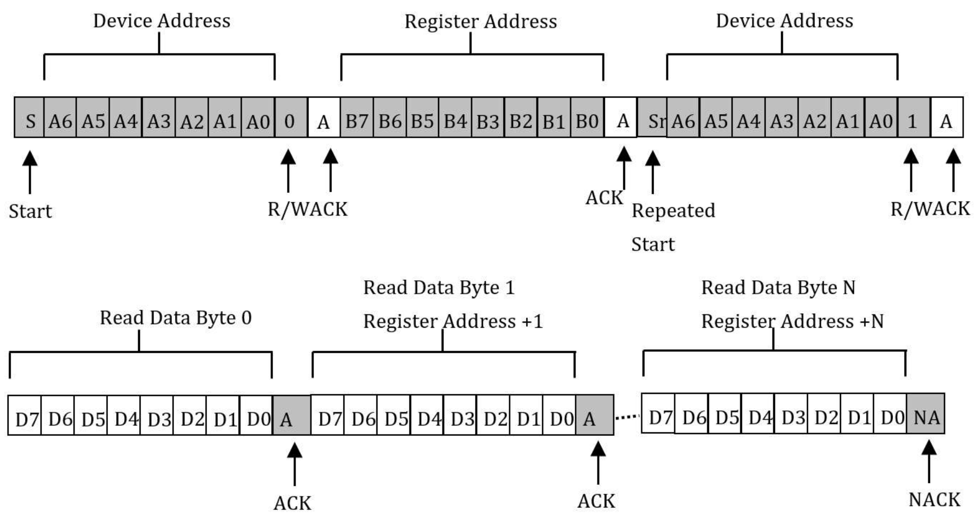
EXTENDED I2C TRANSACTION

The I2C Interface supports extended read and write transactions of the registers. The write burst transaction shown below starts out as a normal I2C write except instead of issuing a Stop at the end of the transaction, the transaction continues. As each byte is written the register address is incremented to write the next byte. The burst is finally ended by issuing a Stop following the last written byte.



I²C Write Burst

The read burst starts out with a I2C Read transaction as shown below. At the end of the first byte read by the I2C Master the I2C Master issues an ACK instead of a NAK. As each byte is read back by the I2C Master, the register address is incremented to the next register to be read. The read burst transaction is finally ended by a NACK followed by a STOP.



I²C Read Burst

info@vespermems.com

I2C ADDRESS

The VA1210 has one I2C address; 0x61.

I2C REGISTERS

The I2C Registers below are user-programmable by setting the appropriate register settings.

Values in parenthesis indicate the default settings for I2C registers shipped with the device. These default values can be read back from the device using I2C readback.

Feature	Address	B7	B6	B5	B4	B3	B2	B1	B0	Read/Write
I2C_Cntrl	0x0			MODE (0x0)	DOUT_CLEAR (0x0)	DOUT_RAW (0x0)	WDT_DLY (0x0)		WDT_ENABLE (0x0)	R/W
WOV_PGA_GAIN	0x1				WOS_PGA_GAIN					R
WOV Filter	0x2				WOV_HPF (0x0)		WOV_LFP (0x0)			R/W
WOV PGA MIN THR	0x3		FAST_MODE_CNT (0x0)		WOV_PGA_MIN_THR (0x1B)					R/W
WOV PGA MAX THR	0x4			WOV_RMS (0x0)	WOV_PGA_MAX_THR (0x1B)					R/W
WOV THRESH	0x5						WOV_THRESH (0x0)			R/W
BIST Cntrl	0x6							BIST_POL (0x0)	BIST_EN (0x0)	R/W

User Programmable I2C Registers

I2C USER PROGRAMMABLE REGISTERS IN VA1210

MODE: this bit will act like the MODE pin if the MODE pin is kept LOW. When this bit is set at 0 the VA1210 will be in Normal Mode. When this bit is set at 1 the VA1210 will be in ZPS mode.

DOUT_CLEAR: when set to 1, DOUT pin will be reset to LOW. This is another way to reset the ZPS mode to look for acceleration trigger without toggling the MODE pin.

DOUT_RAW: when set to 1, DOUT pin will be set as a raw mode which will give access to the DOUT comparator output. When DOUT_RAW is set at 0 the output will be latched until the MODE pin is pulled high again. When set to 1 the DOUT pin can be used to determine when voice is detected and goes above a preset threshold. This function can be used as a Hardware VAD function.

<u>Note</u>: based on Vesper's internal analysis the Hardware VAD function will perform best if WOV_PGA_MIN_THR and WOV_PGA_MAX_THR are set to the same value at 0x1B. This will ensure that the ZPS loop stops adapting. The WOV_THRESH is programmed at 0x0 by default but a value of 0x1 can also be used. It is recommended to try the VAD function on multiple users before choosing the final parameters of the ZPS lineup.

WDT_Delay: In the rare case when the host stops toggling the SCL clock in the middle of an I2C transaction, I2C interface has a Watch Dog Timer to reset the I2C logic. By default, the timer is reset and disabled upon detection of either SCL or SDA transaction. If the timer exceeds the time controlled by the WDT_DLY bits, then the entire I2C logic is reset (the registers and all other logic on VA1210 are not affected). **WDT_Delay** register Sets the watchdog time delay.

WDT_DLY	Watchdog Timer Delay (ms)
00	8
01	16
10	32
11	64

WDT_Enable: The Watchdog Timer can be disabled by setting the WDT_ENABLE bit low.

Programmable gain amplifier gain (WOV_PGA_GAIN) is automatically adjusted by the feedback loop, as described above. The gain value can be read back using I2C register to monitor the ambient acceleration level while in adaptive ZPS mode. The table below shows the translation between acceleration levels and PGA gain. The ZPS engine enables background acceleration level detection in applications such as TWS earbuds, hearables, etc. where the vibration noise must be monitored constantly to identify a new user case (anti-rattling in headphone for example). The device can get the PGA_GAIN register value from I2C and use the lookup table below to measure the background acceleration level. The accelerometer can still operate in ZPS mode during this readback process.

Note: these values have been determined with a WOV_THRESH set a 0x0

WOV_PGA_GAIN[4:0]	Acceleration (g RMS)	WOV_PGA_GAIN[4:0]	Acceleration (g RMS)
00000	1.337	10000	0.084
00001	1.125	10001	0.071
00010	0.947	10010	0.060
00011	0.797	10011	0.050
00100	0.670	10100	0.042
00101	0.564	10101	0.036
00110	0.474	10110	0.030
00111	0.399	10111	0.025
01000	0.336	11000	0.021
01001	0.283	11001	0.018
01010	0.238	11010	0.015
01011	0.200	11011	0.013
01100	0.168	11100	0.011
01101	0.142	11101	0.009
01110	0.119	11110	0.008
01111	0.100	11111	0.006

RMS background acceleration level / Gain Correlation (Address 0x0, Bitfield: [4:0]); WOV_THRESH=0x0

Band Pass Filter (BPF) can be programmed via I2C to adjust the lower and upper frequency between which the device will wake up. The corner frequency settings supported by WOV_LPF and WOV_HPF register bits are below:

WOV_LPF	Corner Frequency (kHz)
000	1
100	2
101	4
110	6
111	8

Low-pass Filter Corners (Address 0x2, Bitfield: [2:0])

WOV_HPF	Corner Frequency (Hz)
00	200
01	300
10	400
11	800

High-pass Filter Corners (Address 0x2, Bitfield: [4:3])

FAST_MODE_COUNT can be programmed to increase the speed at which the ZPS feedback loop adapts to a large change in background noise. The FAST MODE is triggered according to the FAST_MODE_CNT setting described in the table below. For example, when FAST_MODE_CNT[1:0]=01, if the PGA Gain is incremented two times in a row or decremented two times in a row, the FAST MODE will engage.

FAST_MODE_CNT[1:0]	Description
00	Fast mode disabled
01	If two window comparator trips in a row in the same direction, the clocks are sped up 16x
10	If four window comparator trips in a row in the same direction, the clocks are sped up 16x
11	If six window comparator trips in a row in the same direction, the clocks are sped up 16x

Adaptive Loop Fast Start Count (Address 0x3, Bitfield: [6:5])

WOV_RMS can be set to Low/High to switch the sampling interval of the comparator signal between 1 seconds and 0.5 seconds. This effectively changes the low pass corner frequency from 1Hz to 2Hz.

WOV_RMS	Comparator Sampling Interval (seconds)
Low	1
High	0.5

Adaptive Loop Update Frequency (Address 0x4, Bitfield: [5])

WOV_PGA_MAX and **WOV_PGA_MIN** limits are the maximum and minimum allowable gains of the WOV PGA, which define the boundary for the control loop. The PGA Gain would not go higher or lower than the values set in the registers when the ZPS adaptive threshold is being tracked. The bitfields on these registers can be set to any value between '0000' and '11111' corresponding to threshold range between 22mg and 1.5g as per the Table given in WOV_PGA_GAIN register above.

WOV_THRESH can be used to program the threshold level from 0 dB to 18 dB . The table below outlines the different WOV_THRESH values available. Essentially, this programs the amount of margin above the RMS background acceleration level that is needed to trip the DOUT comparator. For example, a code of 100 for WOV_THRESH will program the accelerometer to trigger at a level 5x above the RMS background acceleration level.

WOV_THRESH	Trigger input level relative to average acceleration noise level
000	1x (Default)
001	2x
010	3x
011	4x
100	5x
101	6x
110	7x
111	8x

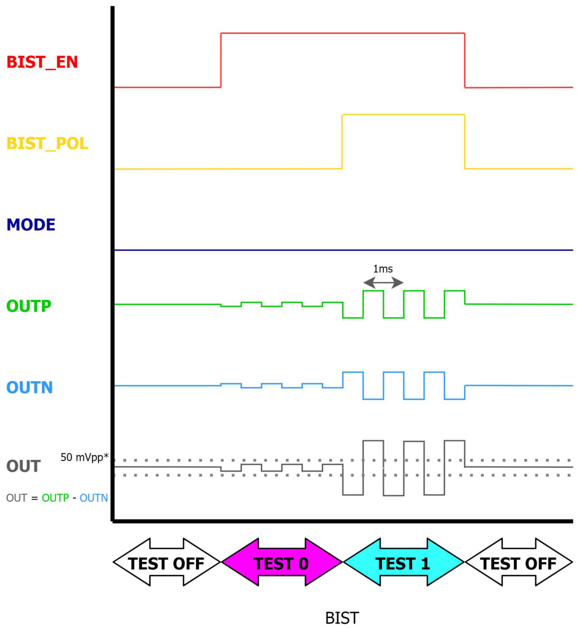
Dout Comparator Threshold Programmable Values

Note: WOV_THRESH value of 000 is not normally recommended for VA1210. This setting corresponds to the RMS level of the background acceleration noise. Therefore, DOUT will trip often just from fluctuations in input acceleration amplitude, and the accelerometer will trigger consistently. However, in some special use cases WOV_THRESH value of 000 can be used. For example, in a TWS earbud where the wearer's voice is the primary acceleration signal and the device's self-noise is the primary background noise, a fixed (non-adaptive) PGA_GAIN setting (WOV_PGA_MAX and WOV_PGA_MIN both at 0x1B) and WOV_THRESH at 000 will give good voice detection and no false trigger on background noise.

BIST_EN and **BIST_POL**: the VA1210 has a BIST function to help customer test the VA1210 during manufacturing. To enable this function the BIST_EN bit needs to be set to 1. The **BIST_POL** controls the polarity of the test.

BIST FUNCTION

The BIST (Built In Self Test) function is designed to provide a basic product integrity test.
The diagram below shows what the output of the VA1210 will look like when the device behaves as expected:



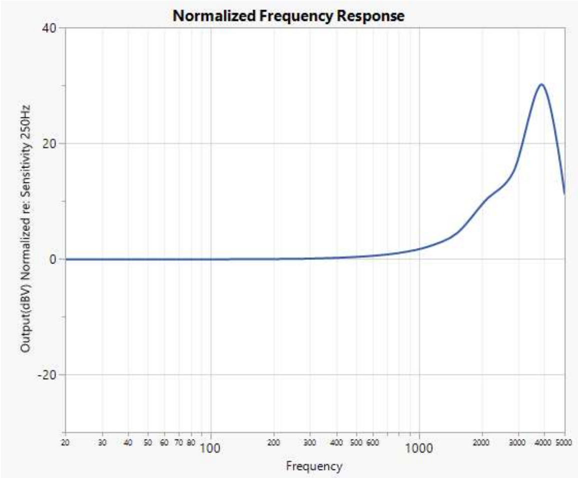
BIST expected test waveform. See "BIST expected value table" for OUT threshold.

When the MODE pin is LOW and the BIST_EN bit is set to 1 the VA1210 enters the BIST mode. If the BIST_POL bit is set to 0 the analog outputs should stay at VCM. When the BIST_POL is set to 1 the analog outputs will start switching at a 1000Hz frequency. Any deviations from this expected behavior (table below) will indicate an internal failure from the VA1210.

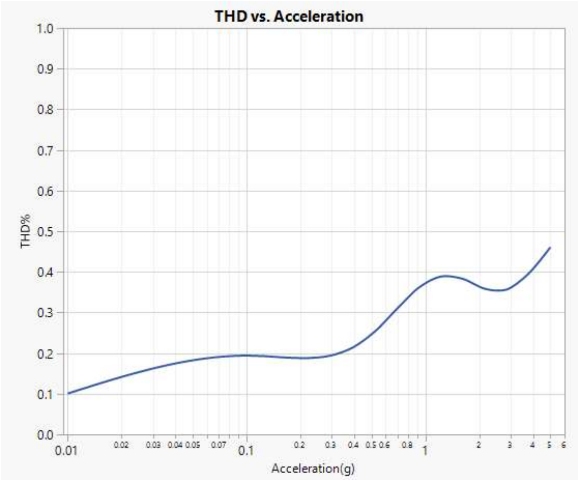
BIST_EN	BIST_POL	Expected OutP-OutM switching amplitude
High	High	> 50 mV_{PP}
High	Low	< 50 mV_{PP}

BIST expected values table

TYPICAL PERFORMANCE CHARACTERISTICS



a. Normalized Frequency Response



b. THD (%) vs Acceleration (g)

SOLDER REFLOW PROFILE

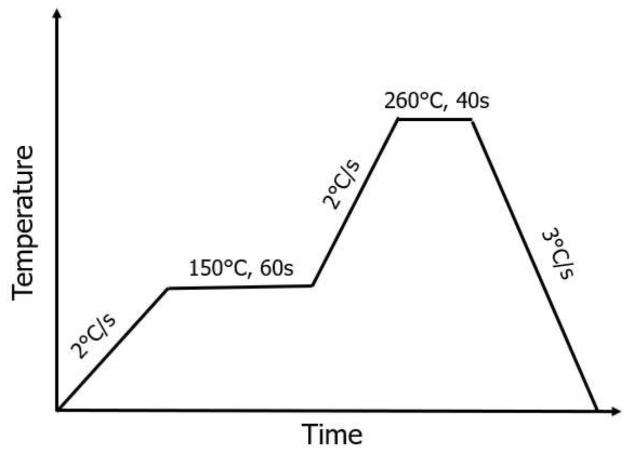
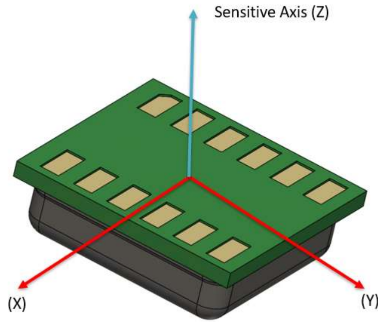


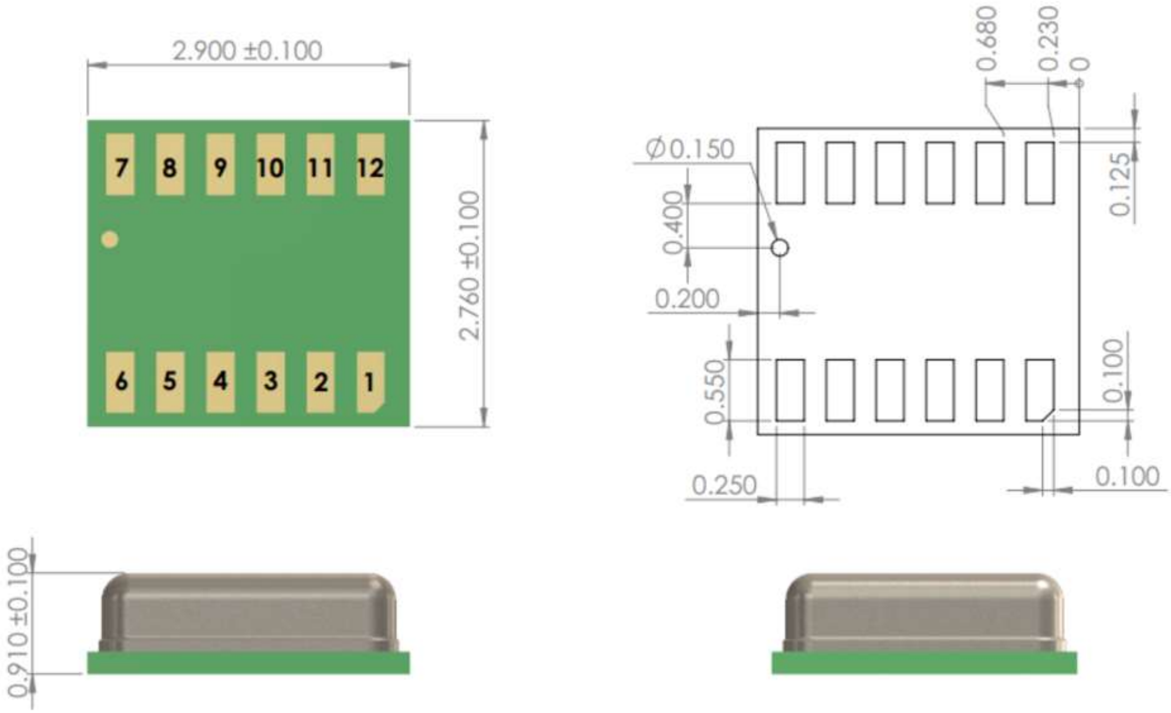
Figure 6: Solder Reflow Profile

SENSITIVE AXIS



Note: Sensitive Axis (Z), Direction Shown (Z-)

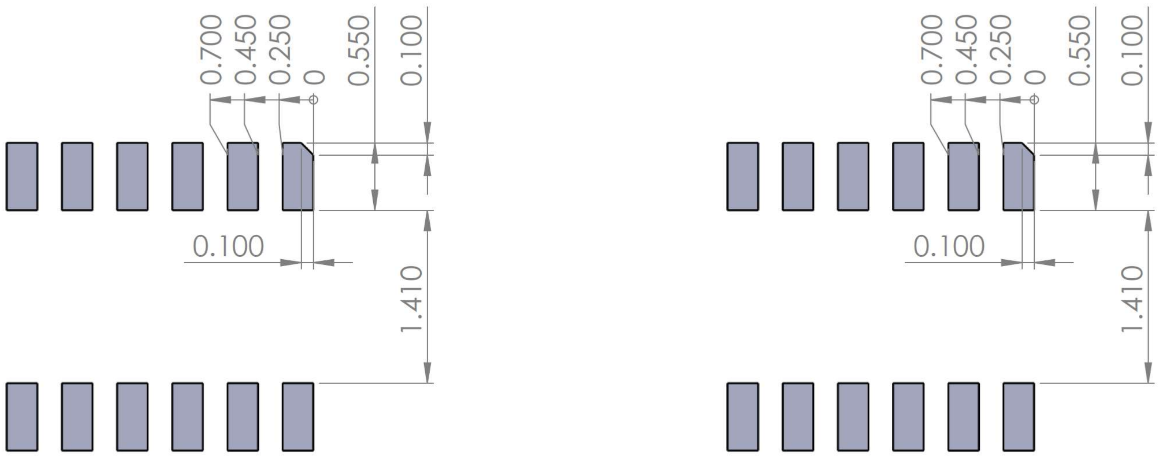
DIMENSIONS AND PIN LAYOUT (Bottom View / Terminal Side Up)



(All dimensions are in mm)

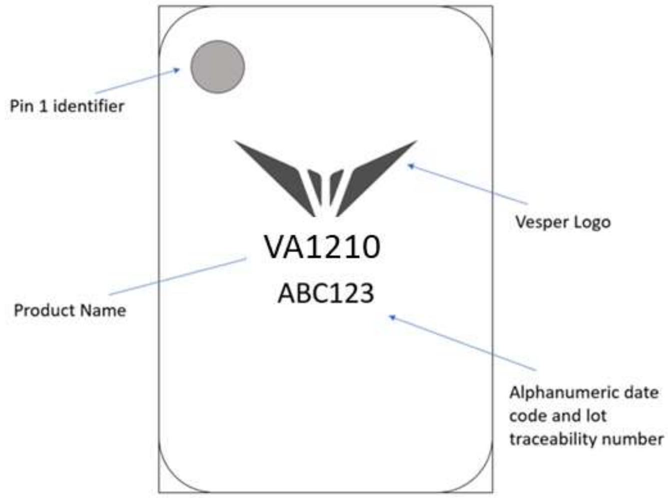
Pin Number	Pin Name	Functionality
1	OUTP	Positive Analog Output
2	OUTN	Negative Analog Output
3	GND	Ground
4	SDA	I2C Data
5	SCL	I2C Clock
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	MODE	Mode pin to change VA1210 mode of operation
11	DOUT	DOUT interrupt
12	VDD	Power

PCB DESIGN AND LAND PATTERN LAYOUT (Top View / Terminal Side Down)



PCB and Solder Stencil Pattern – All dimensions are in mm

LID MARKING



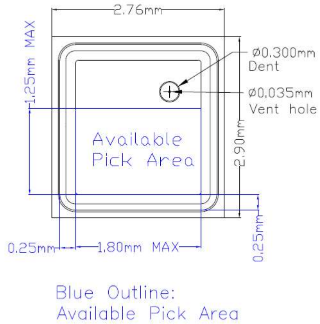
Lid Marking Description

Note: Parts marked “VE” in the product name are Engineering samples. Final samples will be marked “VA”

HANDLING INSTRUCTIONS

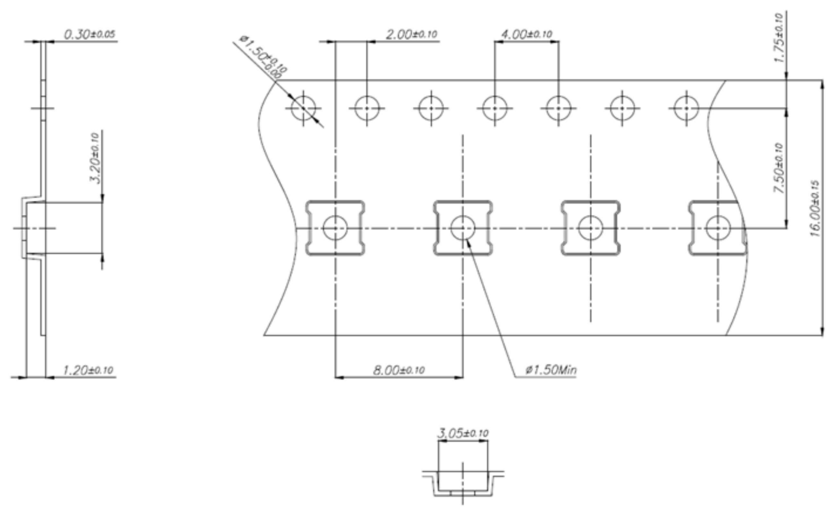
Vesper's piezoelectric MEMS devices are very resistant to harsh environments such as dust and moisture. However, to avoid mechanical damage to the MEMS structure, we recommend using appropriate handling procedures when manually handling the parts or when using pick and place equipment. The following guidelines will avoid damage:

- Do not board wash or clean after the reflow process.
- Use a placement force of <1,000g when using a pick and place machine.
- Recommended device pick location is given below

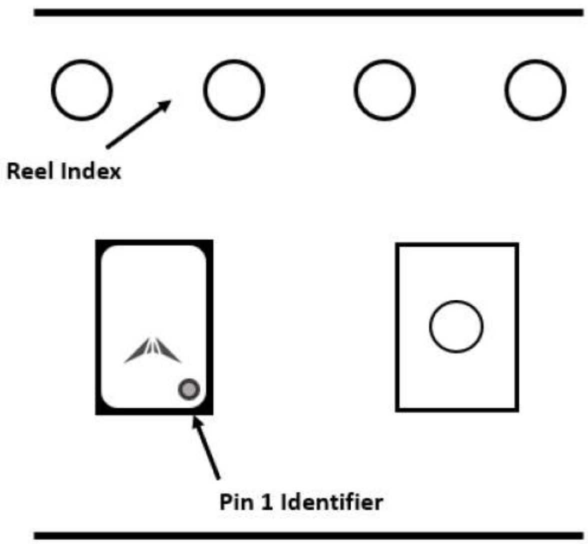


Recommended device pick location

TAPE AND REEL SPECIFICATIONS



Tape & Reel specification



Part Orientation in Reel (dimension not to scale)

SUPPORTING DOCUMENTS

AN10 – Vesper Piezoelectric MEMS Voice accelerometers Assembly and Handling Guideline
AN12 – Vesper Piezoelectric MEMS Voice Accelerometers DESIGN GUIDELINES
Technical Paper - VA1200 - Signal Validation Procedures
Flex-Board VA1210 – User Guideline

COMPLIANCE INFORMATION

Electrostatic discharge (ESD) sensitive device:
Although this product features industry-standard protection circuitry, damage may occur if subjected to excessive ESD. Proper ESD precautions should be taken to avoid damage to the device.

CONTACT DETAILS

Vesper Technologies
77 Summer St Floor 8
Boston, MA 02110
Email: info@vespermems.com

LEGAL INFORMATION

For any questions or comments on the datasheet email: erratum@vespermems.com

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REVISION HISTORY

Revision	Date	Description
0.0.0	03/07/2022	Initial Revision

info@vespermems.com