74HC4060; 74HCT4060

14-stage binary ripple counter with oscillator

Rev. 03 — 14 July 2008 Product data sheet

1. General description

The 74HC4060; 74HCT4060 are high-speed Si-gate CMOS device and is pin compatible with the HEF4060.

The 74HC4060; 74HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, RTC and CTC), ten buffered outputs (Q3 to Q9 and Q11 to Q13) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (RTC and CTC) floating. The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q3 to Q9 and Q11 to Q13 = LOW), independent of other input conditions. In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

2. Features

- All active components on chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4060N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT4060N				
74HC4060D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4060D				
74HC4060DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4060DB				
74HC4060PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4060BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4060BQ				

5. Functional diagram

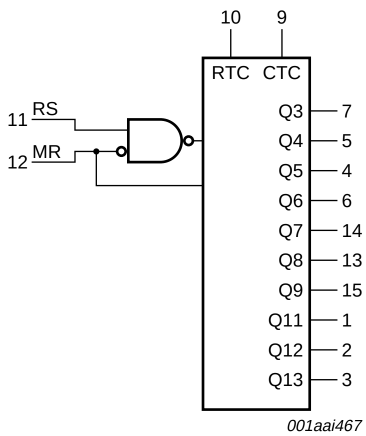


Fig 1. Logic symbol

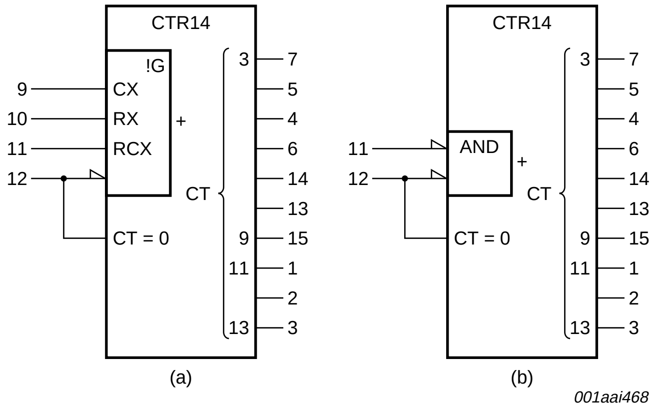


Fig 2. IEC logic symbol

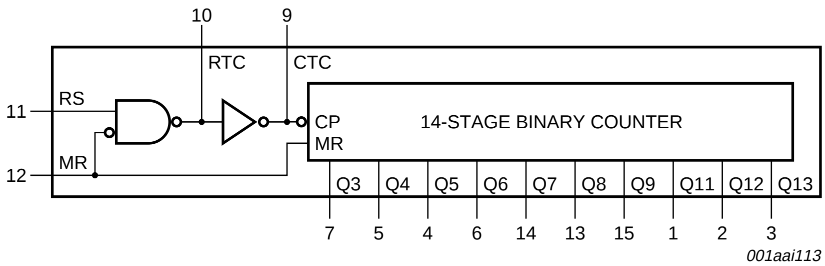


Fig 3. Functional diagram

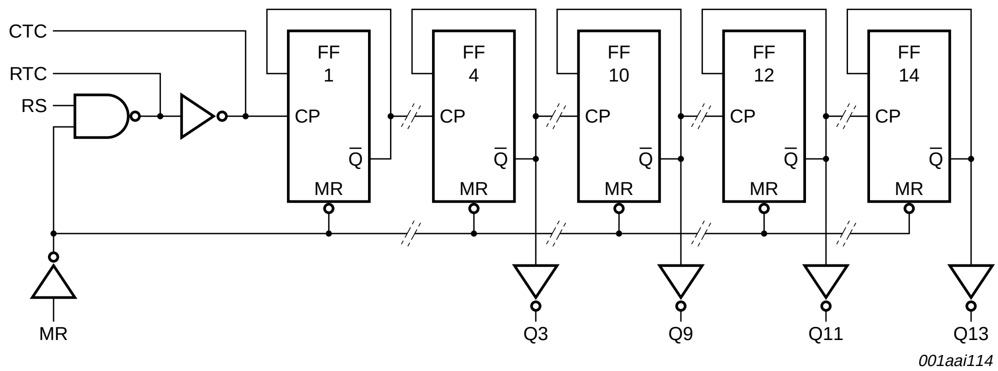


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

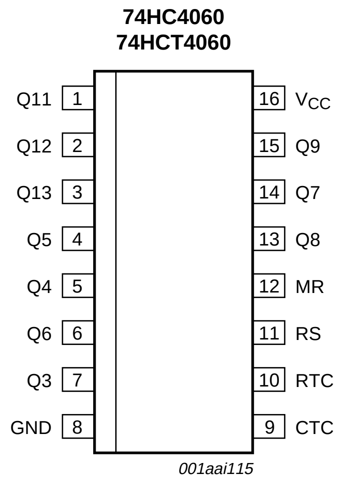
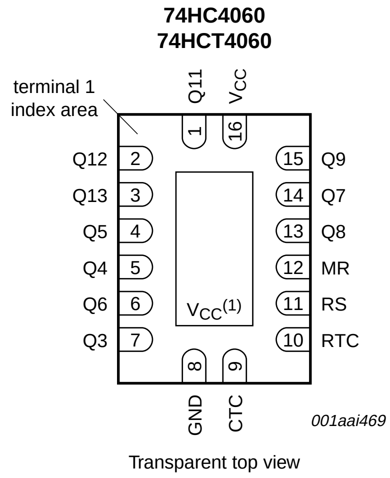


Fig 5. Pin configuration DIP16, SO16 and (T)SSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It cannot be used as supply pin or input.

Fig 6. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input /oscillator pin
MR	12	master reset input (active HIGH)
V_{CC}	16	supply voltage

7. Functional description

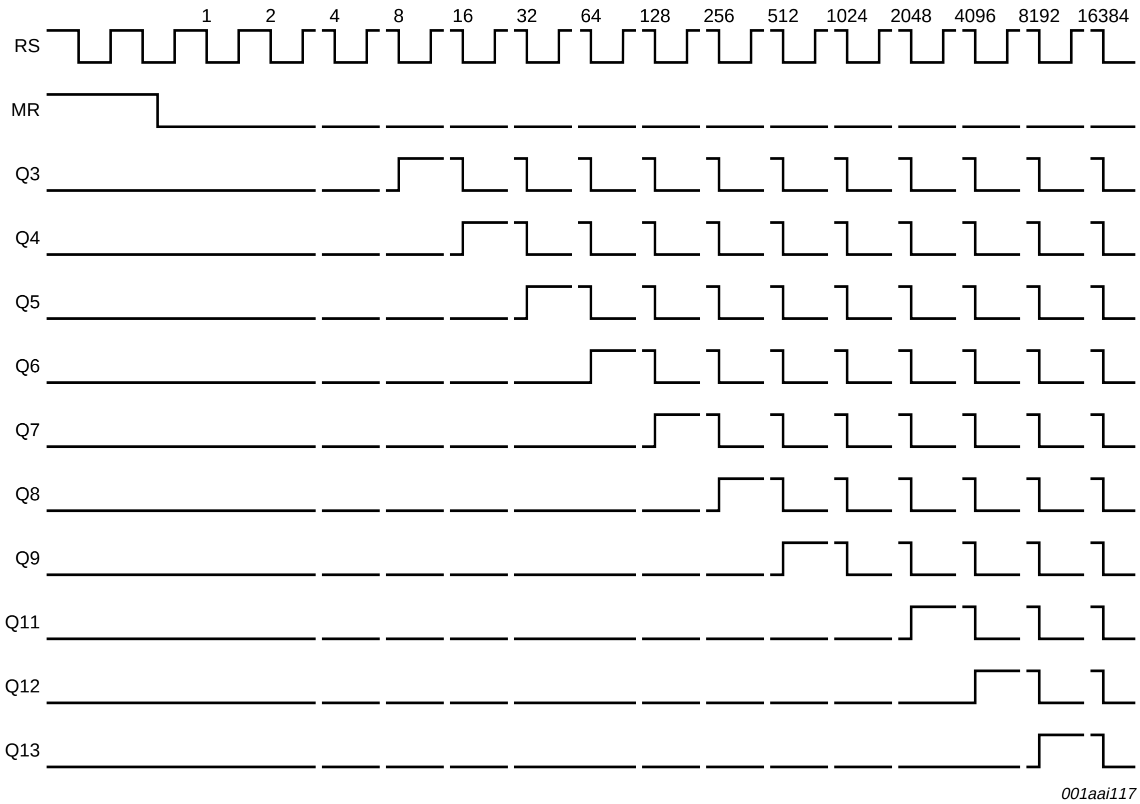


Fig 7. Timing diagram

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$–0.5$ V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C

Table 3. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		DIP16 package	[2]	-	750	mW
		SO16 package	[3]	-	500	mW
		(T)SSOP16 package	[4]	-	500	mW
		DHVQFN16 package	[5]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4060			74HCT4060			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	-	+125	–40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4060										
V_{IH}	HIGH-level input voltage	MR input								
		V_{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
		RS input								
		V_{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V_{CC} = 4.5 V	3.6	-	-	3.6	-	3.6	-	V
		V_{CC} = 6.0 V	4.8	-	-	4.8	-	4.8	-	V

Table 5. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IL}	LOW-level input voltage	MR input								
		V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
		RS input								
		V_{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V_{CC} = 4.5 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 6.0 V	-	-	1.2	-	1.2	-	1.2	V
V_{OH}	HIGH-level output voltage	RTC output; RS = MR = GND								
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –2.6 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = –3.3 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		RTC output; RS = MR = V_{CC}								
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –0.65 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = –0.85 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		CTC output; RS = V_{IH}; MR = V_{IL}								
		I_O = –3.2 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = –4.2 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V
		V_I = V_{IH} or V_{IL}; except RTC output								
		I_O = –20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		V_I = V_{IH} or V_{IL}; except RTC and CTC outputs								
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V

Table 5. Static characteristics *...continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	RTC output; RS = V_{CC}; MR = GND									
		I_O = 20 μA; V_{CC} = 2.0 V		-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V		-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V		-	0	0.1	-	0.1	-	0.1	V
		I_O = 2.6 mA; V_{CC} = 4.5 V		-	-	0.26	-	0.33	-	0.4	V
		I_O = 3.3 mA; V_{CC} = 6.0 V		-	-	0.26	-	0.33	-	0.4	V
		CTC output; RS = V_{IL}; MR = V_{IH}									
		I_O = 3.2 mA; V_{CC} = 4.5 V		-	-	0.26	-	0.33	-	0.4	V
		I_O = 4.2 mA; V_{CC} = 6.0 V		-	-	0.26	-	0.33	-	0.4	V
		V_I = V_{IH} or V_{IL}; except RTC output									
		I_O = 20 μA; V_{CC} = 2.0 V		-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V		-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V		-	0	0.1	-	0.1	-	0.1	V
		V_I = V_{IH} or V_{IL}; except RTC and CTC outputs									
		I_O = 4.0 mA; V_{CC} = 4.5 V		-	-	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V		-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V		-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V		-	-	8.0	-	80	-	160	μA
C_I	input capacitance			-	3.5	-	-	-	-	-	pF
74HCT4060											
V_{IH}	HIGH-level input voltage	MR input; V_{CC} = 4.5 V to 5.5 V	[1]	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	MR input; V_{CC} = 4.5 V to 5.5 V	[1]	-	-	0.8	-	0.8	-	0.8	V

Table 5. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	RTC output; RS = MR = V_{CC}								
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −0.65 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		RTC output; RS = MR = GND								
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −2.6 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		CTC output; RS = V_{IH}; MR = V_{IL}								
		I_O = −3.2 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		V_I = V_{IH} or V_{IL}; except RTC output								
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		V_I = V_{IH} or V_{IL}; except RTC and CTC outputs								
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	RTC output; RS = V_{CC}; MR = GND								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 2.6 mA; V_{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		CTC output; RS = V_{IL}; MR = V_{IH}								
		I_O = 3.2 mA; V_{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		V_I = V_{IH} or V_{IL}; except RTC output								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		V_I = V_{IH} or V_{IL}; except RTC and CTC outputs								
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	40	144	-	180	-	196	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

[1] For HCT4060, only input MR (pin 12) has TTL input switching levels.

11. Dynamic characteristics

Table 6. Dynamic characteristics

GND = 0 V; C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
74HC4060											
t_{pd}	propagation delay	RS to Q3; see Figure 8	[1]								
		V_{CC} = 2.0 V		-	99	300	-	375	-	450	ns
		V_{CC} = 4.5 V		-	36	60	-	75	-	90	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	31	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	29	51	-	64	-	77	ns
		Qn to Qn+1; see Figure 9	[2]								
		V_{CC} = 2.0 V		-	22	80	-	100	-	120	ns
		V_{CC} = 4.5 V		-	8	16	-	20	-	24	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	6	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	6	14	-	17	-	20	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 10									
		V_{CC} = 2.0 V		-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V		-	20	35	-	44	-	53	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V		-	16	30	-	37	-	45	ns
t_t	transition time	Qn; see Figure 8	[3]								
		V_{CC} = 2.0 V		-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V		-	6	13	-	16	-	19	ns
t_W	pulse width	RS (HIGH or LOW); see Figure 8									
		V_{CC} = 2.0 V		80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	5	-	17	-	20	-	ns
		MR (HIGH); see Figure 10									
		V_{CC} = 2.0 V		80	25	-	100	-	120	-	ns
		V_{CC} = 4.5 V		16	9	-	20	-	24	-	ns
		V_{CC} = 6.0 V		14	7	-	17	-	20	-	ns
t_{rec}	recovery time	MR to RS; see Figure 10									
		V_{CC} = 2.0 V		100	28	-	125	-	150	-	ns
		V_{CC} = 4.5 V		20	10	-	25	-	30	-	ns
		V_{CC} = 6.0 V		17	8	-	21	-	26	-	ns

Table 6. Dynamic characteristics *...continued*

GND = 0 V; C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	RS; see Figure 8									
		V_{CC} = 2.0 V		6	26	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V		30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	87	-	-	-	-	-	MHz
		V_{CC} = 6.0 V		35	95	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz	[4]	-	40	-	-	-	-	-	pF
74HCT4060											
t_{pd}	propagation delay	RS to Q3; see Figure 8	[1]								
		V_{CC} = 4.5 V		-	33	66	-	83	-	99	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	31	-	-	-	-	-	ns
		Qn to Qn+1; see Figure 9	[2]								
		V_{CC} = 4.5 V		-	8	16	-	20	-	24	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	6	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Figure 10									
		V_{CC} = 4.5 V		-	21	44	-	55	-	66	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	18	-	-	-	-	-	ns
t_t	transition time	Qn; see Figure 8	[3]								
		V_{CC} = 4.5 V		-	7	15	-	19	-	22	ns
t_W	pulse width	RS (HIGH or LOW); see Figure 8									
		V_{CC} = 4.5 V		16	6	-	20	-	24	-	ns
		MR (HIGH); see Figure 10									
		V_{CC} = 4.5 V		16	6	-	20	-	24	-	ns
t_{rec}	recovery time	MR to RS; see Figure 10									
		V_{CC} = 4.5 V		26	13	-	33	-	39	-	ns
f_{max}	maximum frequency	RS; see Figure 8									
		V_{CC} = 4.5 V		30	80	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF		-	88	-	-	-	-	-	MHz

Table 6. Dynamic characteristics *...continued*

GND = 0 V; C_L = 50 pF unless otherwise specified; for test circuit see Figure 11.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} − 1.5 V; V_{CC} = 5 V; f_i = 1 MHz	[4]	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] Qn+1 is the next Qn output.

[3] t_t is the same as t_{THL} and t_{TLH}.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

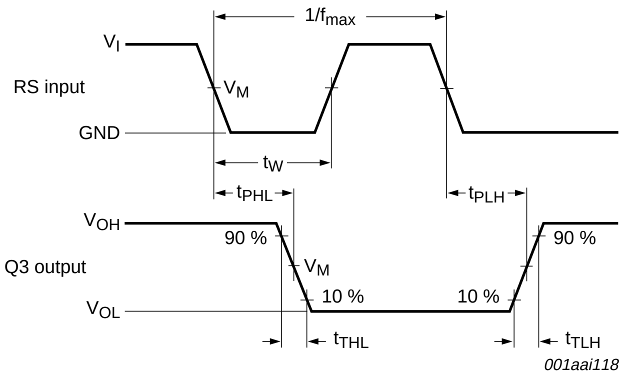
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

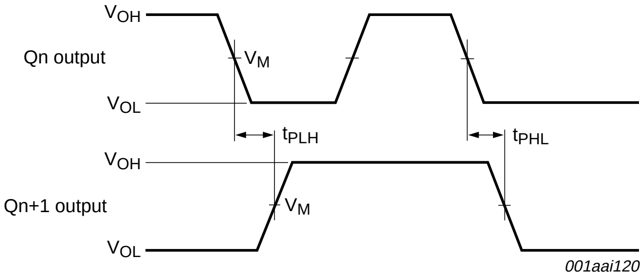
12. Waveforms



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

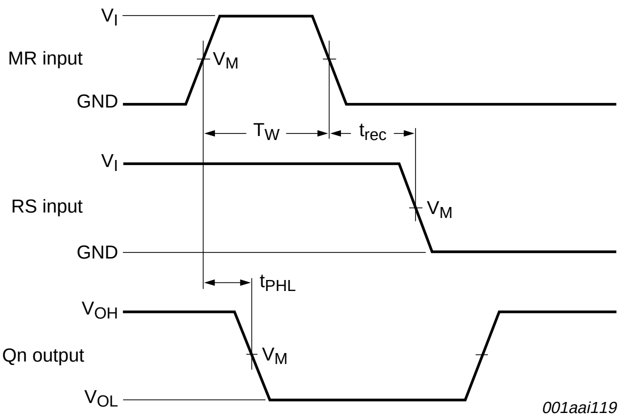
Fig 8. Waveforms showing the clock (RS) to output (Q3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Waveforms showing the output Qn to output Qn+1 propagation delays



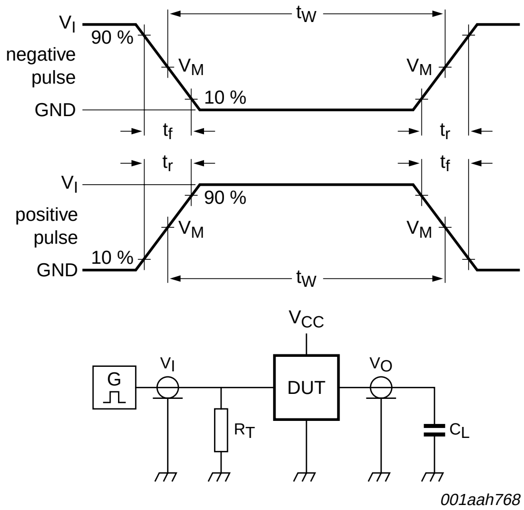
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 10. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (RS) recovery time

Table 7. Measurement points

Type	Input	Output
	V_M	V_M
74HC4060	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT4060	1.3 V	1.3 V



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 11. Test circuit for measuring switching times

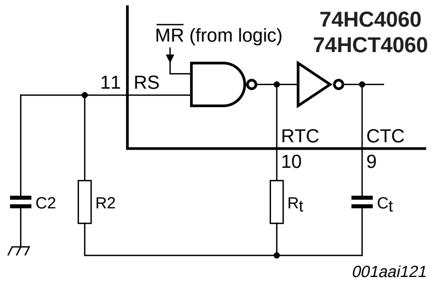
Table 8. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4060	V_{CC}	6 ns	15 pF, 50 pF
74HCT4060	3 V	6 ns	15 pF, 50 pF

13. RC oscillator

13.1 Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ $2R_t$ and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the ON resistance in series with it, which typically is 280 Ω at V_{CC} = 2.0 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6.0 V.



Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$

Fig 12. Example of a RC oscillator

The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value and 10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, R_t ≥ 1 kΩ.

13.2 Typical crystal oscillator circuit

In Figure 13, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

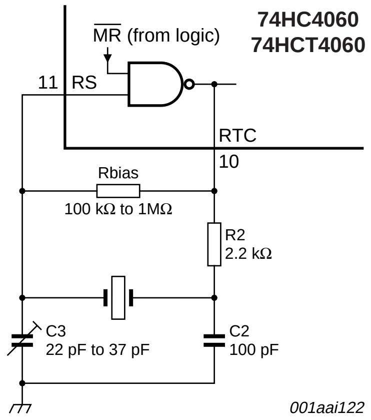
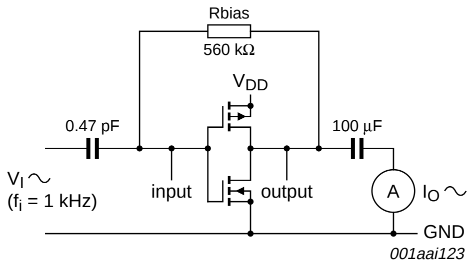


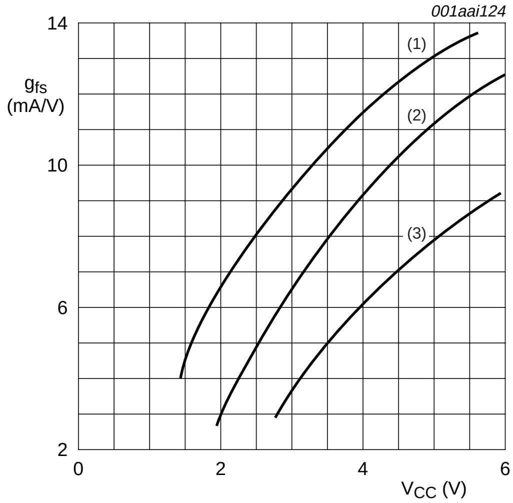
Fig 13. External component connection for a crystal oscillator



$g_{fs} = \Delta I_O / \Delta V_I$ at V_O is constant; MR = LOW.

See also Figure 15.

Fig 14. Test set-up for measuring forward transconductance



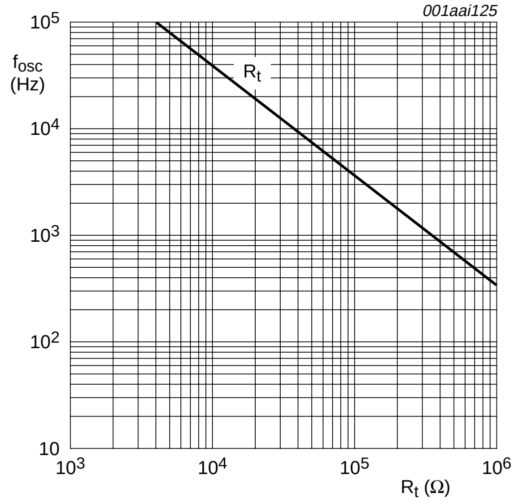
T_{amb} = 25 °C.

(1) Maximum.

(2) Typical.

(3) Minimum.

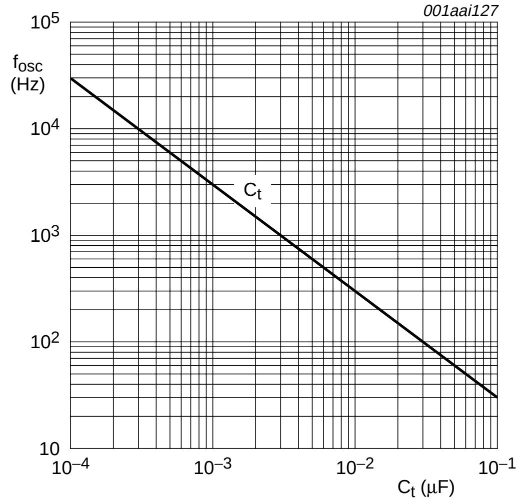
Fig 15. Typical forward transconductance as function of the supply voltage



V_{CC} = 2.0 V to 6.0 V; T_{amb} = 25 °C.

For R_t curve: C_t = 1 nF; R2 = 2 × R_t.

Fig 16. RC oscillator frequency as a function of R_t



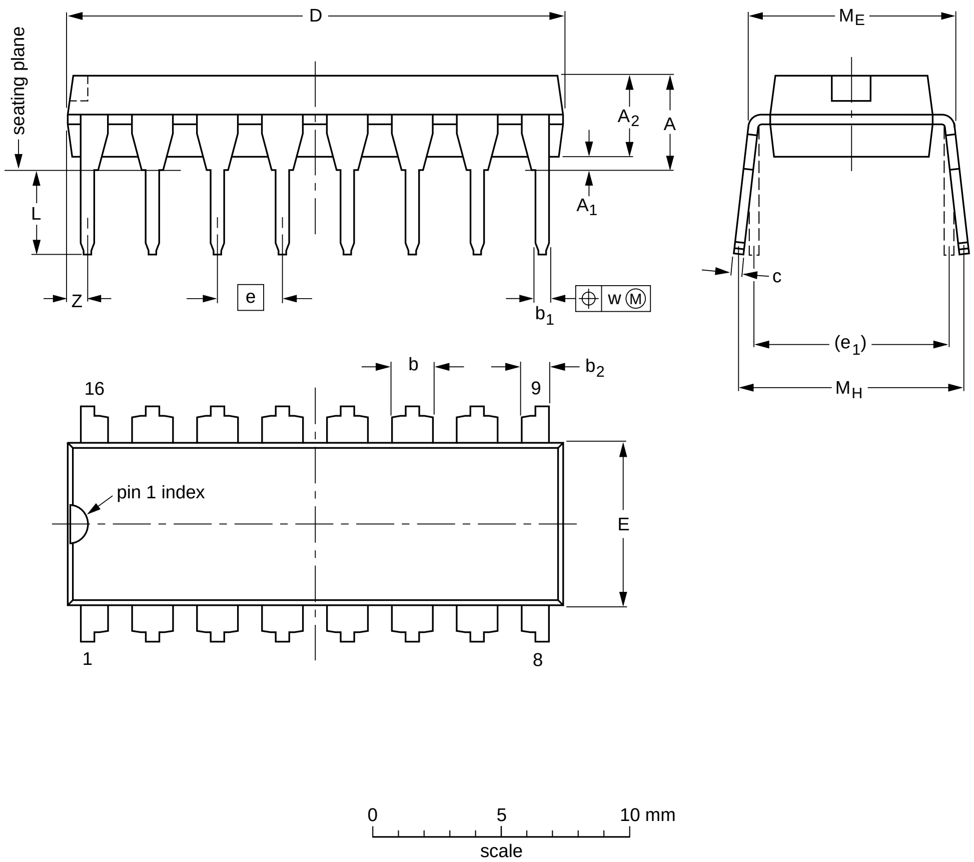
V_{CC} = 2.0 V to 6.0 V; T_{amb} = 25 °C.

For C_t curve: R_t = 100 kΩ; R2 = 200 kΩ.

Fig 17. RC oscillator frequency as a function of C_t

14. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

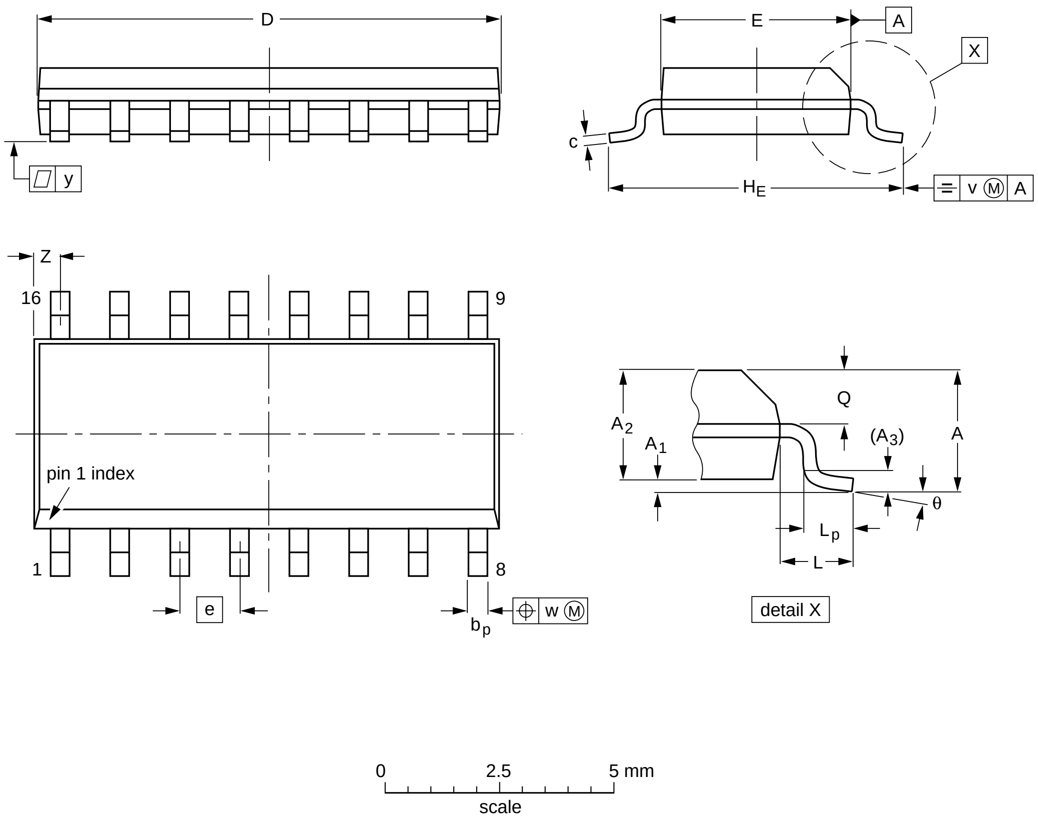
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 18. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

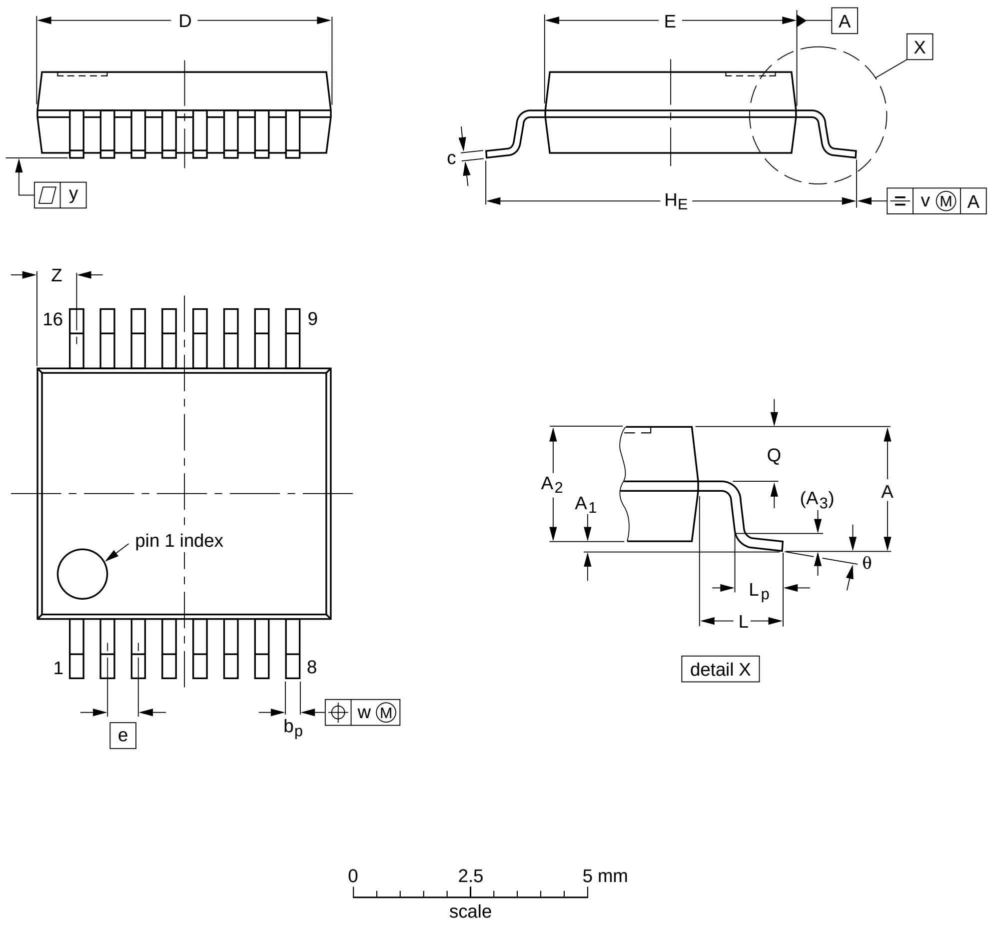
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

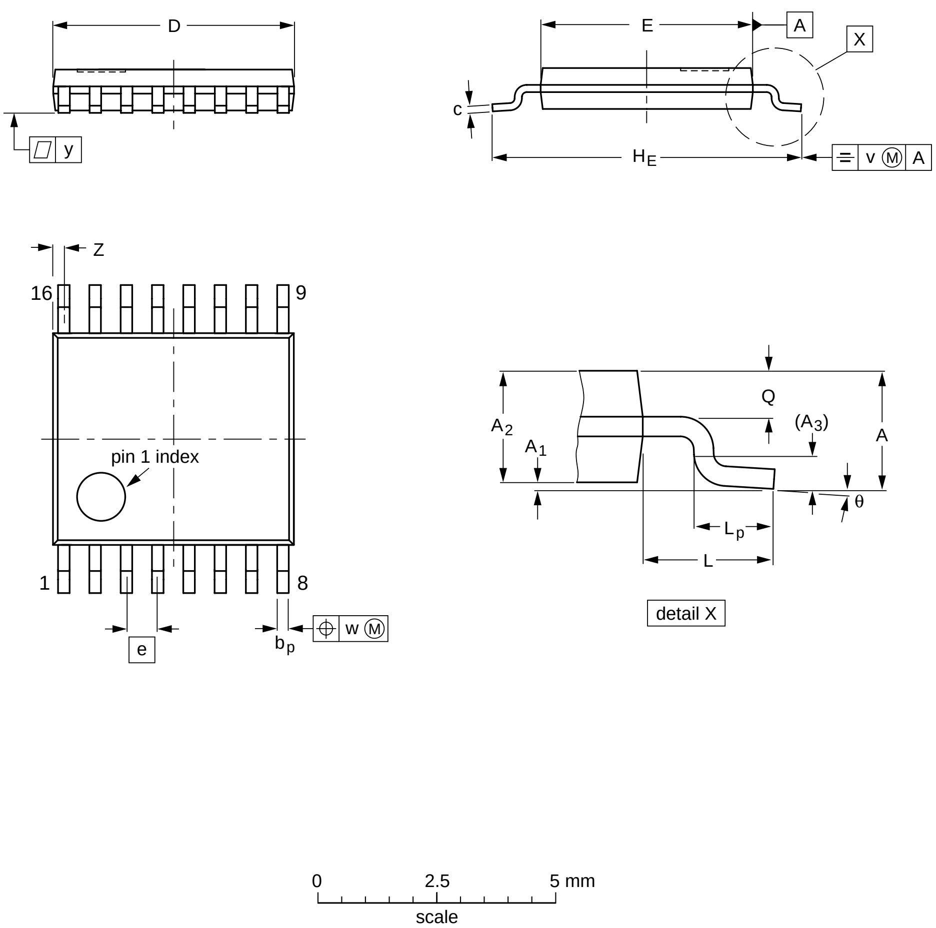
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

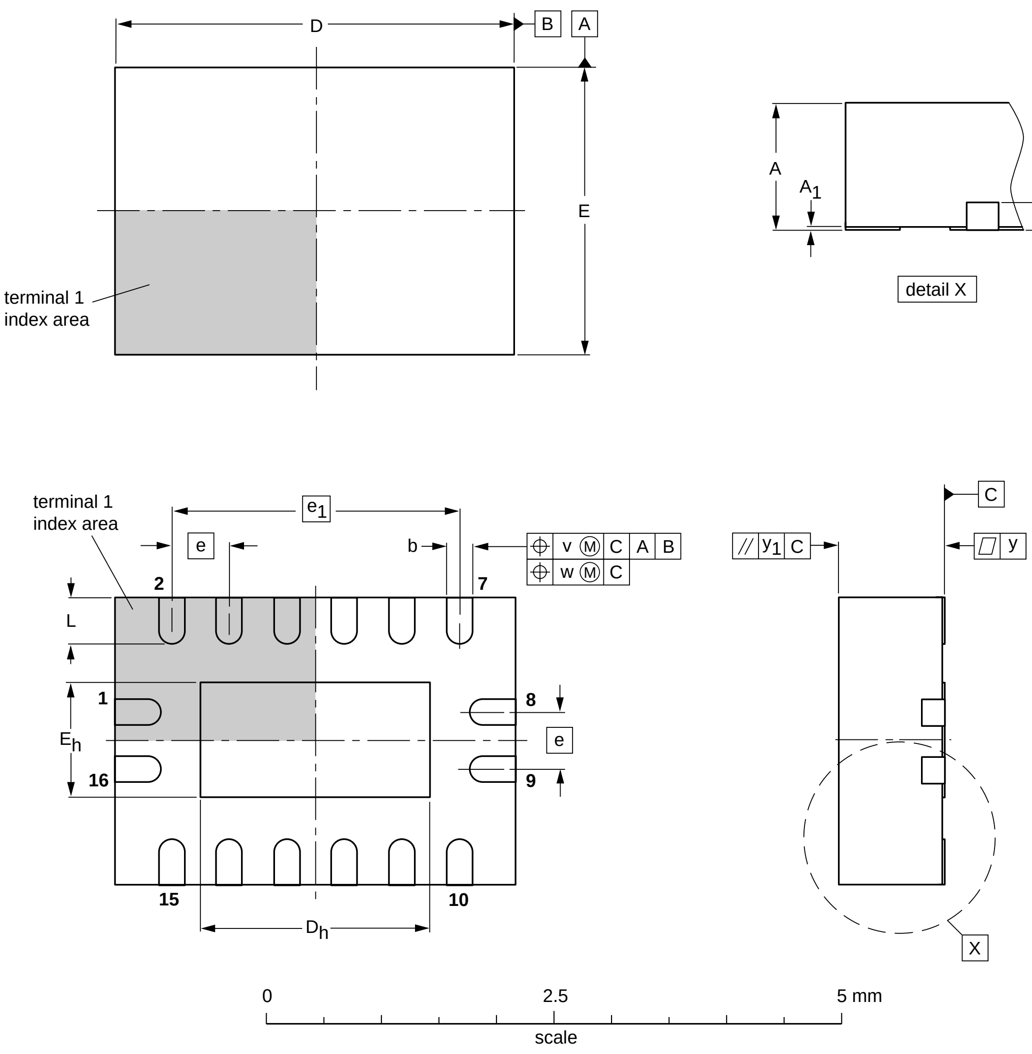
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 22. Package outline SOT763-1 (DHVQFN16)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4060_3	20080714	Product data sheet	-	74HC_HCT4060_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 4: DHVQFN16 package added. • Section 8: derating values added for DHVQFN16 package. • Section 14: outline drawing added for DHVQFN16 package.			
74HC_HCT4060_CNV_2	19970901	Product specification	-	-

17. Legal information

18. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

18.2 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

18.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

20. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 14 July 2008

Document identifier: 74HC_HCT4060_3