### 1.8V Drive Nch+SBD MOSFET

## QS5U34

## - Structure

Silicon N-channel MOSFET
Schottky Barrier DIODE

## - Features

1) The QS5U34 combines Nch MOSFET with a Schottky barrier diode in a single TSMT5 package.
2) Low on-state resistance with fast switching.
3) Low voltage drive ( 1.8 V ).
4) The Independently connected Schottky barrier diode has low forward voltage.

## - Applications

Load switch, DC / DC conversion

## -Packaging specifications

| Type | Package | Taping |
| :--- | :--- | :---: |
|  | Code | TR |
|  | Basic ordering unit (pieces) | 3000 |
| QS5U34 | $\bigcirc$ |  |

-Dimensions (Unit : mm)


## - Equivalent circuit



Transistors
-Absolute maximum ratings $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$

| Parameter |  | Symbol | Limits | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Drain-source voltage |  | V ${ }_{\text {dss }}$ | 20 | V |
| Gate-source voltage |  | Vass | 10 | V |
| Drain current | Continuous | ID | $\pm 1.5$ | A |
|  | Pulsed | ldp *1 | $\pm 3.0$ | A |
| Source current (Body diode) | Continuous | Is | 0.6 | A |
|  | Pulsed | Isp *1 | 2.4 | A |
| Channel temperature |  | Tch | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation |  | Pd *3 | 0.9 | W/ELEMENT |
| <Di> |  |  |  |  |
| Repetitive peak reverse voltage |  | VRM | 30 | V |
| Reverse voltage |  | $V_{\text {R }}$ | 20 | V |
| Forward current |  | $\mathrm{I}_{\mathrm{F}}$ | 0.5 | A |
| Forward current surge peak |  | IFSM *2 | 2.0 | A |
| Junction temperature |  | Tj | 150 | ${ }^{\circ} \mathrm{C}$ |
| Power dissipation |  | Pd *3 | 0.7 | W/ELEMENT |
| <MOSFET AND Di> |  |  |  |  |
| Total power dissipation |  | PD *3 | 1.25 | W / TOTAL |
| Range of Storage temperature |  | Tstg | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

*1 Pw $\leq 10 \mu \mathrm{~s}$, Duty cycle $\leq 1 \%$ *2 60Hz•1cyc. *3 Mounted on a ceramic board
-Electrical characteristics $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$
<MOSFET>

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Gate-source leakage | lass | - | - | 10 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{GS}}=10 \mathrm{~V} / \mathrm{V}_{\mathrm{DS}}=0 \mathrm{~V}$ |
| Drain-source breakdown voltage | $\mathrm{V}_{\text {(BR) }} \mathrm{DSS}$ | 20 | - | - | V | $\mathrm{I}_{\mathrm{D}}=1 \mathrm{~mA}, / \mathrm{V}_{\mathrm{GS}}=0 \mathrm{~V}$ |
| Zero gate voltage drain current | Idss | - | - | 1 | $\mu \mathrm{A}$ | V ${ }_{\text {ds }}=20 \mathrm{~V} / \mathrm{V}_{\mathrm{Gs}}=0 \mathrm{~V}$ |
| Gate threshold voltage | VGS (th) | 0.3 | - | 1.3 | V | $V_{D S}=10 \mathrm{~V} / \mathrm{ID}_{\mathrm{D}}=1 \mathrm{~mA}$ |
| Static drain-source on-state resistance | Rds (on)* | - | 130 | 180 | $\mathrm{m} \Omega$ | $\mathrm{I}_{\mathrm{D}}=1.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=4.5 \mathrm{~V}$ |
|  |  | - | 170 | 240 | $\mathrm{m} \Omega$ | $\mathrm{ld}=1.5 \mathrm{~A}, \mathrm{~V}_{\mathrm{Gs}}=2.5 \mathrm{~V}$ |
|  |  | - | 220 | 310 | $\mathrm{m} \Omega$ | $\mathrm{I}_{\mathrm{D}}=0.8 \mathrm{~A}, \mathrm{~V}_{\mathrm{GS}}=1.8 \mathrm{~V}$ |
| Forward transfer admittance | $\left\|\mathrm{Y}_{\text {fs }}\right\|^{*}$ | 1.6 | - | - | S | $\mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V}, \mathrm{l}=1.5 \mathrm{~A}$ |
| Input capacitance | Ciss | - | 110 | - | pF | $\begin{aligned} & \mathrm{V}_{\mathrm{DS}}=10 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{GS}}=0 \mathrm{~V} \\ & \mathrm{f}=1 \mathrm{MHz} \end{aligned}$ |
| Output capacitance | Coss | - | 18 | - | pF |  |
| Reverse transfer capacitance | Crss | - | 15 | - | pF |  |
| Turn-on delay time | $\mathrm{t}_{\text {d (on) }}$ * | - | 5 | - | ns | $\begin{aligned} & \hline \mathrm{ID}=1.0 \mathrm{~A} \\ & \mathrm{VDD} \fallingdotseq 10 \mathrm{~V} \\ & \mathrm{VGS}=4.5 \mathrm{~V} \\ & \mathrm{RL}=10 \Omega \\ & \mathrm{RG}=10 \Omega \end{aligned}$ |
| Rise time | tr | - | 5 | - | ns |  |
| Turn-off delay time | td (off) * | - | 20 | - | ns |  |
| Fall time | $\mathrm{tf}^{\text {f }}$ | - | 3 | - | ns |  |
| Total gate charge | $\mathrm{Q}_{\mathrm{g}}$ * | - | 1.8 | 2.5 | nC | $\begin{aligned} & \hline \mathrm{V}_{\mathrm{DD}} \fallingdotseq 10 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{GS}}=4.5 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{D}}=1.5 \mathrm{~A} \\ & \hline \end{aligned}$ |
| Gate-source charge | $\mathrm{Qgs}_{\text {s }}$ * | - | 0.3 | - | nC |  |
| Gate-drain charge | Qgd * | - | 0.3 | - | nC |  |

*Pulsed
<MOSFET>Body diode (source-drain)

| <MOSFET>Body diode (source-drain) |
| :--- |
| Forward voltage |

<Di>

| Forward voltage | $\mathrm{V}_{\mathrm{F}}$ | - | - | 0.36 | V | $\mathrm{I}_{\mathrm{F}=0.1 \mathrm{~A}}$ |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | - | - | 0.47 | V | $\mathrm{I}_{\mathrm{F}}=0.5 \mathrm{~A}$ |
| Reverse current | $\mathrm{I}_{\mathrm{R}}$ | - | - | 100 | $\mu \mathrm{~A}$ | $\mathrm{~V}_{\mathrm{R}}=20 \mathrm{~V}$ |

Transistors

## $\bullet$ Electrical characteristic curves

## <MOSFET>



Fig. 1 Typical Capacitance vs. Drain-Source Voltage


Fig. 2 Switching Characteristics


Fig. 3 Dynamic Input Characteristics


Fig. 4 Typical Transfer Characteristics


Fig. 7 Static Drain-Source
On-State Resistance
vs. Drain Current ( I )


Fig. 5 Static Drain-Source On-State Resistance vs. Gate-source Voltage


Fig. 6 Source Current vs.
Source-Drain Voltage


Fig. 8 Static Drain-Source
On-State Resistance
vs. Drain Current ( II )


Fig. 9 Static Drain-Source
On-State Resistance
vs. Drain Current ( III )


Fig. 10 Forward Temperature Characteristics


Fig. 11 Reverse Temperature Characteristics

## - Notice

1. SBD has a large reverse leak current compared to other type of diode. Therefore; it would raise a junction temperature, and increase a reverse power loss. Further rise of inside temperature would cause a thermal runaway.
This built-in SBD has low $\mathrm{V}_{\mathrm{F}}$ characteristics and therefore, higher leak current. Please consider enough the surrounding temperature, generating heat of MOSFET and the reverse current.
2. This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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