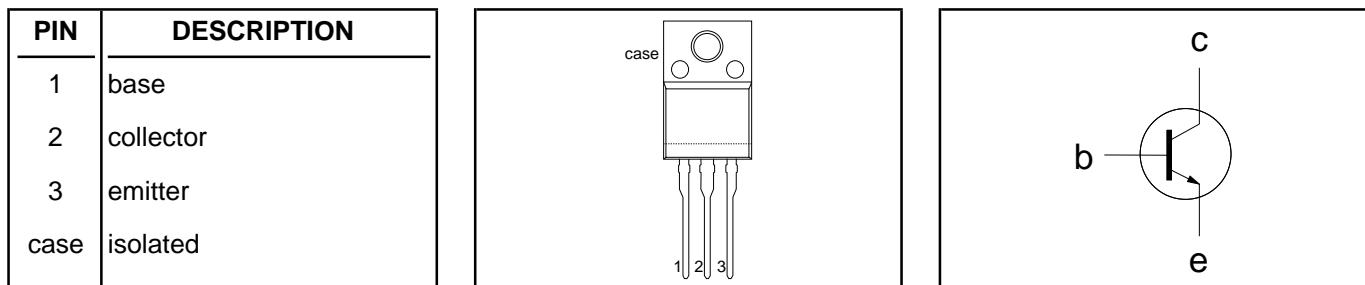


**Silicon Diffused Power Transistor****BUT11APX****GENERAL DESCRIPTION**

Enhanced performance, new generation, high-voltage, high-speed switching npn transistor in a plastic full-pack envelope intended for use in horizontal deflection circuits of colour television receivers. Features exceptional tolerance to base drive and collector current load variations resulting in a very low worst case dissipation.

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$V_{CESM}$	Collector-emitter voltage peak value	$V_{BE} = 0 \text{ V}$	-	1000	V
$V_{CBO}$	Collector-Base voltage (open emitter)		-	1000	V
$V_{CEO}$	Collector-emitter voltage (open base)		-	450	V
$I_C$	Collector current (DC)		-	5	A
$I_{CM}$	Collector current peak value		-	10	A
$P_{tot}$	Total power dissipation	$T_{hs} \leq 25 \text{ }^{\circ}\text{C}$	-	32	W
$V_{CEsat}$	Collector-emitter saturation voltage		-	1.5	V
$I_{Csat}$	Collector saturation current		3.5	-	A
$t_f$	Fall time	$I_{Csat}=2.5\text{A}, I_{B1}=0.5\text{A}, I_{B2}=0.8\text{A}$	145	160	ns

**PINNING - SOT186A****PIN CONFIGURATION****SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CESM}$	Collector to emitter voltage	$V_{BE} = 0 \text{ V}$	-	1000	V
$V_{CEO}$	Collector to emitter voltage (open base)		-	450	V
$V_{CBO}$	Collector to base voltage (open emitter)		-	1000	V
$I_C$	Collector current (DC)		-	5	A
$I_{CM}$	Collector current peak value		-	10	A
$I_B$	Base current (DC)		-	2	A
$I_{BM}$	Base current peak value		-	4	A
$P_{tot}$	Total power dissipation	$T_{hs} \leq 25 \text{ }^{\circ}\text{C}$	-	32	W
$T_{stg}$	Storage temperature		-65	150	°C
$T_j$	Junction temperature		-	150	°C

**THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{thj-hs}$	Junction to heatsink	with heatsink compound	-	3.95	K/W
$R_{thj-a}$	Junction to ambient	in free air	55	-	K/W

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**ISOLATION LIMITING VALUE & CHARACTERISTIC** $T_{hs} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{isol}$	R.M.S. isolation voltage from all three terminals to external heatsink	$f = 50-60 \text{ Hz}$ ; sinusoidal waveform; $R.H. \leq 65\%$ ; clean and dustfree	-		2500	V
$C_{isol}$	Capacitance from T2 to external heatsink	$f = 1 \text{ MHz}$	-	10	-	pF

**STATIC CHARACTERISTICS** $T_{hs} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CES}$	Collector cut-off current <sup>1</sup>	$V_{BE} = 0 \text{ V}$ ; $V_{CE} = V_{CESMmax}$	-	-	1.0	mA
$I_{CES}$		$V_{BE} = 0 \text{ V}$ ; $V_{CE} = V_{CESMmax}$ ; $T_j = 125^\circ\text{C}$	-	-	2.0	mA
$I_{EBO}$	Emitter cut-off current	$V_{EB} = 9 \text{ V}$ ; $I_C = 0 \text{ A}$	-	-	10	mA
$V_{CEO}sust$	Collector-emitter sustaining voltage	$I_B = 0 \text{ A}$ ; $I_C = 100 \text{ mA}$ ; $L = 25 \text{ mH}$	450	-	-	V
$V_{CEsat}$	Collector-emitter saturation voltages	$I_C = 3.0 \text{ A}$ ; $I_B = 0.6 \text{ A}$	-	0.25	1.5	V
$V_{BEsat}$	Base-emitter saturation voltage	$I_C = 2.5 \text{ A}$ ; $I_B = 0.33 \text{ A}$	-	-	1.3	V
$h_{FE}$	DC current gain	$I_C = 5 \text{ mA}$ ; $V_{CE} = 5 \text{ V}$	10	22	35	
$h_{FE}$		$I_C = 500 \text{ mA}$ ; $V_{CE} = 5 \text{ V}$	14	25	35	
$h_{FEsat}$		$I_C = 2.5 \text{ A}$ ; $V_{CE} = 5 \text{ V}$	10	13.5	17	
$h_{FEsat}$		$I_C = 3.5 \text{ A}$ ; $V_{CE} = 5 \text{ V}$	8	10	12	

**DYNAMIC CHARACTERISTICS** $T_{hs} = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$t_{on}$	Switching times (resistive load)	$I_{Csat} = 2.5 \text{ A}$ ; $I_{B1} = -I_{B2} = 0.5 \text{ A}$ ; $R_L = 75 \text{ ohms}$ ; $V_{BB2} = 4 \text{ V}$			
$t_s$	Turn-on time		0.5	0.7	$\mu\text{s}$
$t_s$	Turn-off storage time		3.3	4	$\mu\text{s}$
$t_f$	Turn-off fall time		0.33	0.45	$\mu\text{s}$
$t_s$	Switching times (inductive load)	$I_{Csat} = 2.5 \text{ A}$ ; $I_{B1} = 0.5 \text{ A}$ ; $L_B = 1 \mu\text{H}$ ; $-V_{BB} = 5 \text{ V}$			
$t_f$	Turn-off storage time		1.4	1.6	$\mu\text{s}$
$t_s$	Turn-off fall time		145	160	ns
$t_s$	Switching times (inductive load)	$I_{Csat} = 2.5 \text{ A}$ ; $I_{B1} = 0.5 \text{ A}$ ; $L_B = 1 \mu\text{H}$ ; $-V_{BB} = 5 \text{ V}$ ; $T_j = 100^\circ\text{C}$			
$t_f$	Turn-off storage time		1.7	1.9	$\mu\text{s}$
$t_f$	Turn-off fall time		160	200	ns

<sup>1</sup> Measured with half sine-wave voltage (curve tracer).

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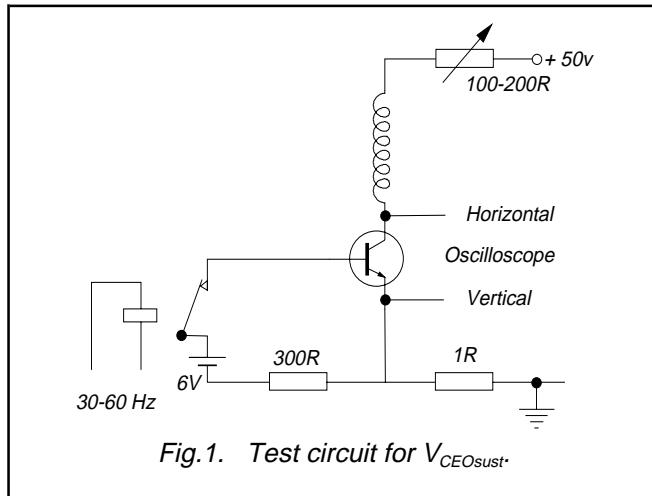
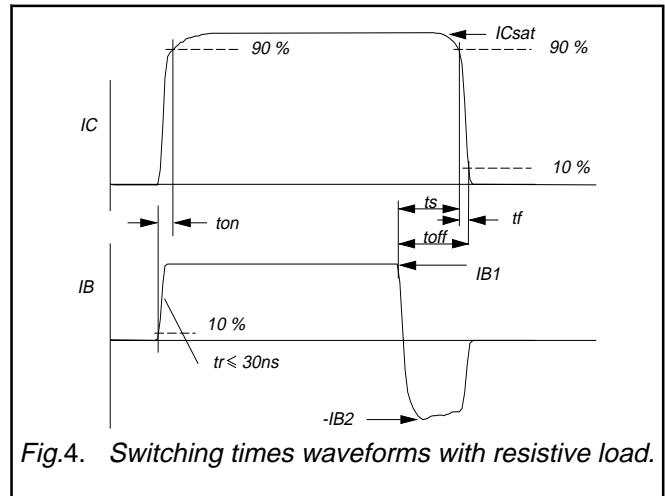
Fig.1. Test circuit for  $V_{CEO}$  sust.

Fig.4. Switching times waveforms with resistive load.

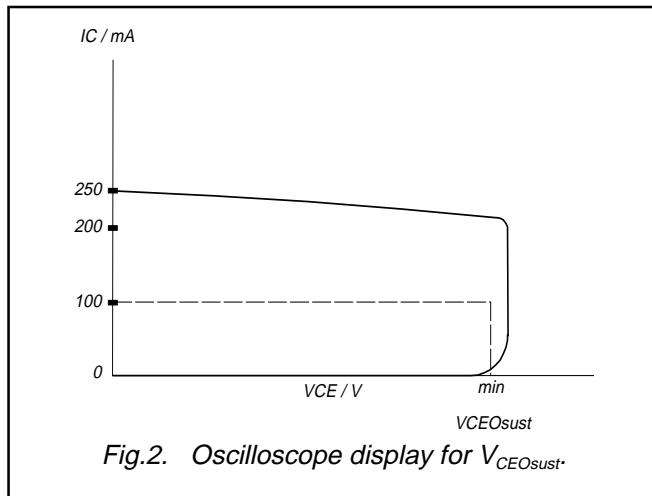
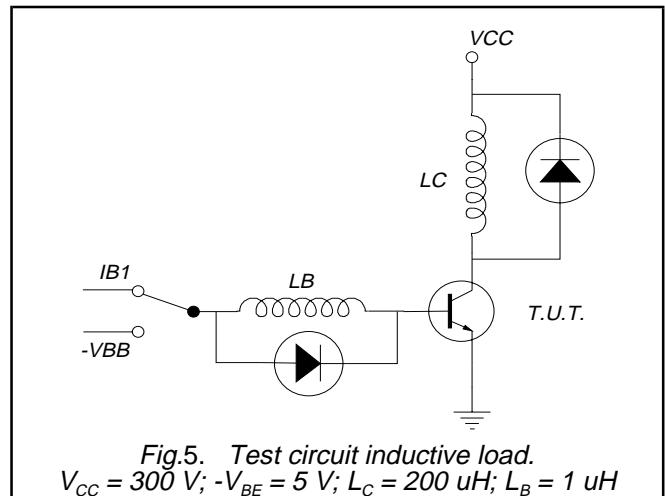
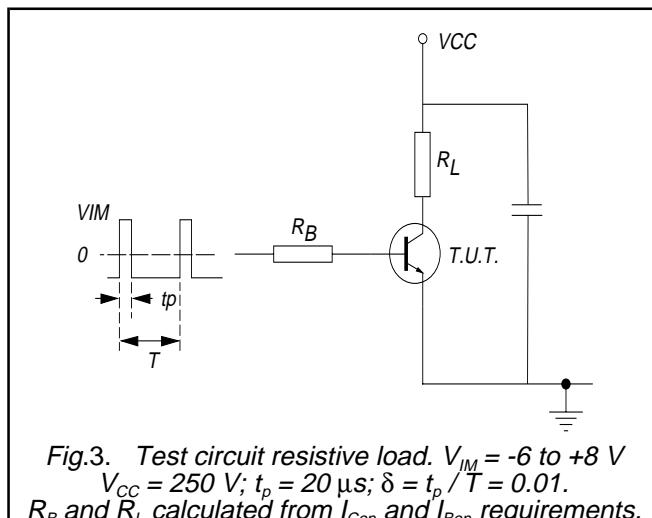
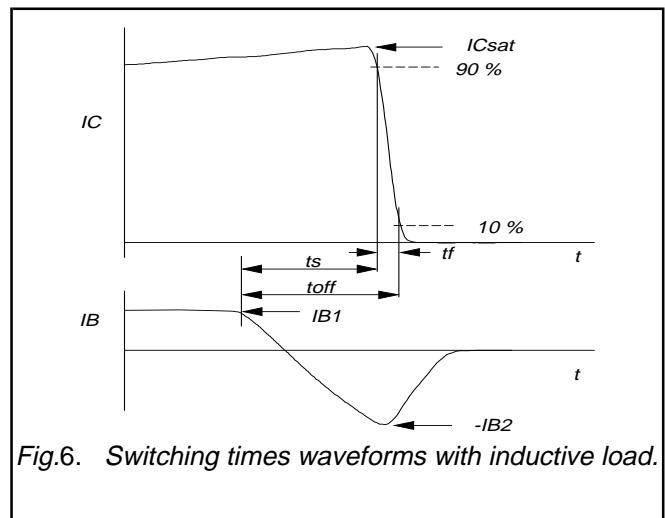
Fig.2. Oscilloscope display for  $V_{CEO}$  sust.Fig.5. Test circuit inductive load.  
 $V_{CC} = 300\text{ V}$ ;  $-V_{BE} = 5\text{ V}$ ;  $L_C = 200\text{ }\mu\text{H}$ ;  $L_B = 1\text{ }\mu\text{H}$ Fig.3. Test circuit resistive load.  $V_{IM} = -6$  to  $+8\text{ V}$   
 $V_{CC} = 250\text{ V}$ ;  $t_p = 20\text{ }\mu\text{s}$ ;  $\delta = t_p/T = 0.01$ .  
 $R_B$  and  $R_L$  calculated from  $I_{Con}$  and  $I_{Bon}$  requirements.

Fig.6. Switching times waveforms with inductive load.

## Silicon Diffused Power Transistor

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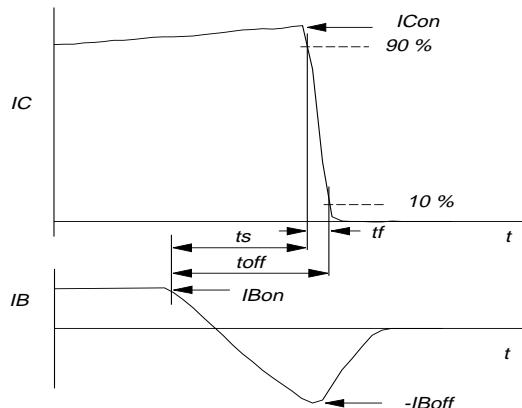
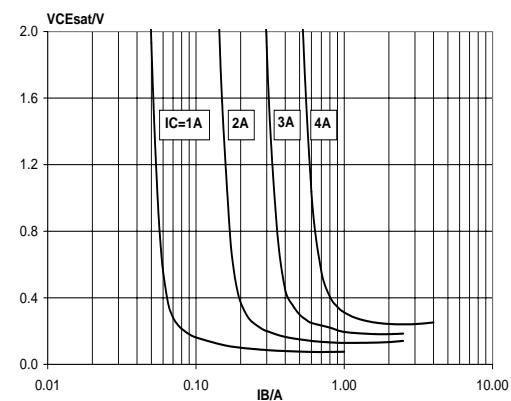
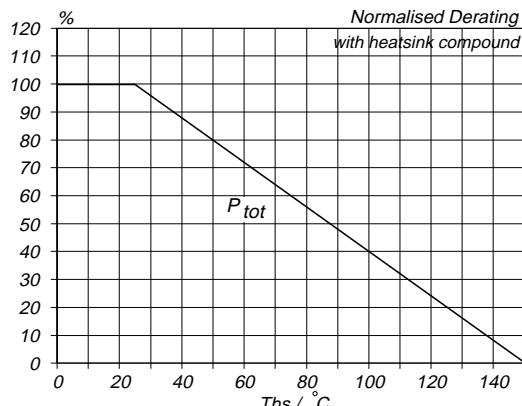
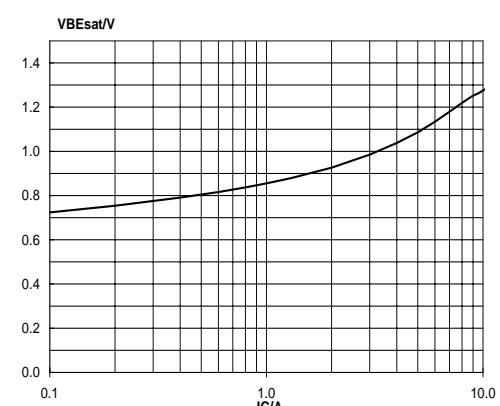
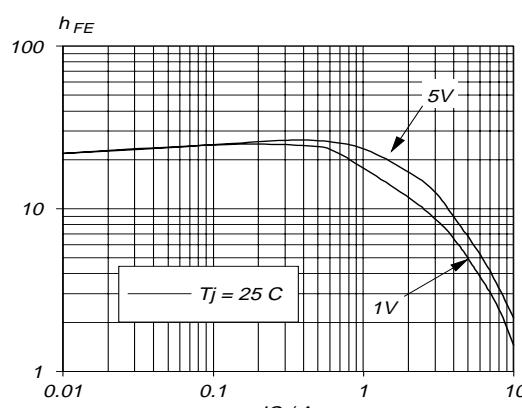
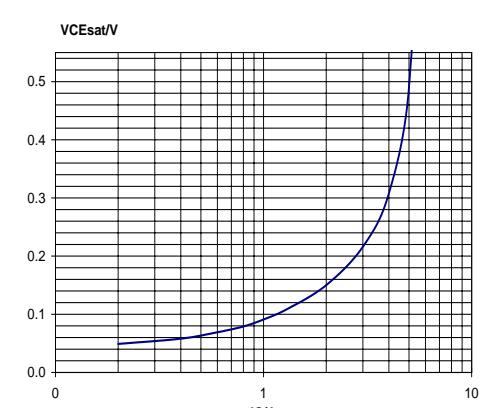


Fig.7. Switching times waveforms with inductive load.

Fig.10. Collector-Emitter saturation voltage.  
Solid lines = typ values,  $V_{CEsat} = f(IB)$ ;  $T_j = 25^\circ C$ .Fig.8. Normalised power dissipation.  
 $PD\% = 100 \cdot PD/PD_{25^\circ C} = f(T_{hs})$ Fig.11. Base-Emitter saturation voltage.  
Solid lines = typ values,  $V_{BEsat} = f(IC)$ ; at  $IC/IB = 4$ .Fig.9. Typical DC current gain.  $h_{FE} = f(IC)$   
parameter  $V_{CE}$ Fig.12. Collector-Emitter saturation voltage.  
Solid lines = typ values,  $V_{CEsat} = f(IC)$ ; at  $IC/IB = 4$ .

## Silicon Diffused Power Transistor

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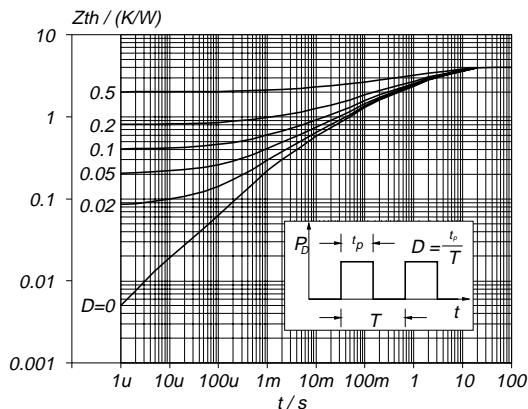


Fig.13. Transient thermal impedance.  
 $Z_{th(j-hs)} = f(t)$ ; parameter  $D = t_p/T$

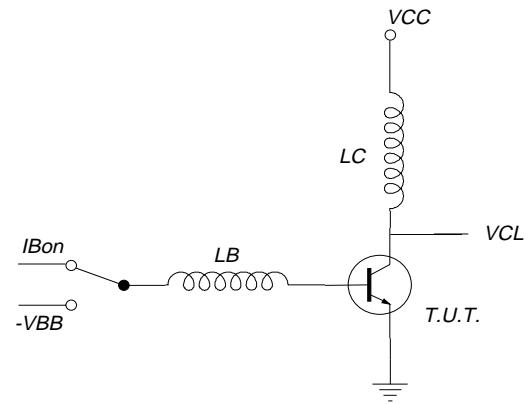


Fig.15. Test circuit RBSOA.  $V_{cl} \leq 1000V$ ;  $V_{cc} = 150V$ ;  
 $V_{BB} = -5V$ ;  $L_B = 1\mu H$ ;  $L_c = 200\mu H$

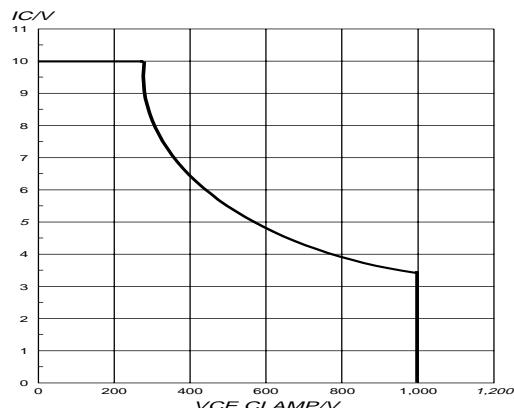
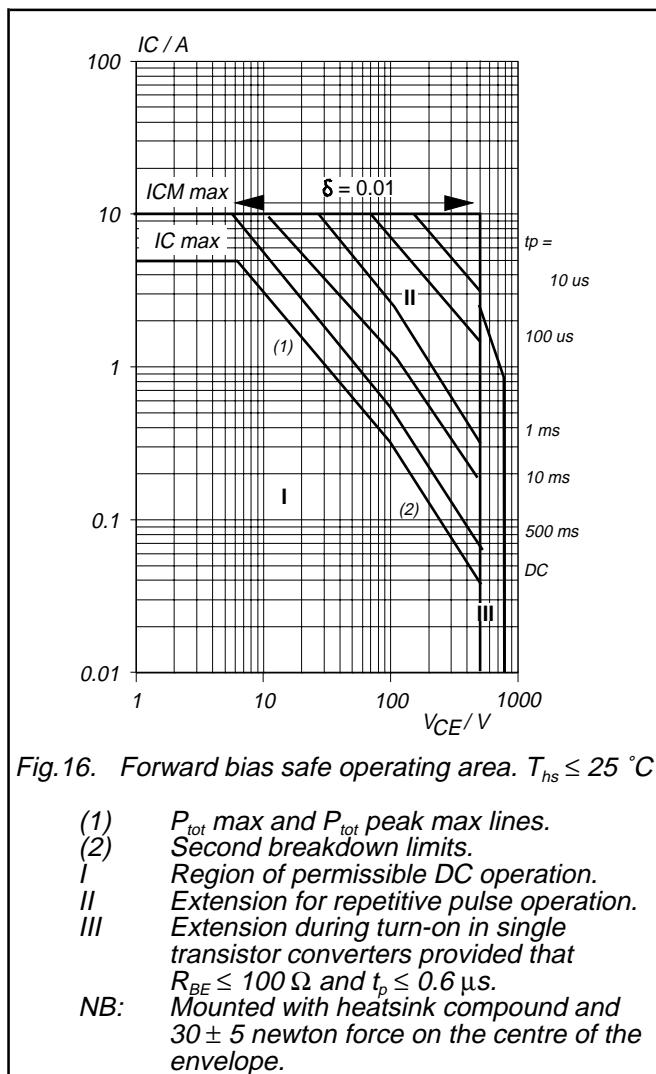


Fig.14. Reverse bias safe operating area.  $T_j \leq T_{j\max}$

## Silicon Diffused Power Transistor

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**MECHANICAL DATA***Dimensions in mm*

Net Mass: 2 g

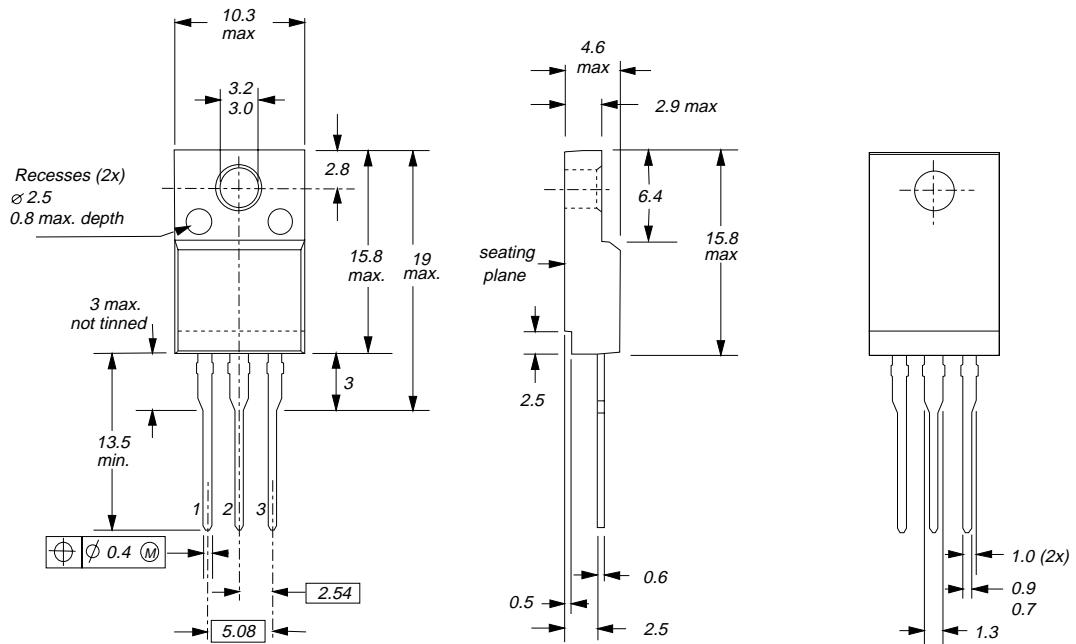


Fig.17. SOT186A; The seating plane is electrically isolated from all terminals.

**Notes**

1. Refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".

**Silicon Diffused Power Transistor****BUT11APX****DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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