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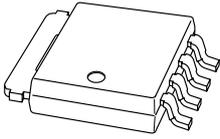
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Kind regards,

Team Nexperia



# PH4840S

## N-channel TrenchMOS intermediate level FET

Rev. 02 — 6 November 2006

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Low thermal resistance
- Low threshold voltage
- SO8 equivalent area footprint
- Low on-state resistance

### 1.3 Applications

- DC-to-DC converters
- Portable appliances
- DC motor drives
- Switched-mode power supplies
- Notebook computers

### 1.4 Quick reference data

- $V_{DS} \leq 40$  V
- $R_{DS(on)} \leq 4.1$  m $\Omega$
- $I_D \leq 94.5$  A
- $P_{tot} \leq 62.5$  W

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

**SOT669 (LFPACK)**

### 3. Ordering information

**Table 2. Ordering information**

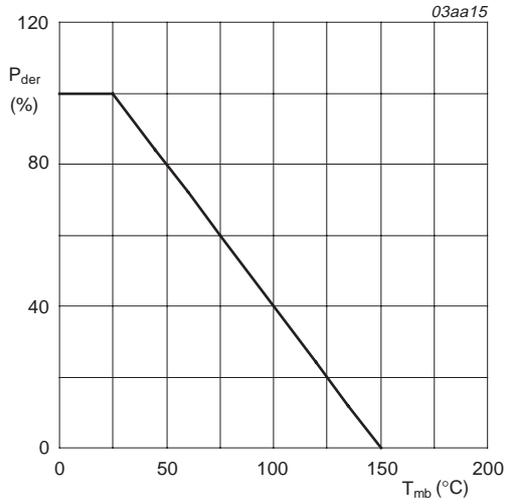
Type number	Package		Version
	Name	Description	
PH4840S	LFPAK	plastic single-ended surface-mounted package; 4 leads	SOT669

### 4. Limiting values

**Table 3. Limiting values**

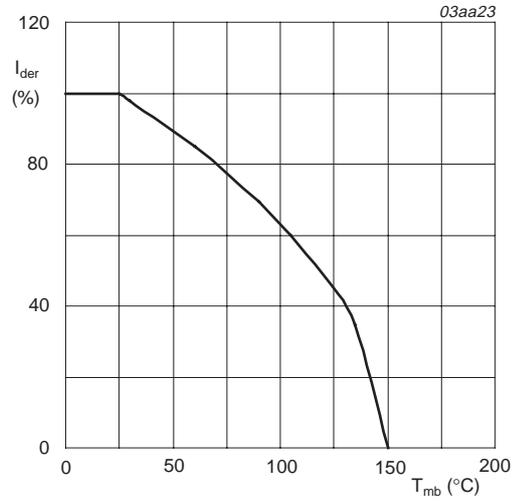
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	40	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	94.5	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	59.5	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	283	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	150	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 51\text{ A}$ ; $t_p = 0.21\text{ ms}$ ; $V_{DS} \leq 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	250	mJ



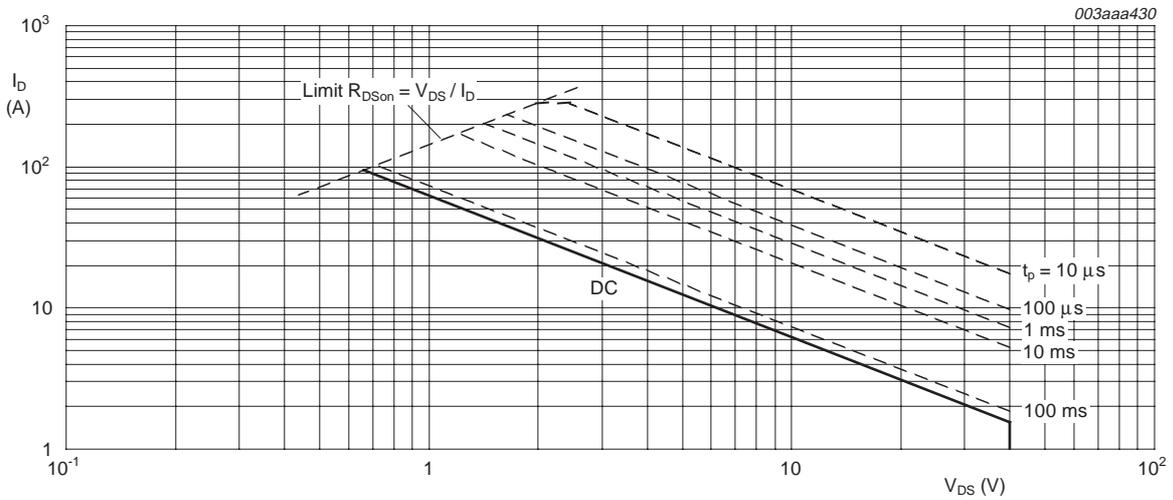
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 10\text{ V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

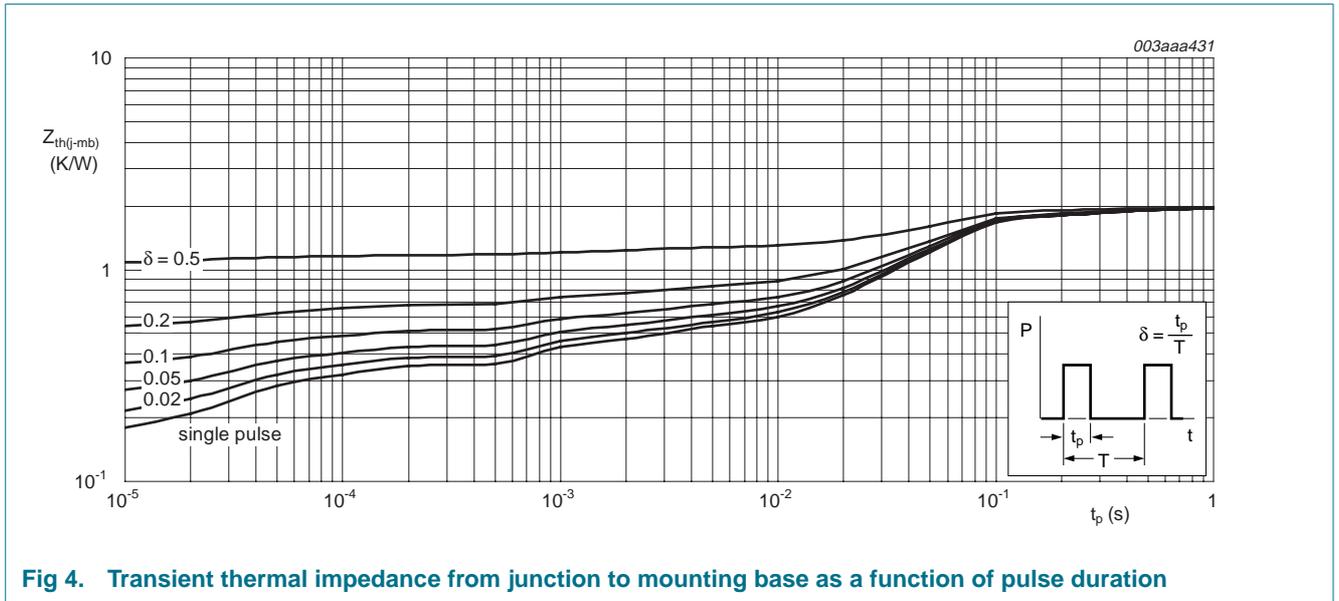


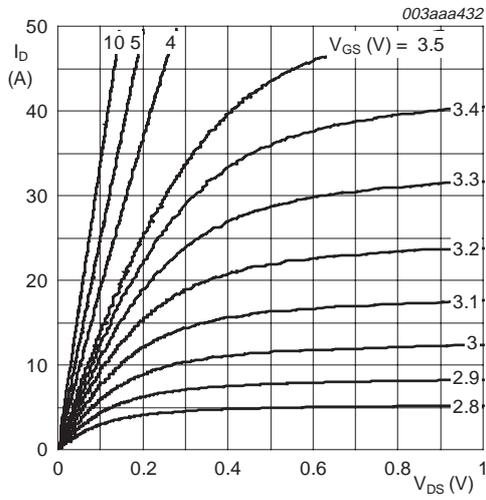
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

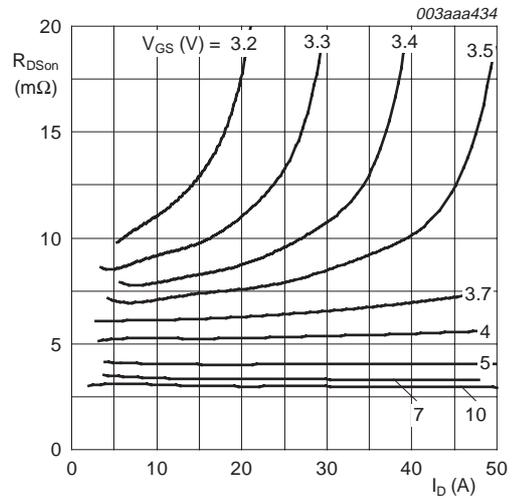
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ °C}$	1	2	3	V
		$T_j = 150\text{ °C}$	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	0.06	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 25\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	3.5	4.1	m $\Omega$
		$T_j = 150\text{ °C}$	-	5.6	7.0	m $\Omega$
		$V_{GS} = 7\ \text{V}; I_D = 25\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	3.85	4.8	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 30\ \text{A}; V_{DS} = 32\ \text{V}; V_{GS} = 10\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	67	-	nC
$Q_{GS}$	gate-source charge		-	8.6	-	nC
$Q_{GD}$	gate-drain charge		-	16	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 10\ \text{V}; f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	3660	-	pF
$C_{oss}$	output capacitance		-	877	-	pF
$C_{rss}$	reverse transfer capacitance		-	454	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\ \text{V}; I_D = 25\ \text{A}; V_{GS} = 10\ \text{V}$ ; $R_G = 4.7\ \Omega$	-	21	-	ns
$t_r$	rise time		-	35	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
$t_f$	fall time		-	31	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\ \text{A}; V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\ \text{A}; di_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	46	-	ns



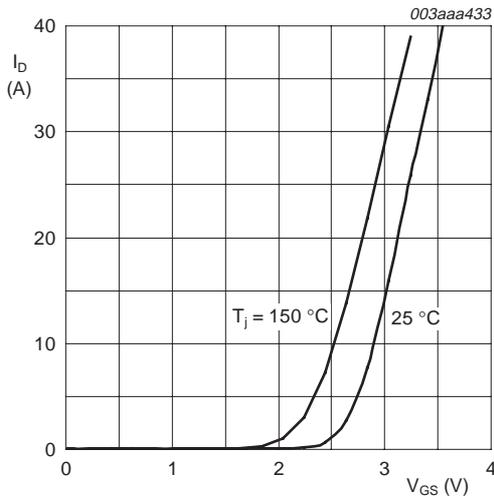
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



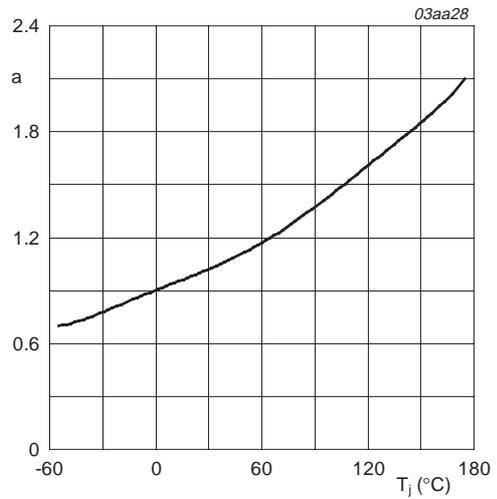
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



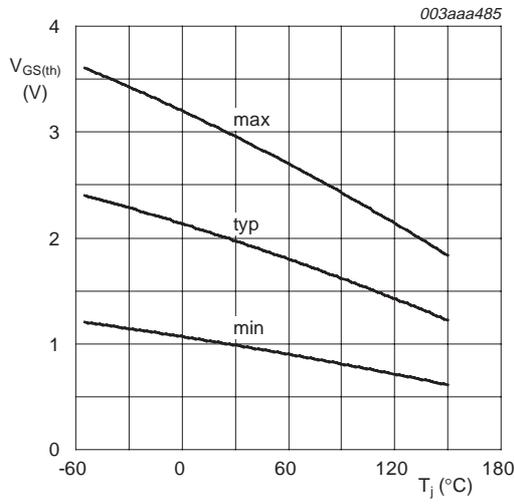
$T_j = 25\text{ }^\circ\text{C}$  and 150  $^\circ\text{C}$ ;  $V_{DS} > I_b \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



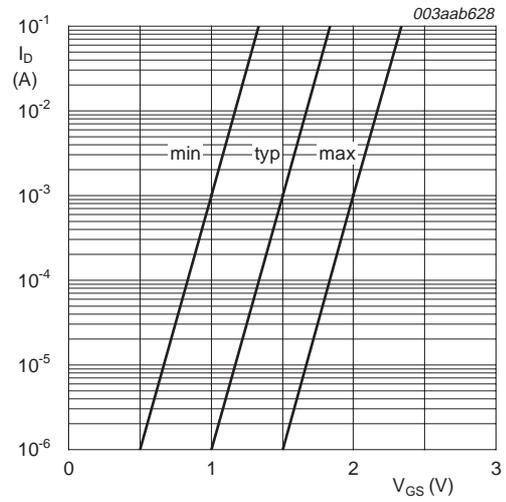
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



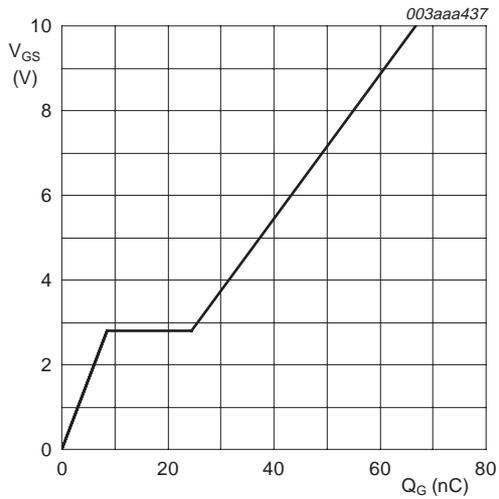
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 30 \text{ A}; V_{DS} = 32 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

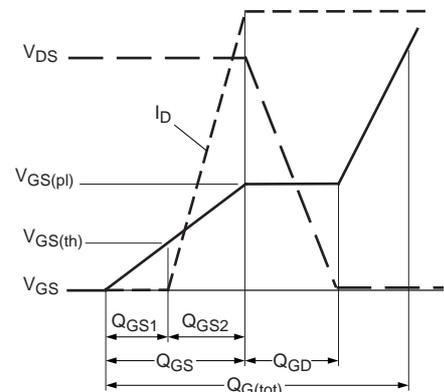
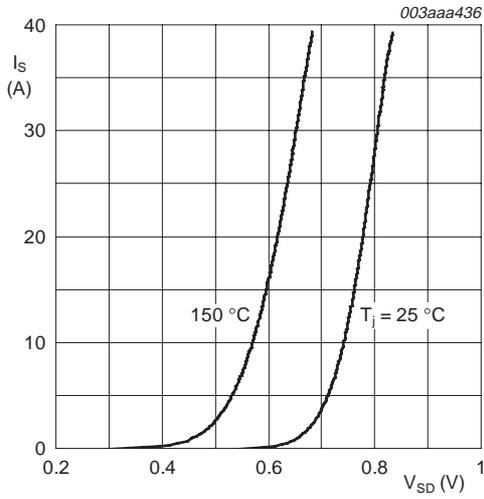
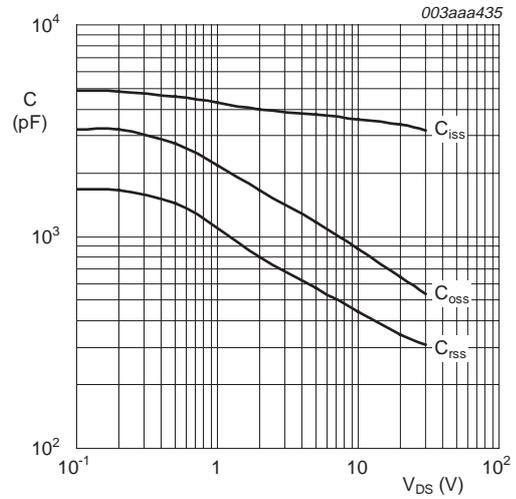


Fig 12. Gate charge waveform definitions



$T_j = 25\text{ °C}$  and  $150\text{ °C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



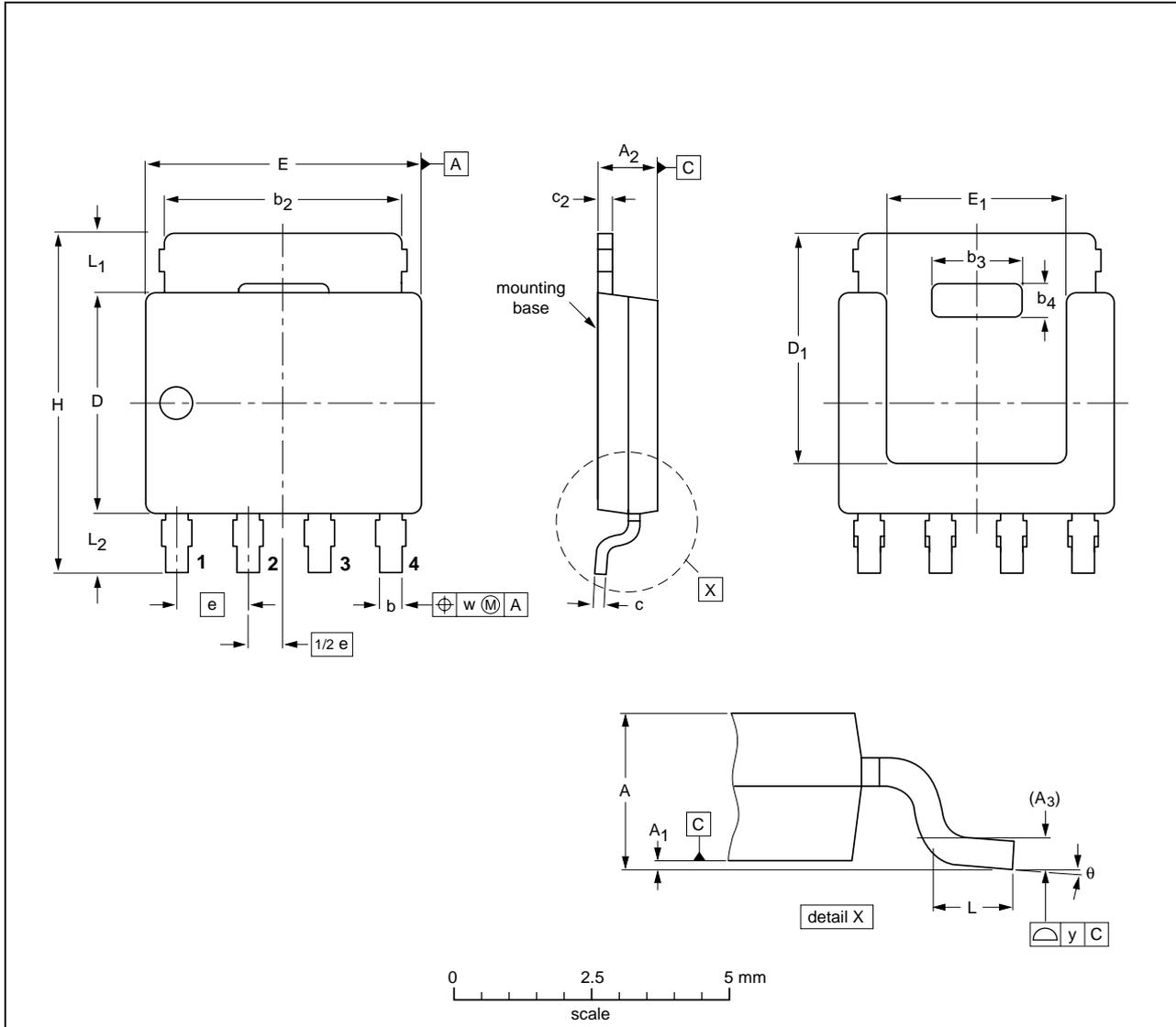
$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT669		MO-235			04-10-13 06-03-16

Fig 15. Package outline SOT669 (LPAK)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH4840S_2	20061106	Product data sheet	-	PH4840S-01
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
PH4840S-01 (9397 750 12814)	20040304	Preliminary data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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## 11. Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Limiting values</b> .....	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> .....	<b>4</b>
<b>6</b>	<b>Characteristics</b> .....	<b>5</b>
<b>7</b>	<b>Package outline</b> .....	<b>9</b>
<b>8</b>	<b>Revision history</b> .....	<b>10</b>
<b>9</b>	<b>Legal information</b> .....	<b>11</b>
9.1	Data sheet status .....	11
9.2	Definitions .....	11
9.3	Disclaimers .....	11
9.4	Trademarks .....	11
<b>10</b>	<b>Contact information</b> .....	<b>11</b>
<b>11</b>	<b>Contents</b> .....	<b>12</b>

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