# SYNCHRONOUS SEPARATOR WITH AFC

## ■ GENERAL DESCRIPTION

The **NJM2257** excutes Horizontal and Vertical synchronous signal separation, and odd / even field signal detection, from composit video signals.

Built-in 1 / 2 fH Killer Function circuit can make stabilization of the Horizontal signal oscillation output during the vertical period.

## FEATURES

- Operating Voltage (+4.5 to +5.3V)
- Internal AFC circuit (Horizontal sync. signal.)
- Internal 1 / 2 fH Killer Function
- AFC output Pulse Delay time is Adjustable
- Vertical synchronous pulse width is Adjustable
- Internal Field Discrlainat Function
- Package Outline DIP16, DMP16
- Bipolar Technology

## ■ APPLICATION

• VTR, TV, AV components etc.

#### BLOCK DIAGRAM



PACKAGE OUTLINE



NJM2257D

NJM2257M

C Sync OUT VIDEO IN 8 16 13 Vertical symchronizing Symchroonizing Vertical 14 signal separator 1 synchronizing Signal separaror Signal generator vd out Field 15 discrlainator FD OUT 1/321/2 CN 2 divider killer 32fH AFC HD phase 12 VCO detector pulse generator AFC HD OUT 3 9 4 5 6 10 11 v. HD OUT GND

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	SYMBOL	RATINGS	UNIT	
Supply Voltage	V <sup>+</sup>	+7	V	
Power Dissipation	P <sub>D</sub>	(DIP16) 500 (DMP16) 350	mW mW	
Operating Temperature Range	T <sub>opr</sub>	-20 to +75	C°	
Storage Temperature Range	T <sub>stg</sub>	- 40 to +125	C°	

PARAMETER		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiessent Current		l <sub>Q</sub>		-	23.0	30.0	mA
AFC Free Run Frequency		f <sub>OH</sub>		15.54	15.74	15.94	KHz
	none adjust	T <sub>AHW1</sub>	SW=a	3.5	4.0	4.5	μS
AFC HD pulse width	adjust	T <sub>AHW2</sub>	SW=b	2.5	4.0	5.5	
AFC HD Delet Time		T <sub>AHD</sub>		-1.0	0.5	2.0	μS
AFC Lock Range		$\Delta f_{HL}$		500	700	-	Hz
AFC Cap Charange		$\Delta f_{HP}$		400	600	-	Hz
AFC Output Voltage	Н	V <sub>HAH</sub>		4.0	4.2	-	v
AFC Oulput Voltage	L	VHAL		-	0	0.1	v
Sync Sepa Sync. Separation L	_evel	V <sub>HSR</sub>		-	0.16	0.18	V
Sync Sepa Delay Time		T <sub>HCD</sub>		0.05	0.20	0.35	μS
Sync Sepa Output Voltage	Н	$V_{\text{HCH}}$		4.0	4.2	-	- V
Sync Sepa Oulpul Vollage	L	V <sub>HCL</sub>		-	0	0.1	
HD Output Palth Width		T <sub>HPW</sub>		4.0	5.5	7.0	μS
HD Output Delay Time		T <sub>HPD</sub>		0.35	0.6	0.8	μS
HD Output Voltage	Н	V <sub>HfH</sub>		4.0	4.2	-	v
HD Oulput Vollage	L	$V_{\text{HfL}}$		-	0	0.1	v
V Sync Palth Width		$V_{VW}$		170	190	210	μS
V Sync Delay Time		T <sub>VD</sub>		7.0	10.0	13.0	μS
V Svac Output Voltage	Н	T <sub>VH</sub>		4.0	4.2	-	- V
V Sync Output Voltage	L	V <sub>VL</sub>		-	0	0.1	
Field Distinction Dolay Time	odd	T <sub>FOD</sub>		246	256	266	
Field Distinction Delay Time	even	T <sub>FED</sub>		216	226	236	μS
Fideld Distinction Output	odd	V <sub>FOR</sub>		4.0	4.2	-	v
Voltage	even	V <sub>FER</sub>		-	0	0.1	7 <sup>v</sup>

#### ■ APPLICATION CIRCUIT



#### APPLICATION NOTES

It shows the characteristics by changing of the following resistor.

- The resistance between 9 Pin and GND
  - High resistance AFC HD pulse is wide
  - Low resistance AFC HD pulse is narrow
- The resistor between 9 Pin and  $V^{+}$

At the resistor is 100  $\!\Omega$ . AFC HD Delay adjustment is off, and AFC HD output width is 4  $\!\mu s$  (typ.)

- The resistor between 9 Pin and GND is fundamentally  $14.2k\Omega$ , because the purpose of this resistor is pulse width adjusts  $4\mu$ s.
- The resistor between 10 Pin and GND
  - High resistance AFC HD Delay time gains
  - Low resistance AFC HD Delay time loses
- The resistor between 13 Pin and GND
  - High resistance Vsync pulse is wide
  - Low resistance Vsync pulse is narrow
- The resistor joind 2 Pin

Please adjust the wide of following W is from 33  $\mu$ s to 37  $\mu$ s (W = - (C·R)In0.5)



# Fig 11/OPULSE



PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	VIDEO-IN	Composit Video Signal Input	
2	MM-HT	HD & FD puse are Controlled by setling mono multi	
3	HD-OUT	1 / 2 f <sub>H</sub> Killer D Output	3 3 777
4	VCO-OUT	VCO Output is to be given to Ceramic Oscillator	
5	VCO-FILTER 1	Decide the Volume to be transfered shall by decided of Ceramic Oscillator. (90°late)	

# ■ TERMINAL EXPLANATION

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PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
6	VCO-FILTER 2	Decide the Volume to be transfered shall by decided of Cramic Oscillator. (90°late)	3.3k
7	L. P. F	L. P. F. of AFC	
8	V <sup>+</sup>	Supply Voltage	
9	VR-1	AFC-HD Output Can be adjusted by putting resistor between 9 to GND (9 to V <sub>CC</sub> no adjustment). The pulse width cam be adjusted by making changeable of resister (Adjusting mode)	9
10	VR-2	AFC-HD Output delay adjustment by putting 10 pin resister changeable at 9 pin ajustment mode.	10 10 10 10 10 12. 6k
11	GND	Ground	

PIN NO.	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
12	AFC, HD-OUT	AFC-HD Output	12 15k
13	MM-VT	Pulse Width of Vsync-OUT is adjusted by setting mono multi time constant.	
14	Vsync-OUT	Vertical Synchronous Signal Output.	14 20k
15	FD-OUT discrimination	Field Distiniction Signal Output.	15 20k
16	Csyne-OUT	Synchronous Separation Output	16 7/7

# ■ TERMINAL EXPLANATION

## ■ PIN FUNCTION

PIN NO.	FUNCTION BLOCK	OPERATIONAL DESCRIPTION	NOTE	
1)Pin	Signal Input	Video Signal input	Sync tip clump	
2)Pin	HD pulse control	HD pulse and FD pulse control by time constant of CR		
3 Pin	HD pulse output	$1/2  f_H$ killer HD pulse output	In a period of vertical synchronizing, a $f_{\rm H}$ is converted to $f_{\rm H}$	
(4)Pin	Oscillation of 503KHz by a ceramic			
5 Pin	AFC Oscillation	oscillator, and divided by 32 to get down		
6 Pin		to 15.74KHz		
7 Pin	AFC control	Leg Lead filter for phase detection		
8 Pin	V <sub>CC</sub>	V <sub>cc</sub>		
9Pin	AFC HD output Switch (AFC HD pulse width adjustment)	The case that R is connected between 9pin and V <sub>CC</sub> Fixed output The case that R is connected between 9pin and GNDAdjustable AFC HD Delay Mode	High Resistance $\rightarrow$ Wide pulse width Low Resistance $\rightarrow$ Narrow pulse width	
10 Pin	AFC HD Delay adjustment	The case that R is connected between 9pin and GNDAdjustable AFC HD Delay output	High Resistance $\rightarrow$ AFC HD Delay time gains Low Resistance $\rightarrow$ AFC HD Delay time loses	
(11) Pin	GND	GND		
(12) Pin	AFC HD output	AFC HD pulse output	Positive polarity	
(13) Pin	VD pulse width adujstment	VD pulse width control by time constant of CR		
(14) Pin	VD output	Vertical synchronizing signal output	Positive polarity	
(15) Pin	FD output	Field discriminating signal output	odd field $\rightarrow$ High Output even field $\rightarrow$ Low Output	
(16) Pin	C Sync. output	Composite Sync Signal output	Positive polarity	

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