PES1600-12-080NA

AC-DC Front-End Power Supply

The PES1600-12-080NA is a 1600 Watt AC to DC, power-factor-corrected (PFC) power supply that converts standard AC power into a main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The PES1600-12-080NA utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

RoHS Compliant

80 PLUS PLATINUM

Key Features & Benefits

- Designed to meet Intel CRPS compatibility
- Best-in-class, meet 80 plus “Platinum” efficiency
- Auto-selected input voltage ranges: 90-140 VAC, 180-264 VAC
- AC input with active power factor correction
- 1600 W continuous output power capability
- Always-on 12 VSB / 3.5 A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- High power density design: 42 W/in^3
- Small form factor: 195 x 80 x 40 mm (7.68 x 3.15 x 1.57 in)
- Power Management Bus communications protocol for control, programming and monitoring
- Status LED with fault signaling

Applications

- Networking Switches
- Servers & Routers
- Telecommunications

1. ORDERING INFORMATION

PES	1600	-	12	-	080	N	A	x
Product Family	**Power Level**	**Dash**	**V1 Output**	**Dash**	**Width**	**Airflow**	**Input**	**AC Inlet**
PES Front-Ends	1600 W		12 V		80 mm	N: Normal	A: AC	Blank - C20 P - C22

2. OVERVIEW

The PES1600-12-080NA AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range the PES1600-12-080NA maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.
The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I^2C bus. The I^2C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. Cooling is managed by a fan controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I^2C bus.

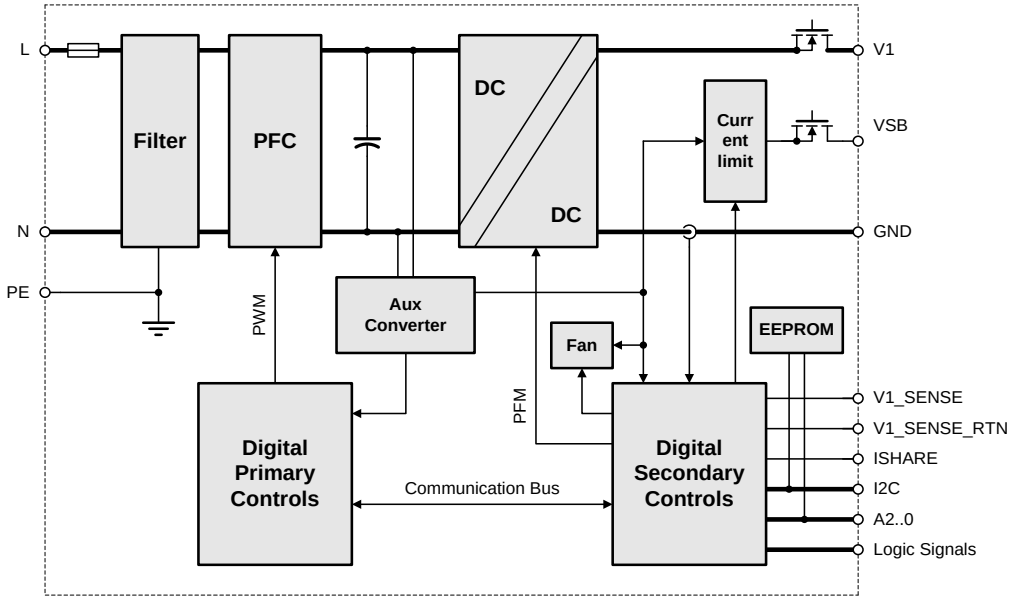


Figure 1. PES1600-12-080NA Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Vi maxc	Maximum Input	Continuous		264	VAC

4. INPUT

General Condition: T_A = 0… 55 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	AC Nominal Input Voltage	Rated Voltage High Line ($V_{i\,nom\,HL}$)	200	230	240	VAC
		Rated Voltage Low Line ($V_{i\,nom\,LL}$)	100	115	127	VAC
$V_{i\,nom\,DC}$	DC Nominal Input Voltage	Rated HVDC		240		VDC
$V_{i\,DC}$	DC Input Voltage range	Normal operating ($V_{i\,min}$ to $V_{i\,max}$)	180		300	VDC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min\,HL}$ to $V_{i\,max\,HL}$), High Line	180		264	VAC
		Normal operating ($V_{i\,min\,LL}$ to $V_{i\,max\,LL}$), Low Line	90		140	VAC
$I_{i\,max}$	Maximum Input Current	V_{IN} = 90 VAC, I_1 =91.6 A, I_{SB} =3.5 A			15	A_{RMS}
		V_{IN} = 180 VAC, I_1 =133 A, I_{SB} =3.5 A			10.5	A_{RMS}
$I_{i\,inrush}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{NTC} = 25°C, 5 ms			50	A_p
f_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	Vi = 230 VAC, 50 Hz and 60 Hz, Vi = 115 VAC,60 Hz				
		10% Load	0.8			W/VA
		20% Load	0.9			W/VA
		50% Load	0.9			W/VA
		100% Load	0.95			W/VA
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	85		90	VAC
$V_{i\,off}$	Turn-off Input Voltage[1]	Ramping down	80		85	VAC
η	Efficiency[2]	V_{IN} = 230 VAC, 10% load	82			%
		V_{IN} = 230 VAC, 20% load	90	92.5		%
		V_{IN} = 230 VAC, 50% load	94	94.3		%
		V_{IN} = 230 VAC, 100% load	91	92.7		%
$T_{V1\,holdup}$	Hold-up Time V_1	V_{IN} = 230 VAC, I_1 =133 A, I_{SB} =3.5 A	11			ms
		V_{IN} = 115 VAC, I_1 =91.6 A, I_{SB} =3.5 A	11			ms
$T_{VSB\,holdup}$	Hold-up Time V_{SB}	12 V_{SB}, full load	70			ms

4.1 INPUT FUSE

Time-lag 20 A input fuse (5.4 x 22.5 mm) in series with the L-line inside the power supply protects against severe defects. The fuse is not accessible from the outside and is therefore not a serviceable part.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X capacitance of only 4.7 µF , resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (PTC) may not sufficiently cool down.

[1] The Front-End is provided with a typical hysteresis of 5 VAC during turn-on and turn-off within the ranges. PSU will restart once input voltage within the $V_{i\,on}$.
[2] Efficiency measured without fan power per EPA server guidelines.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

4.5 EFFICIENCY

High efficiency (see *Figure 2)* is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

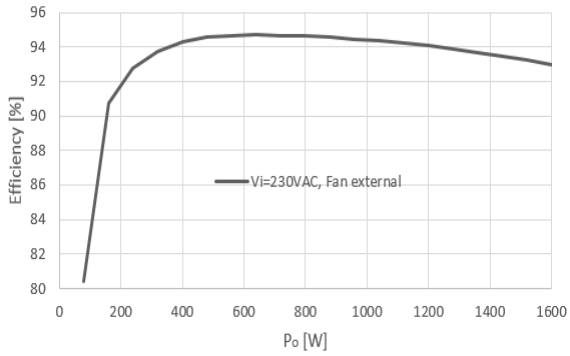


Figure 2. Efficiency vs. Load current (ratio metric loading)

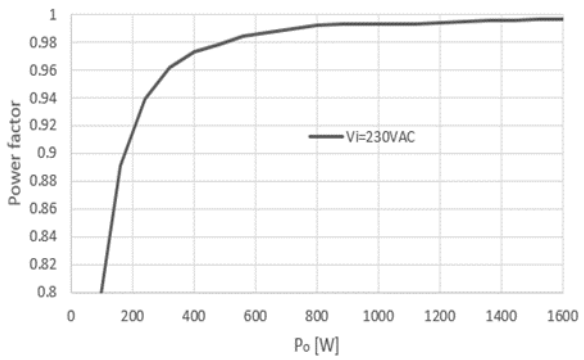


Figure 3. Power factor vs. Load current

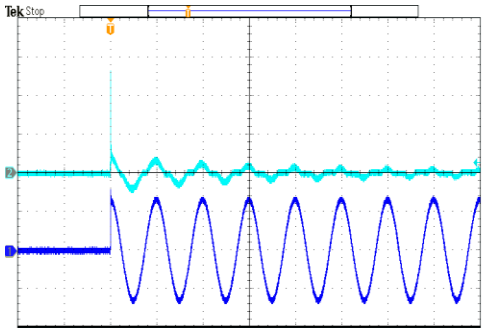


Figure 4. Inrush current, Vin = 230Vac, 90°
CH1: Vin (250V/div), CH2: Iin (10A/div)

4.6 INPUT LINE CURRENT HARMONIC

The power supply shall meet the requirements of EN61000-3-2 Class A and the Guidelines for the Suppression of Harmonics in Appliances and General Use Equipment Class A for harmonic line current content at full rated power.

	Per: EN 61000-3-2	Per: JEIDA MITI
Harmonic Order n	Maximum permissible Harmonic current at 230 VAC / 50 Hz in Amps	Maximum permissible Harmonic current at 100 VAC /50 Hz in Amps
Odd Harmonics		
3	2.3	5.29
5	1.14	2.622
7	0.77	1.771
9	0.4	0.92
11	0.33	0.759
13	0.21	0.483
15≤ n ≤39	0.15x (15/n)	0.345x (15/n)
Even Harmonics		
2	1.08	2.484
4	0.43	0.989
6	0.3	0.69
8≤ n ≤40	0.23x (8/n)	0.529x (8/n)

Table 1. Harmonic Limits for Class A Equipment

4.7 AC LINE TRANSIENT SPECIFICATION

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

AC Line Sag (10 sec interval between each sagging)

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 1/2 AC cycle	95%*	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
1 AC cycle to 500ms	>30%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self-recoverable

*** Comment:** for 95% sag condition, the load is 80%.

Table 2. AC Line Sag Transient Performance

AC Line Surge

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

Table 3. AC Line Surge Transient Performance

5. OUTPUT

General condition: T_A = 0…55 °C, V_i = 230VAC unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.0		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-1		+1	%$V_{1\ nom}$
dV1 load	Load Regulation	0 to 100% I1 nom			480	mV
dV1 line	Line Regulation	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			120	mV
$dV_{1\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$	-5		+5	%$V_{1\ nom}$
$P_{1\ nom}$	Nominal Output Power	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$		1600		W
		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$		1100		W
$I_{1\ peak}$	Peak Output Loading	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$ *(max 20s)*			150	ADC
		$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$ *(max 100us)*			205	ADC
		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$ *(max 20s)*			105	ADC
$I_{1\ nom}$	Output Current	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	0.0		133	ADC
$I_{1\ nom\ red}$		$V_{i\ min\ LL}$ to $V_{i\ max\ LL}$	0.0		91.6	ADC
$V_{1\ pp}$	Output Ripple Voltage[3]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			120	mVpp
$dI_{1\ share}$	Current Sharing	Deviation from $I_{1\ tot}$ / N, I_1 > 20%	-5		+5	% $I_{1\ nom}$
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		8		VDC
$dV_{1\ dyn}$	Dynamic Load Regulation	Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, ΔI1 = 60% $I1_{nom}$, I1 = 3A … 100% $I1_{nom}$, 2000µF capacitive loading dI1/dt = 0.25A/µs, recovery within 1% of $V1_{nom}$	11.40		12.60	VDC
t_{rec}	Recovery Time				2	ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$	1		70	ms
$t_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{1\ nom}$			0.6	V
$dV_{1\ sense}$	Remote Sense	Compensation for cable drop, 0 to 100% $I_{1\ nom}$			0.25	V
$C_{V1\ load}$	Capacitive Loading				22	mF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 ·$I_{SB\ nom}$, T_A = 25°C		12.0		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	%V_{SBnom}
dV_{sb} load	Load Regulation	0 to 100% ISB nom			480	mV
dV_{sb} line	Line Regulation	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			120	mV
$dV_{SB\ tot}$	Total Regulation	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$	-5		+5	%V_{SBnom}
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		42		W
$I_{SB\ peak}$	Peak Output Loading	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			4	ADC
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$	0.0		3.5	ADC
$V_{SB\ pp}$	Output Ripple Voltage [3]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			120	mVpp
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔI_{SB} = 50% $I_{SB\ nom}$, I_{SB} = 0 … 100% $I_{SB\ nom}$, dI_{SB}/dt = 0.25A/µs, recovery within 1% of $V_{SB\ nom}$	11.40		12.60	VDC
t_{rec}	Recovery Time				2	ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,	5		10	ms
$t_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$			0.6	V
$C_{VSB\ load}$	Capacitive Loading				1000	µF

[3] Ripple noise and dynamic load measured with a 10 µF low ESR capacitor in parallel with a 0.1 µF ceramic capacitor at the point of measurement.

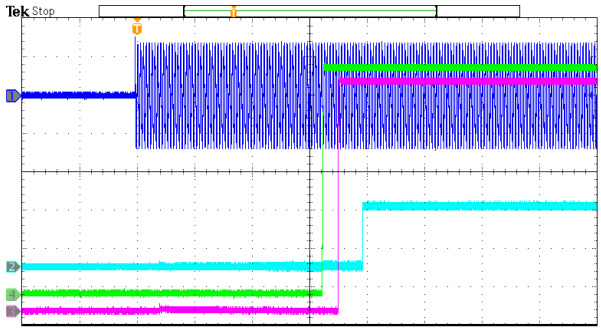


Figure 5. Turn-On AC Line 230VAC, full load (400ms/div)
CH1: Vin (400V/div) CH2: PWOK_H (2V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

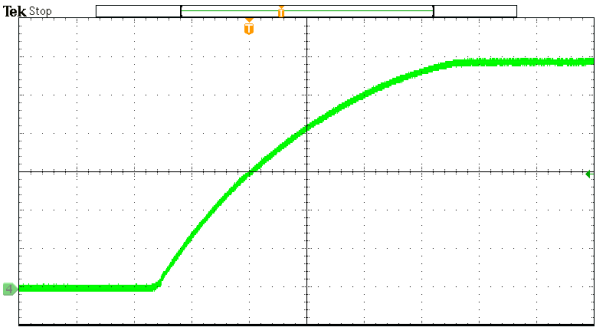


Figure 6. Turn-On AC Line 230VAC, full load (2ms/div)
CH4: V_{SB} (2V/div)

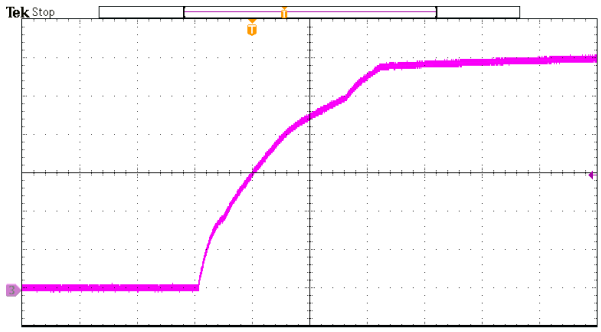


Figure 7. Turn-On AC Line 230VAC, full load (2ms/div)
CH3: V_1 (2V/div)

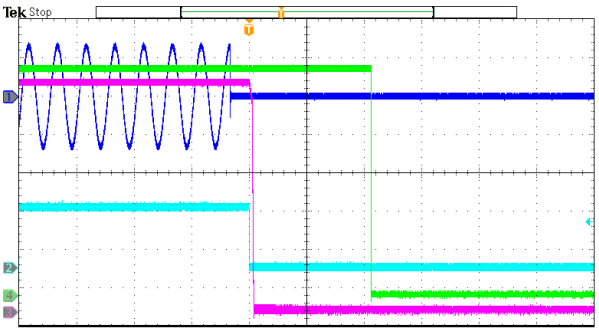


Figure 8. Turn-Off AC Line 230VAC, full load (40ms/div)
CH1: Vin (400V/div) CH2: PWOK_H (5V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

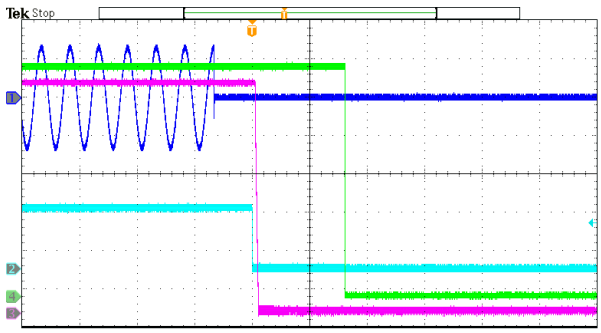


Figure 9. Turn-Off AC Line 230VAC, half load (40ms/div)
CH1: Vin (400V/div) CH2: PWOK_H (2V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (2V/div)

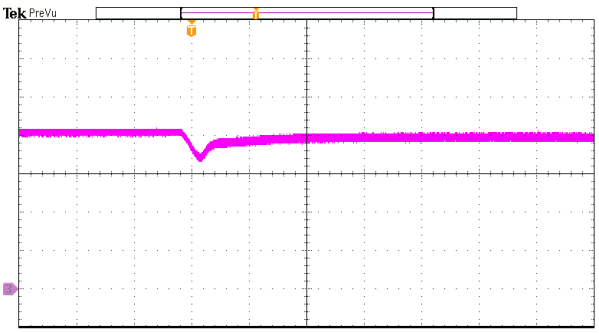


Figure 10. Load transient V_1, 53.2 to 133A (0.8ms/div)
CH3: V_1 (500mV/div)

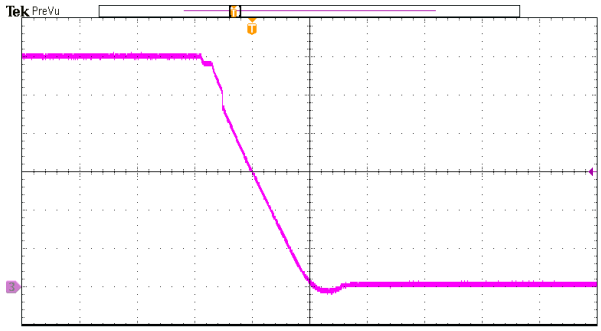


Figure 11. Short circuit on V1 (0.4ms/Div)
CH3: V_1 (2V/div)

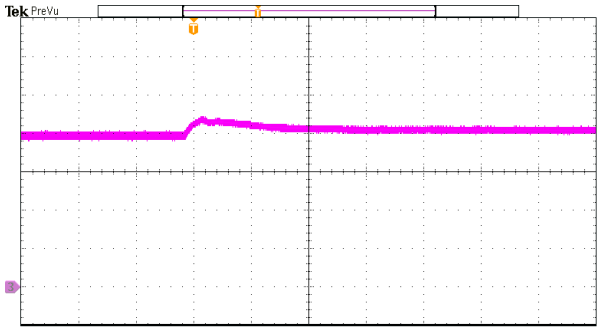


Figure 12. Load transient V_1, 133 to 53.2A (0.8ms/div)
CH3: V_1 (500mV/div)

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 13*. Alternatively, separated ground signals can be used as shown in *Figure 14*. In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE:
Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

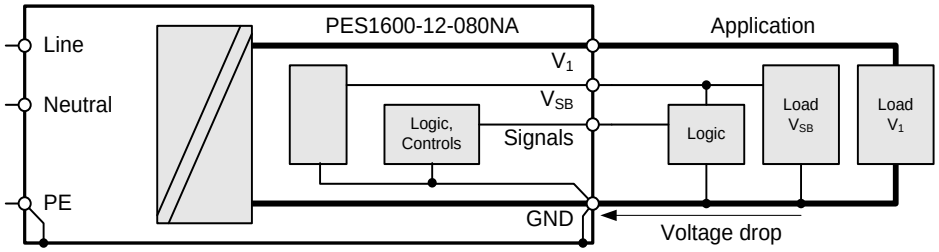


Figure 13. Common Low Impedance Ground Plane

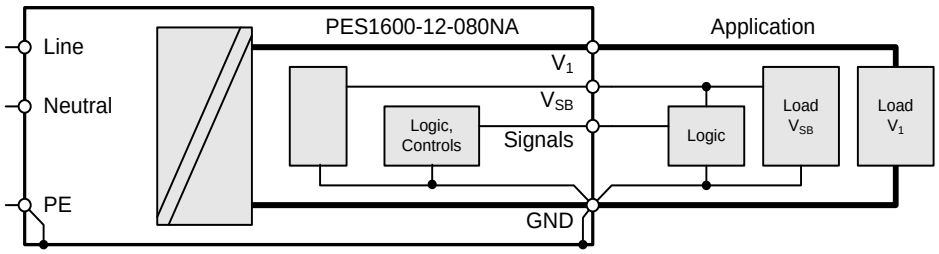


Figure 14. Separated Power and Signal Ground

5.2 CLOSED LOOP STABILITY

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB-gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 10%, 20%, 50% and 100% loads as applicable, 0% is just for reference.

5.3 RESIDUAL VOLTAGE IMMUNITY IN STANDBY MODE

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON_L signal is de-asserted.

5.4 COMMON MODE NOISE

The common mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 20MHz.

The measurement shall be made across a 100Ω resistor between each of DC outputs, including ground at the DC power connector and chassis ground (power subsystem enclosure), the test set-up shall use a FET probe such as Tektronix model P6046 or equivalent.

5.5 SOFT STARTING

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

5.6 ZERO LOAD STABILITY REQUIREMENTS

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.7 HOT SWAP REQUIREMENTS

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process, the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

5.8 FORCED LOAD SHARING

The PES front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 10% at full load.

The 12VSB output is not required to actively share current between power supplies (passive sharing).

5.9 RIPPLE / NOISE

The test set-up shall be following *Figure 15*.

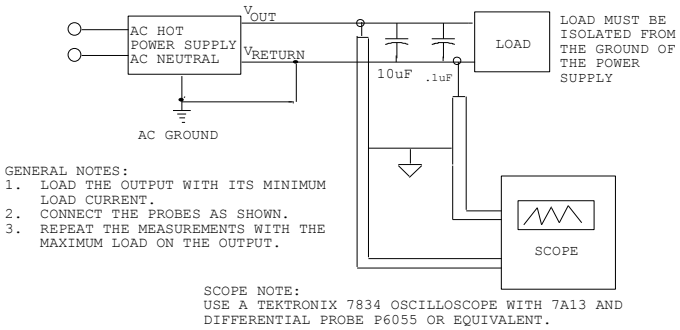


Figure 15. Differential Noise Test Setup

Note: Load must be isolated from the safety ground to *Figure 15*.

Note: When performing this test, the probe clips and capacitors should be located close to the load.

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input fuse (L)	Not use accessible, time-lag (T)		20		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	13.0	13.9	14.5	VDC
$V_{SB\ OV}$	OV Threshold V_{SB}	Over Voltage V_{SB} Protection, Auto-recovery Type	13.0	13.9	14.5	VDC
$V_{1\ UV}$	UV Threshold V_1	Under Voltage V_1 Protection, Latch-off Type		11.2		VDC
$V_{SB\ UV}$	UV Threshold V_{SB}	Under Voltage V_{SB} Protection, Auto-recovery Type		11.2		VDC
$I_{V1\ OC}$	OC Limit V_1	Over Current Limitation, Latch-off, $V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	Refer to section 6.5			ADC
		Over Current Limitation, Latch-off, $V_{i\ min\ LL}$ to $V_{i\ max\ LL}$				ADC
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current Limitation, Automatic recovery Type	4.5		5.5	A
T_{SD}	Over Temperature on Critical Points	Automatic shut-down	Refer to *Table 13*			°C

6.1 PROTECTION CIRCUITS

Protection circuits inside the power supply shall cause only the power supply's main output to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15sec and a PSON_L cycle HIGH for 1sec shall be able to reset the power supply.

6.2 OVER TEMPERATURE PROTECTION (OTP)

The power supply will be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature.
In an OTP condition, the PSU will shut down, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 5°C higher than over temperature warning threshold level.

6.3 OVER VOLTAGE PROTECTION

The PES1600-12-080NA front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. 12VSB will be auto-recovered after removing OVP limit.

6.4 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage.
The main output will latch off if the main output voltage V_1 falls below 11.2 V (typically in an overload condition), The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.
If the standby output leaves its regulation bandwidth for more than 10 ms then the main output is disabled to protect the system.

6.5 OVER CURRENT LIMIT & OVER POWER PROTECTION (OCP & OPP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown in Table 4 and Table 5. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared only by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 12VSB will be auto-recovered after removing OCP limit.

NORM	DESCRIPTION	CURRENT THRESHOLD (A)		TRIP TIMING		TESTING RANGE	COMMENTS
		MIN	MAX	MIN	MAX		
OCP1	Fast over current protection (shutdown, latch)	210	225	10µs	100us	OCP1 to Short Circuit	
OPP	Over power protection (voltage foldback)	195	210	5ms	20ms	OPP to Vfoldback to 8V	
OCW1	Fast over current warning (SMB_ALERT_L)	180	195	5µs	20µs		SMB_ALERT_L Latch and hold for 50-150ms
OCP2	Slow over current protection (shutdown, latch)	150	180	50ms	100ms		
OCW2	Slow over current warning (SMB_ALERT_L)	150	180	15ms	50ms		
OCPstby	Standby over current protection (shutdown, hiccup mode)	4.5	5.5				10ms minimum delay

Table 4. High Line Input

NORM	DESCRIPTION	CURRENT THRESHOLD (A)		TRIP TIMING		TESTING RANGE	COMMENTS
		MIN	MAX	MIN	MAX		
OCP2	Slow over current protection (shutdown, latch)	105	120	50ms	100ms		
OCW2	Slow over current warning (SMB_ALERT_L)	105	120	15ms	50ms		

Table 5. Low Line Input

The power supply shall have a circuit to quickly assert the SMB_ALERT_L signal when the output current exceeds the over power protection threshold in the PSU, The SMB_ALERT_L signal must always assert before the over power protection threshold is exceeded. SMB_ALERT_L must always latch for about 100msec before being released.

6.6 PEAK LOAD WITH ADDED SYSTEM BUFFER CAPACITANCE

The power supply shall be able to support higher peak power levels with added system buffer capacitance for up to 100µsec. Table 6 are PMAX testing conditions.

PEAK POWER	PEAK CURRENT	SYSTEM CAPACITANCE	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
2460W	205A	6,150 µF	100µs	5%

Table 6. PMAX Testing Conditions

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I2C / POWER MANAGEMENT BUS COMMUNICATION and document PES1600-12-080NA Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input Voltage	$V_{i\,min\,LL} \leq V_i \leq V_{i\,max}$	-2		+2	VAC
$I_{i\,mon}$	Input Current		-0.35		+0.35	A
$P_{i\,mon}$	True Input Power	$I_1 < 10\%\ I_{1\,nom}$	-8		+8	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-4		+4	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
$E_{i\,mon}$	Total Input Energy	$I_1 < 10\%\ I_{1\,nom}$	-8		+8	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-4		+4	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
$V_{1\,mon}$	V_1 Voltage		-1		+1	%
$I_{1\,mon}$	V_1 Current	$I_1 < 10\%\ I_{1\,nom}$	-1		+1	ADC
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-5		+5	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
P_{nom}	V_1 Output Power	$I_1 < 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
E_{nom}	V_1 Output Energy	$I_1 < 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
T_{ambmon}	Ambient Temperature	é°C ≤ T_{amb} ≤ 55°C	-3		+3	°C
F_S	Fan speed		-500		+500	RPM

8. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
PSON_L						
V_{IL}	Input Low Level Voltage	PSON_L: Main output enabled	0		0.8	V
V_{IH}	Input High Level Voltage	PSON_L: Main output disabled	2		5.25	V
$I_{IL,H}$	Maximum Source Current	V_I = -0.2V to +3.5V			4	mA
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			10		kΩ
PWOK_H						
V_{OL}	Output Low Level Voltage	$Vi < V_{i\ min\ LL}$, I_{sink}=400µA	0		0.4	V
V_{OH}	Output High Level Voltage	$Vi > V_{i\ min\ LL}$, I_{source}=200µA	2.4		3.46	V
I_S	Maximum Sink Current Maximum Source Current	PWOK_H = low PWOK_H = high			400 2	µA mA
SMB_ALERT_L						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			None		
I_S	Sink Current	SMB_ALERT_L = low SMB_ALERT_L= high			4 50	mA µA
VIN_OK_H						
V_{ext}	Maximum External Pull up Voltage				3.46	V
V_{OL}	Output Low Level Voltage	Failure or Warning condition, I_{sink} < 4mA	0		0.4	V
$R_{pull\ up}$	Pull-up to 3V3 Located in Power Supply			1		kΩ
I_S	Sink Current	VIN_OK_H = low			4	mA

8.2 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.
With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.3 PRESENT_L OUTPUT

The PRESENT_L pin is wired through a 100Ohms resistor to internal GND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 5mA to guarantee a low level voltage if power supply is seated.

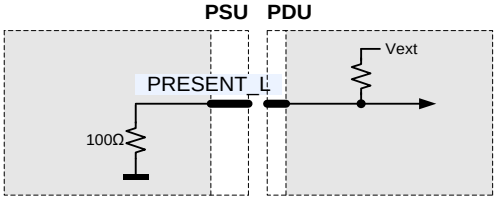


Figure 16. PRESENT_L Connection

8.4 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3 V) input signal to enable/disable the main output V1 of the front-end. With low level input the main output is enabled. This active-low pin is also used to clear any latched fault condition. The PSON_L can be either controlled by an open collector device or by a voltage source.

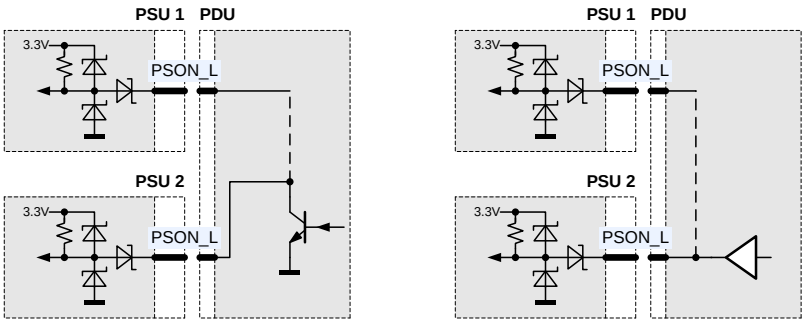


Figure 17. PSON_L connection

8.5 PWOK_H OUTPUT

PWOK_H is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK_H will be de-asserted to a LOW state. The start of the PWOK_H delay time shall inhibited as long as any power supply output is in current limit.
The PWOK_H and I2C bus of PSU are connected together on the redundant system. The below block diagram was shown the wiring on the system. The internal PWOK_H circuit of power supply is designed so that the PWOK_H bus is the wire-ORed function of the individual PWOK_H signals of all the power supply in parallel. Suggest system Pull-up to 3V3 and pull-up resistance is 10K. The PWOK_H signal also can be separated for each PSU design in system side to indicate each PSU output state.

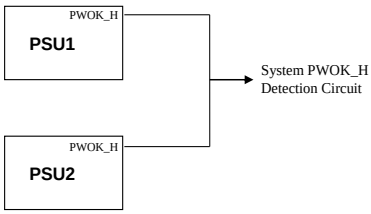


Figure 18. PWOK_H connection

8.6 SMB_ALERT_L OUTPUT

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Yellow.

The inlet temperature warning threshold must be set at 63°C, preventing exhaust air and cord temperatures temperature exceeding safety ratings. The warning gets de-asserted once inlet air temperature returns into specified operating temperature range. Fan speed control algorithm shall ramp up the fan speed to the maximum prior to the OT_WARNING bit set in STATUS_TEMPERATURE (7Dh) register.

In case exhaust air temperature exceeds 70°C higher temp rating cord must be used.

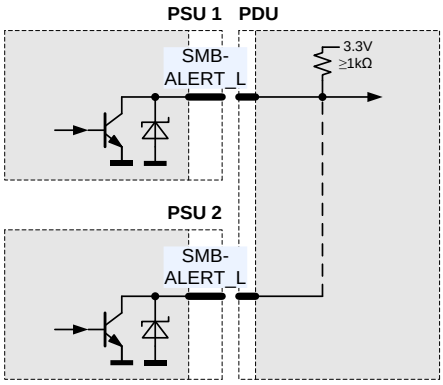


Figure 19. SMB_ALERT_L Connection

8.7 VIN_OK_H OUTPUT

This signal will be asserted, driven high, by the power supply to indicate that the input voltage meets the minimum requirements of the parametric PSU specification.

The PSU shall de-assert (drive low) under input over-voltage condition.

AC Line and AC loss detection algorithm

AC line voltage detection for power on:

The power supply will use Vrms to determine if the input voltage is within the specified requirements for turning on the power supply unit as called out by the individual power supply specification for AC input voltage range. The Vrms of the input must be determined within 5-cycles after the application of AC & Standby has reached regulation. Assertion requirements for VIN_OK_H remain the same.

AC line voltage detection for an AC brownout and dropout:

PSU shall detect both AC brown out and dropout conditions and issue a power down warning to the end system. The PSU shall de-assert (drive low) VIN_OK_H at least 4mS(T1) prior to the de-assertion of PWOK_H upon input conditions that fall below the Vin (turn-off) specification of the PSU parametric specification. Under such conditions. After VIN_OK_H de-assertion, the PSU shall be capable of delivering all outputs within the regulation limits for at least 4mS before de-asserting PWOK_H(T1). In a similar manner the PSU shall de-assert PWOK_H a minimum of 1mS prior to the main rail voltage degrading to 95% of the set point voltage value. Upon a VIN_OK_H de-assertion, the PSU shall derive an average RMS input voltage, measured over a moving average window equal to T2, to establish if conditions meet the requirements for assertion of VIN_OK_H. Refer to *Figure 20*.

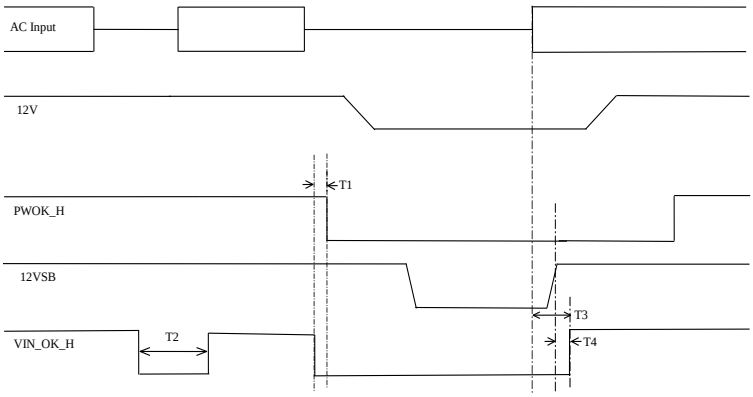


Figure 20. VIN_OK_H Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T1	VIN_OK_H & PWOK_H	4			ms
T2	VIN_OK_H Dwell Time	75		120	ms
T3	VIN_OK_H delay to AC			1700	ms
T4	VIN_OK_H to 12VSB			20	ms

Note1: T2 is the minimum VIN_OK_H de-assertion dwell time that is initiated when the PSU has declared a loss of input voltage.

Table 7. VIN_OK_H Timing Requirements

8.8 TIMING REQUIREMENTS

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 1 to 70ms. For 12VSB, it is allowed to rise from 5.0 between 10ms. All outputs must rise monotonically. T*able 8* shows the timing requirements for the power supply being turned on and off two ways; 1) via the AC input with PSON_L held low; 2) via the PSON_L signal with the AC input applied. The PSU needs to remain off for 1 second minimum after PWOK_H is de-asserted.

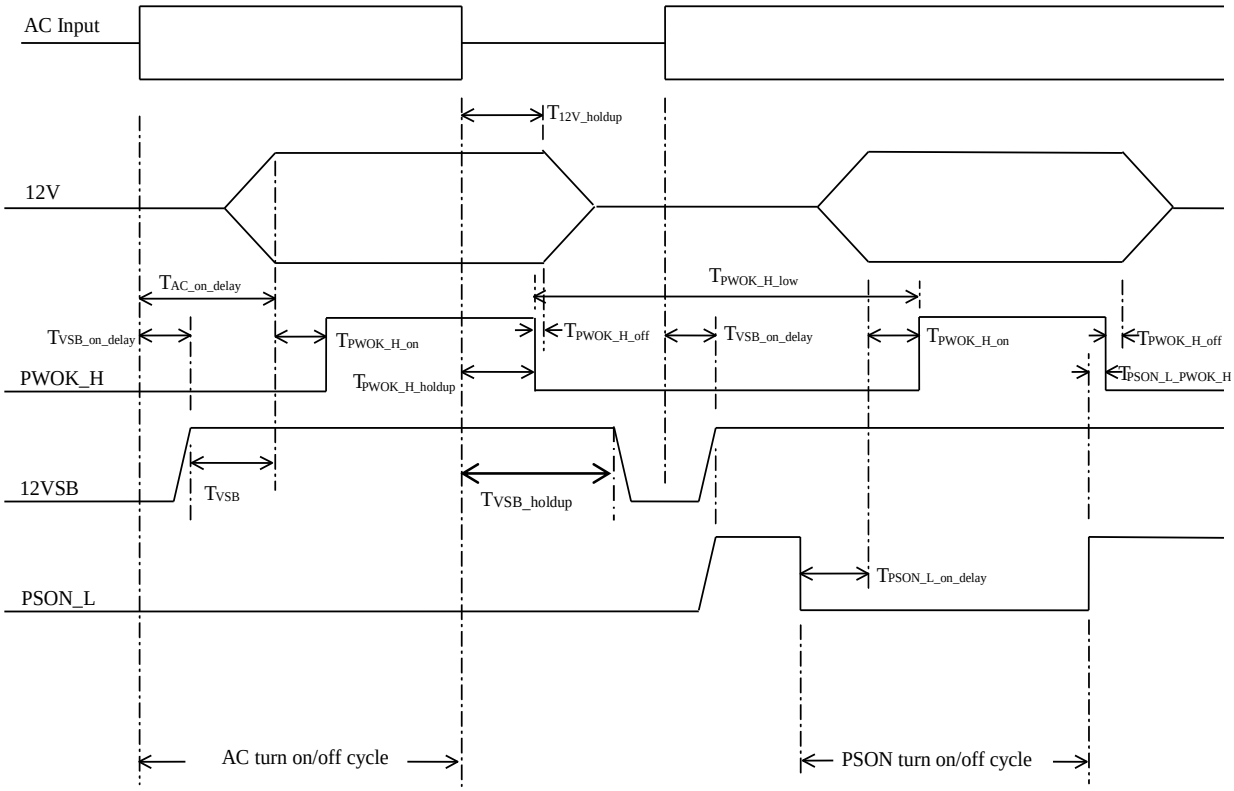


Figure 21. Turn On/Off Timing

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
T_{12V_rise}	Output voltage rise time	1.0 *		70 *	ms
$T_{VSB\_on\_delay}$	Delay from AC being applied to 12VSB being within regulation.			1500	ms
$T_{AC\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.			3000	ms
T_{12V_holdup}	Time 12V output voltage stay within regulation after loss of AC.	11			ms
$T_{PWOK\_H\_holdup}$	Delay from loss of AC to de-assertion of PWOK_H	10			ms
$T_{PSON\_L\_on\_delay}$	Delay from PSON_L active to output voltages within regulation limits.	5		400	ms
$T_{PSON\_L\_PWOK\_H}$	Delay from PSON_L deactivate to PWOK_H being de-asserted.			5	ms
$T_{PWOK\_H\_on}$	Delay from output voltages within regulation limits to PWOK_H asserted at turn on.	100		500	ms
$T_{PWOK\_H\_off}$	Delay from PWOK_H de-asserted to output voltages dropping out of regulation limits.	1			ms
$T_{PWOK\_H\_low}$	Duration of PWOK_H being in the de-asserted state during an off/on cycle using AC or the PSON_L signal.	100			ms
T_{VSB}	Delay from 12VSB being in regulation to O/Ps being in regulation at AC turn on.	50		1000	ms
T_{VSB_holdup}	Time the 12VSB output voltage stays within regulation after loss of AC.	70			ms
$T_{AC\_off\_SMB\_ALERT\_L}$	The power supply shall assert the SMB_ALERT_L signal quickly after a loss of AC input voltage			2	ms

* The 12VSB output voltage rise time shall be from 5.0 ms between 10 ms.

Table 8. Timing Requirements

8.9 HOT_STANDBY

The hot-standby operation is an operating mode allowing to further increase efficiency at light load conditions in a redundant power supply system. Under specific conditions one of the power supplies is allowed to disable Oring gate, to make sure into hot standby mode. This will save the power losses associated with this power supply and at the same time the other power supply will operate in a load range having a better efficiency.

8.10 LED INDICATOR

The front-end has one front LED showing the status of the supply. The LED is bi-colored: green and yellow, and indicates AC and DC power presence and warning or fault conditions. *Table 10* lists the different LED status.

	MIN λd WAVELENGTH	NOMINAL λd WAVELENGTH	MAX λd WAVELENGTH	UNITS
Green		570		nm
Yellow		590		nm

Table 9. LED Characteristics

OPERATING CONDITION	LED STATE
Output ON and OK	Solid GREEN
No AC power to all power supplies	OFF
AC present / Only 12VSB on (PS off) or PS in Hot standby state	1Hz Blink GREEN
AC cord unplugged; with a second power supply in parallel still with AC input power.	Solid YELLOW
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink YELLOW
Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	Solid YELLOW
Power supply in FW upload mode	2Hz Blink GREEN

Table 10. LED Status

9. I²C / POWER MANAGEMENT BUS COMMUNICATION

The PES front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 11* further characterized through:

- The SDA/SCL IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery
- within 10 ms
- Recognizes any time Start/Stop bus conditions

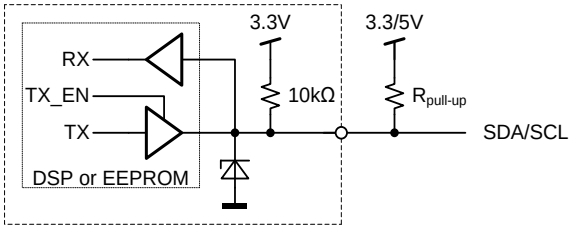


Figure 22. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 11. I²C / SMBus Specification

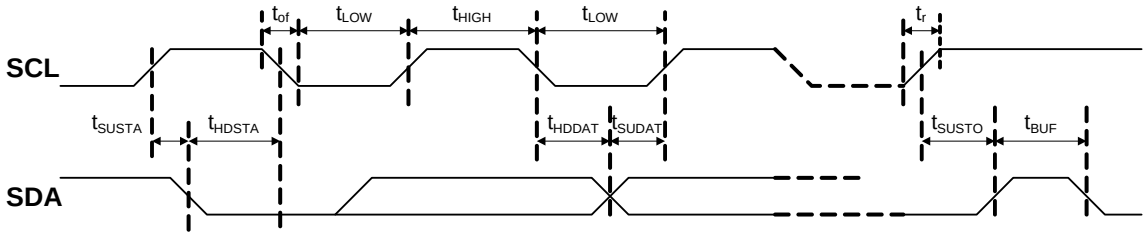


Figure 23. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pins A2, A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A2 / A1 / A0 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

A2	A1	A0	I2C Address *	
			Controller	EEPROM
0	0	0	0xB0	0xA0
0	0	1	0xB2	0xA2
0	1	0	0xB4	0xA4
0	1	1	0xB6	0xA6
1	0	0	0xB8	0xA8
1	0	1	0xBA	0xAA
1	1	0	0xBC	0xAC
1	1	1	0xBE	0xAE

* The LSB of the address byte is the R/W bit

Table 12. Address and Protocol Encoding

9.1 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure *24*) and can be accessed under different addresses, see ADDRESS SELECTION.
The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3V3.
The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

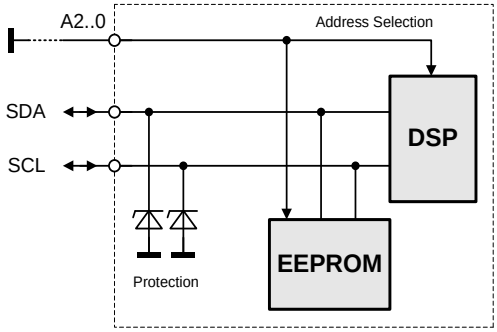


Figure 24 - I2C Bus to DSP and EEPROM

9.2 EEPROM PROTOCOL

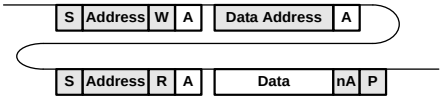
The EEPROM follows the industry communication protocols used for this type of device. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

WRITE

The write command follows the SMBus 1.1 Write Byte protocol. After the device address with the write bit cleared a first byte with the data address to write to is sent followed by the data byte and the STOP condition. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.

READ

The read command follows the SMBus 1.1 Read Byte protocol. After the device address with the write bit cleared the data address byte is sent followed by a repeated start, the device address and the read bit set. The EEPROM will respond with the data byte at the specified location.



9.3 POWER MANAGEMENT BUS PROTOCOL

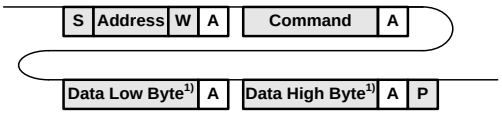
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PES1600-12-080NA supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

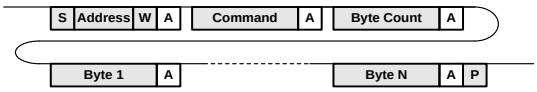
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



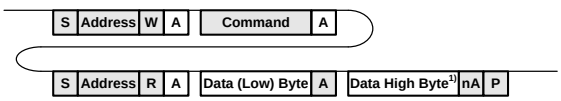
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.



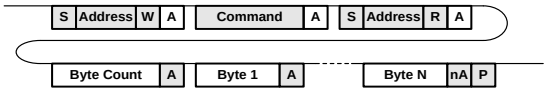
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



9.4 POWER SUPPLY DIAGNOSTIC "EVENT RECORDER"

The power supply shall save the latest data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus interface with an external source providing power to the 12Vstby output.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.00199_PES1600-12-080NA Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

9.5 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 12Vstby pins. BPS standard GUI supports the firmware upgrade function.

9.6 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its "I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PES1600-12-080NA Front-End.
The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the YTM.00103 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.

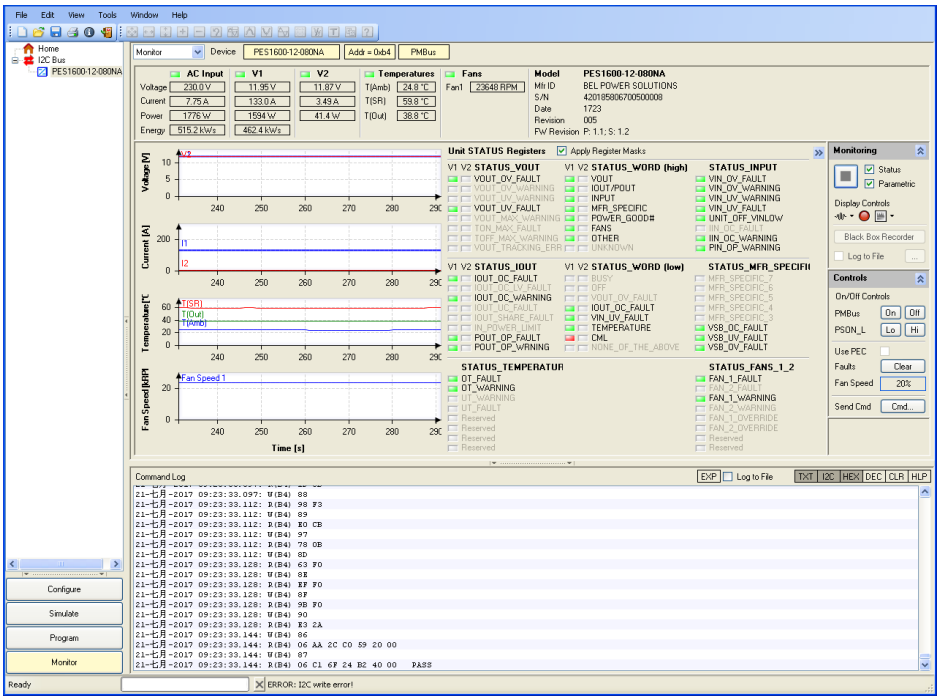


Figure 25. Monitoring dialog of the I²C Utility

10. TEMPERATURE AND FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The PES1600-12-080NA is pro-vided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet. The PES1600-12-080NA supply has been designed for horizontal operation.

The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

The fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA (roughly 10% mean speed). This condition may be treated as steady state fan speed condition.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60s.

The PES1600-12-080NA provides access via I²C to the measured temperatures of in total 4 sensors within the power supply, see *Table 13*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK_H and SMB_ALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	8Dh	63	68
Syn rectifier Mosfet	Sensor located close to Syn rectifier Mosfet	8Eh	110	115
Outlet air temperature	Sensor located on main board close to AC front of power supply	8Fh	80	85
PFC heat sink	Sensor located on PFC heat sink	EAh	96	101

Table 13. Temperature Sensor Location and Thresholds

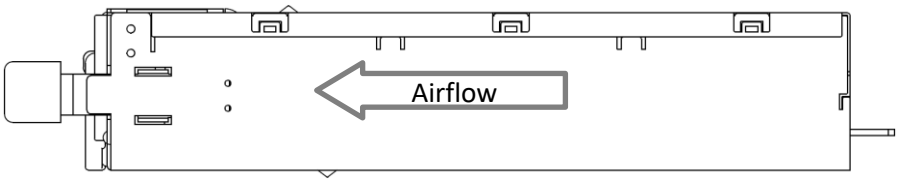


Figure 26. Airflow Direction

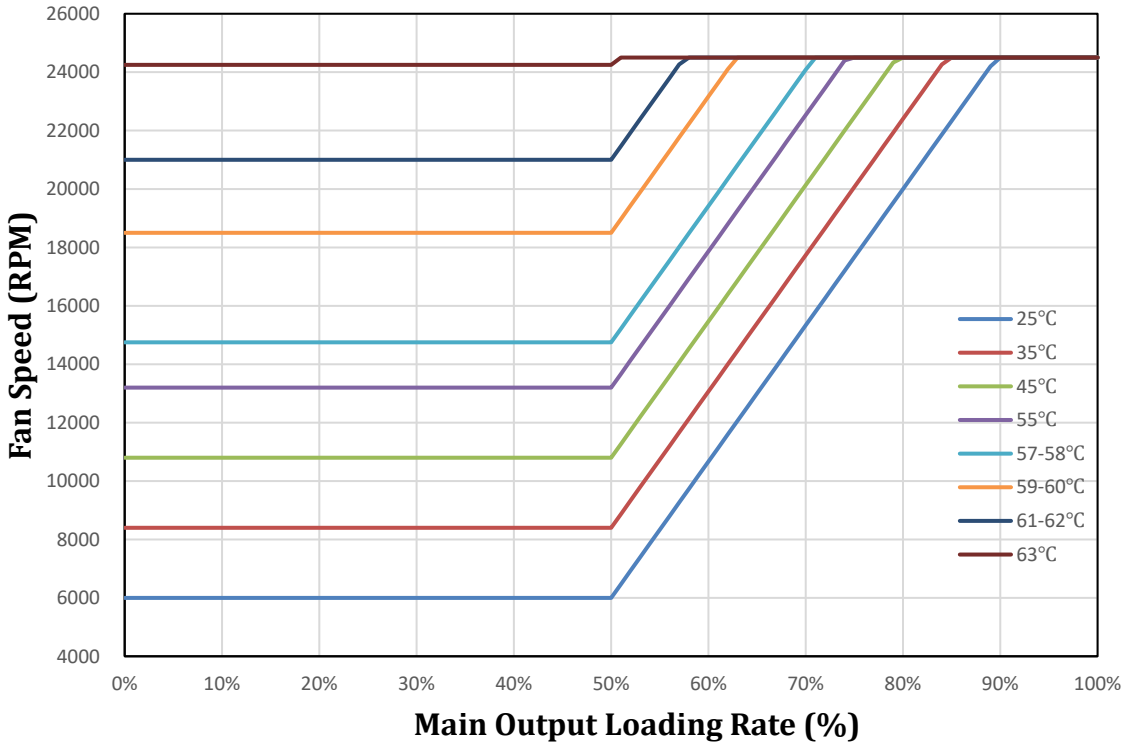


Figure 27. Fan Speed vs. Main Output Load

Comment: The fan minimum speed is 6000RPM.

11. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.	B
Radiated Electromagnetics Filed	EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24	A
Burst	EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24	B
Surge*	The power supply shall be tested with the system for immunity to AC Unidirectional wave; 2kV line to ground and 1kV line to line, per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition 1.1:2001-04	B
RF Conducted Immunity	IEC / EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 … 80 MHz	A
Harmonic Emissions	The power supply shall meet the requirements of EN61000-3-2	A
AC Flicker	IEC 61000-3-3, Vi = 230 VAC / 50Hz, 100% Load	Pass
Voltage Dips and Interruptions	EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in Annex B of CISPR 24, the load is 80%.	C

* The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.
The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in Annex B of CISPR 24

LEVEL	DESCRIPTION
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

Table 14. Performance Criteria

11.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A
	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 power supplies in a system	Class A
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A
	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 power supplies in a system	Class A
Acoustical Noise	A-weighted sound power, 25°C, 50% Load	49dB

12. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL60950-1/CSA 60950-1 (USA / Canada) EN60950-1 (Europe) IEC60950-1 (International) CB Certificate & Report, IEC60950-1 (report to include all country national deviations) CE - Low Voltage Directive 2014/35/EC GB4943.1- CNCA Certification (China) CNS14336-1	Approved
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Reinforced
	Output to chassis	None (Direct connection)
Electrical Strength Test	Input to output	4242 VDC
	Input to chassis	2121 VDC

Comment: All printed wiring boards and all connectors meet UL94V-0 level.

13. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as “Handle, knobs, grips, etc. held for short periods of time only”.

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature that is in compliance with IEC/UL 60950-1 and additionally 85°C rated power cords must also be used with this power supply.

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum typical load under redundant configurations		890	W
Top1	Operating temperature range; 900m	0	55	°C
Top2	Operating temperature range; 3050m	0	50	°C
Texit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters

Table 15. Requirements for Redundant Power Supply Configuration

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum rated output load		1600	W
Top1	Operating temperature range; 900m	0	45	°C
Top2	Operating temperature range; 3050m	0	40	°C
Texit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 40°C inlet		3050	meters
Altitude2	Maximum operating altitude; 45°C inlet		900	meters

Table 16. Requirements for Non-Redundant Power Supply Configuration (Typical System Ambient)

ITEM	DESCRIPTION	MIN	MAX	UNITS
Load	Maximum rated output load		1600	W
Top1	Operating temperature range; 900m	0	55	°C
Top2	Operating temperature range; 3050m	0	50	°C
Texit	Maximum exit air temperature		68	°C
Tnon-op	Non-operating temperature range	-40	70	°C
Altitude1	Maximum operating altitude; 50°C inlet		3050	meters
Altitude2	Maximum operating altitude; 55°C inlet		900	meters

Table 17. Requirements for Non-Redundant Power Supply Configuration (High System Ambient)

13.1 HUMIDITY

Operating: To 85% relative humidity (non-condensing)

Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

13.2 ALTITUDE

Operating: To 3050 m (Maximum operating altitude 5000 meters and the Maximum operating temperature to 40°C.)

Non-operating: To 15200 m

13.3 SHOCK AND VIBRATION

13.3.1 RANDOM VIBRATION – OPERATING

Sample Size: For all product classes and categories, the minimum number of samples shall be 3 devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance. Each device shall be tested in three axes for a minimum of 30 minutes per axis. The device shall be powered for the duration of the test at nominal input voltage and no load. For operating vibration testing, see *Figure 28*.

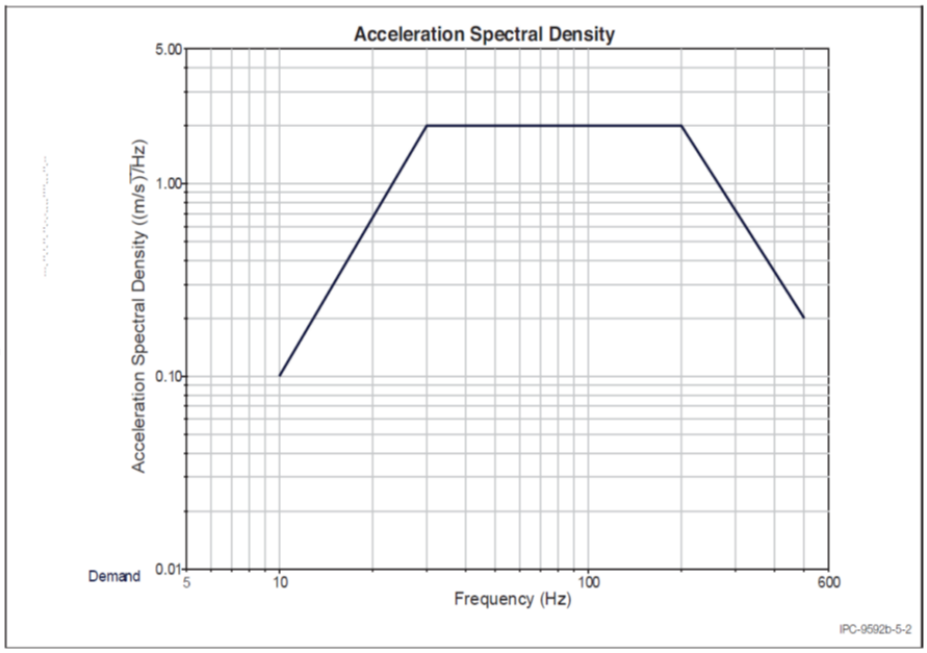


Figure 28. Class II PCDs Operating Vibration Test: Acceleration vs Frequency

The total acceleration for Class II PCDs is approximately 2.4g rms (See Table 18)

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
10	0.022	0.000229	0.1	0.00046
30	0.20	0.0021	2	0.0052
200	0.20	0.0021	2	0.0052
500	0.0052	0.000054	0.2	0.0001
	Grms = 0.71		Grms = 2.40	

Table 18. Operation Vibration Profile Charts

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.2 RANDOM VIBRATION - NON-OPERATING

Sample Size: For all product categories and product classes, the minimum number of samples shall be 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing - Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance, with the acceleration spectral density curves provided in this document. The products are in the shipping packaging for this test. For non-operating vibration testing, see Table *19*. Each shipping package shall be tested in three axes for a minimum of 30 minutes per axis.

The total acceleration for Class II PCDs is approximately 3.8g rms (See Table *19*).

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
5	1	0.01	5	0.0052
200	1	0.01	5	0.0052
500	0.03	0.003	0.3	0.003
	Grms = 1.90		Grms = 3.80	

Table 19. Non-Operating Vibration Profile Charts

Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed. All units shall also pass a functional test.
There are no requirements on the condition of the shipping package.

13.3.3 SHOCK – OPERATING

Sample Size: For all product types and product classes, the minimum number of samples shall be three devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-27, Environmental Testing-Part 2.27 Test Ea and guidance: Shock. Each tested device shall be exposed to three shocks in each of 3 axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11mS.

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

13.3.4 THERMAL SHOCK (SHIPPING)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

14. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time between failure	T_A = 40°C, 75% load, according Telcordia SR-332, issue 2	250			kh

Comment: All components de-rating follow IPC9592B.

15. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width Heigth Depth		80 40 195		mm mm mm
m	Weight			1		kg

Tolerance unless otherwise stated: 0.5-30 mm: +/-0.3 mm; 30-120 mm: +/-0.4 mm; 120-400 mm: +/-0.5 mm.

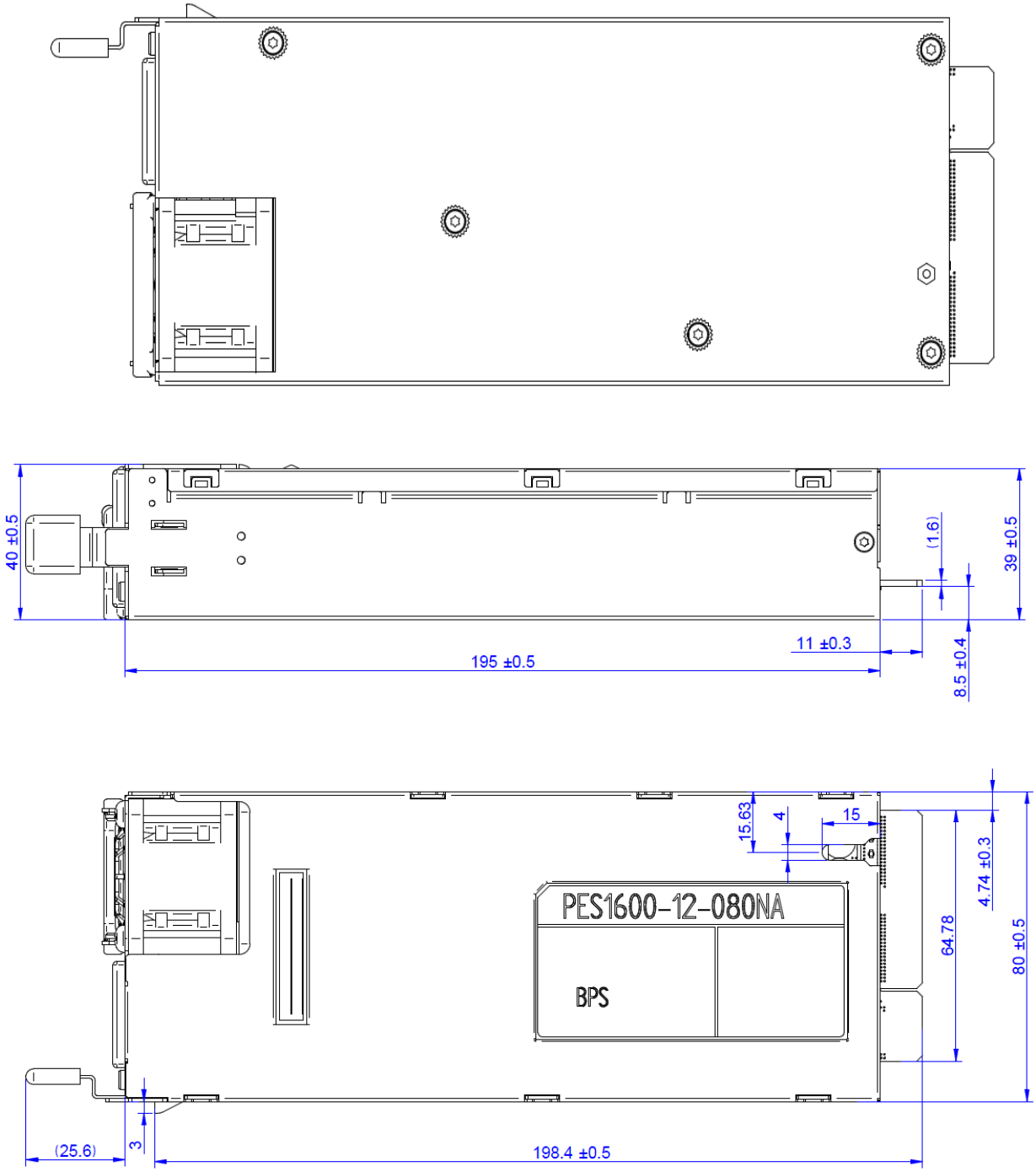


Figure 29. Top, bottom and side view

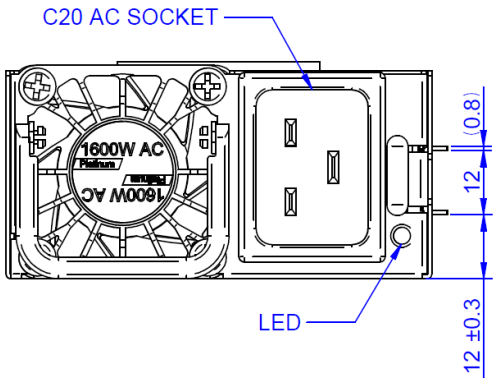


Figure 30. Front view

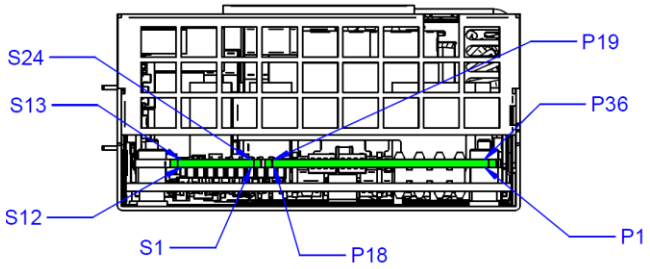


Figure 31. Rear view

16. CONNECTORS

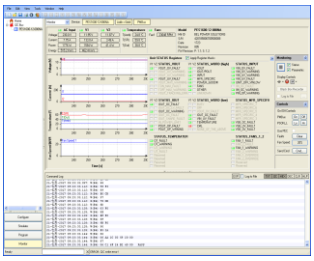
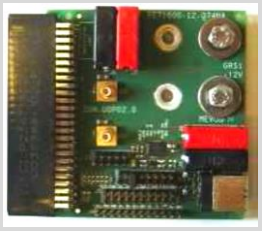
PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
AC inlet	IEC 60320 C20				
AC cord requirement	Wire size		16		AWG
Output connector	36 Power + 24 signals Pins PCB card edge				
Mating output connector	Manufacturer : FCI Electronics Manufacturer P/N: 10130248-005LF BEL P/N: ZES.00678				

PIN	SIGNAL NAME	DESCRIPTION	Mating Sequence[4]
P1 ~ P10	GND	Power and signal ground (return)	1
P29 ~ P36	GND		
P11 ~ P18	V1	+12VDC main output	2
P19 ~ P28	V1		
S1	A0	I²C address selection input	1
S2	A1		1
S3, S4	VSB	+12V Standby positive output (as pins S3, S4)	1
S5	Hot_ Standby	Hot standby Bus	1
S6	ISHARE	Analog current share bus	1
S7	VIN_OK _H	Input OK signal output, active-high	1
S8	PRESENT_L	Power supply seated, active-low	3
S9	A2	I²C address selection input	1
S10 ~ S15	GND	Power and signal ground (return)	1
S16	PWOK_H	Power OK signal output, active-high	1
S17	V1_SENSE	Main output positive sense	1
S18	V1_SENSE_R	Main output negative sense	1
S19	SMB_ALERT_L	SMB Alert signal output, active-low	1
S20	PSON_L	Power supply on input, active-low	3
S21, S22	VSB	+12V Standby positive output (as pins S3, S4)	1
S23	SCL	I²C clock signal line	1
S24	SDA	I²C data signal line	1

Table 20. Output connector pin assignment

[4] 1 = First, 3 = Last, given by different card edge finger pin lengths and mating connector pin arrangement

17. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor Front-End power supplies (and other I²C units)	N/A	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate PES1600-12-080NA. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	YTM.00103	belfuse.com/power-solutions

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For more information on these products consult: tech.support@psbel.com

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