2PD2150

20 V, 3 A NPN low V_{CEsat} (BISS) transistor Rev. 02 — 2 January 2007

Product data sheet

Product profile

1.1 General description

NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a medium power SOT89 (SC-62/TO-243) flat lead Surface-Mounted Device (SMD) plastic package.

PNP complement: 2PB1424.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- DC-to-DC conversion
- MOSFET gate driving
- Motor control
- Charging circuits
- Power switches (e.g. motors, fans)
- Thin Film Transistor (TFT) backlight inverter

1.4 Quick reference data

Table 1. **Quick reference data**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CEO}	collector-emitter voltage	open base	-	-	20	V
I_{C}	collector current		-	-	3	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	-	5	Α
V _{CEsat}	collector-emitter saturation voltage	$I_C = 2 A$; $I_B = 0.1 A$	<u>[1]</u> _	0.2	0.5	V

^[1] Pulse test: $t_p \le 300 \ \mu s; \ \delta \le 0.02.$



20 V, 3 A NPN low V_{CEsat} (BISS) transistor

2. Pinning information

Table 2. Pinning

	3				
Pin	Description	Simplified outline	Symbol		
1	emitter		_		
2	collector		2 J		
3	base	3 2 1	3 — 1 sym042		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2PD2150	SC-62	plastic surface-mounted package; collector pad for good heat transfer; 3 leads	SOT89

4. Marking

Table 4. Marking codes

Type number	Marking code
2PD2150	M2

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

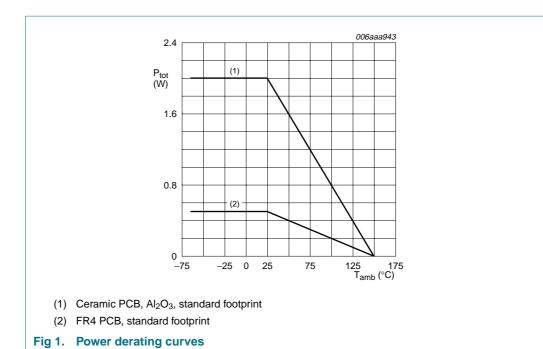
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	40	V
V_{CEO}	collector-emitter voltage	open base	-	20	V
V_{EBO}	emitter-base voltage	open collector	-	6	V
$I_{\mathbb{C}}$	collector current		-	3	Α
I _{CM}	peak collector current	single pulse; $t_p \le 1 \text{ ms}$	-	5	Α
P _{tot}	total power dissipation	$T_{amb} \le 25 ^{\circ}C$	<u>[1]</u> _	0.5	W
			[2] -	2	W
Tj	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T_{stg}	storage temperature		-65	+150	°C

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

© Nexperia B.V. 2007. All rights reserved.

^[2] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

20 V, 3 A NPN low V_{CEsat} (BISS) transistor



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-a)}$	thermal resistance from	in free air	<u>[1]</u> -	-	250	K/W
	junction to ambient		[2] _	-	62	K/W

^[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

^[2] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

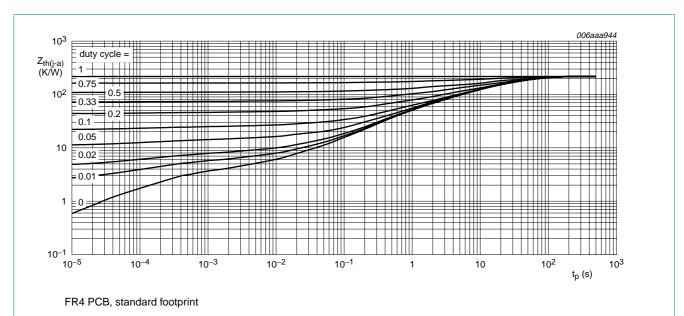


Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

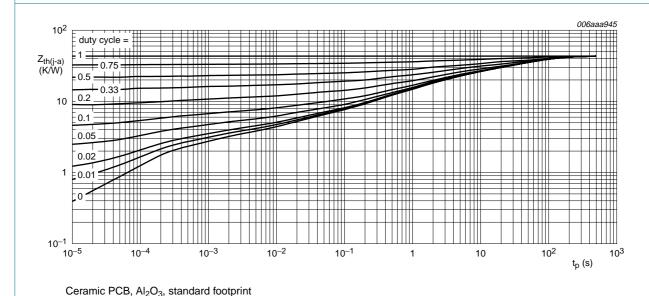


Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

7. Characteristics

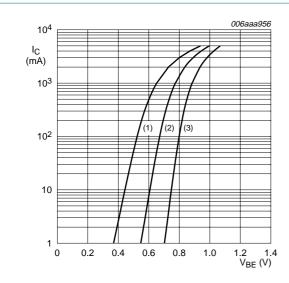
Table 7. Characteristics

 $T_{amb} = 25 \,^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{CBO}	collector-base cut-off current	$V_{CB} = 30 \text{ V}; I_E = 0 \text{ A}$	-	-	0.1	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}$	-	-	0.1	μΑ
h _{FE}	DC current gain	$V_{CE} = 2 \text{ V}; I_{C} = 0.1 \text{ A}$	180	-	390	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 2 A; I_B = 0.1 A$	[1] _	0.2	0.5	V
f _T	transition frequency	$V_{CE} = 2 \text{ V}; I_{E} = -0.5 \text{ A};$ f = 100 MHz	-	220	-	MHz
C _{ib}	common-base input capacitance	$V_{EB} = 5 \text{ V}; I_E = I_e = 0 \text{ A};$ f = 1 MHz	-	180	-	pF
C_{ob}	common-base output capacitance	$V_{CB} = 10 \text{ V}; I_E = i_e = 0 \text{ A};$ f = 1 MHz	-	20	-	pF

^[1] Pulse test: $t_p \le 300 \ \mu s; \ \delta \le 0.02.$

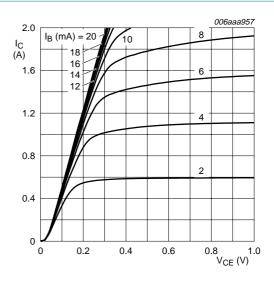
20 V, 3 A NPN low V_{CEsat} (BISS) transistor



$$V_{CE} = 2 V$$

- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \,^{\circ}C$
- (3) $T_{amb} = -40 \, ^{\circ}C$

Fig 4. Collector current as a function of base-emitter voltage; typical values



T_{amb} = 25 °C

Fig 5. Collector current as a function of collector-emitter voltage; typical values

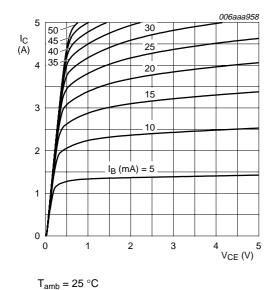
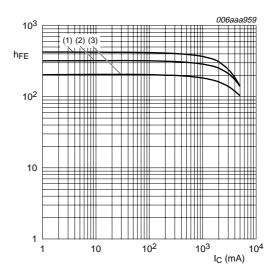


Fig 6. Collector current as a function of collector-emitter voltage; typical values



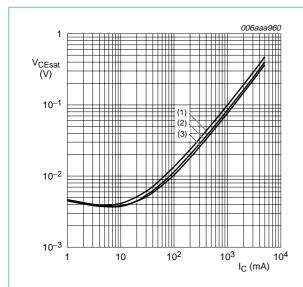
 $V_{CE} = 2 V$

- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -40 \, ^{\circ}C$

Fig 7. DC current gain as a function of collector current; typical values

PD2150 © Nexperia B.V. 2007. All rights reserved.

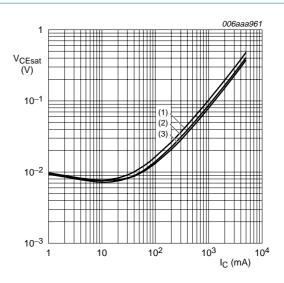
20 V, 3 A NPN low V_{CEsat} (BISS) transistor



$$I_{\rm C}/I_{\rm B} = 10$$

- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -40 \, ^{\circ}C$

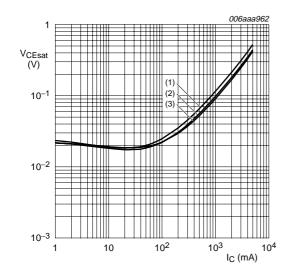
Fig 8. Collector-emitter saturation voltage as a function of collector current; typical values



$$I_{\rm C}/I_{\rm B} = 20$$

- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -40 \, ^{\circ}C$

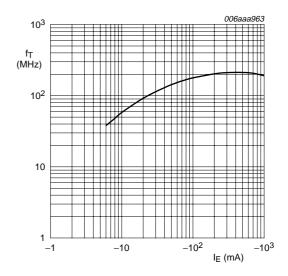
Fig 9. Collector-emitter saturation voltage as a function of collector current; typical values



 $I_{\rm C}/I_{\rm B}=50$

- (1) $T_{amb} = 100 \, ^{\circ}C$
- (2) $T_{amb} = 25 \, ^{\circ}C$
- (3) $T_{amb} = -40 \, ^{\circ}C$

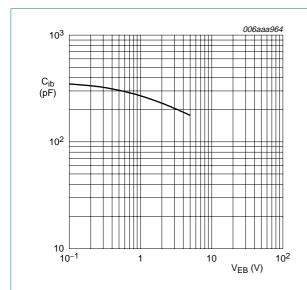
Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



 $T_{amb} = 25 \, ^{\circ}C; \, V_{CE} = 2 \, V$

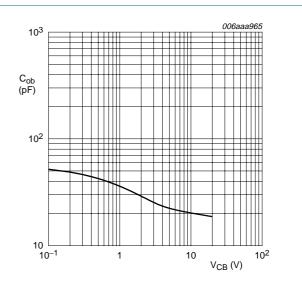
Fig 11. Transition frequency as a function of emitter current; typical values

20 V, 3 A NPN low V_{CEsat} (BISS) transistor



 T_{amb} = 25 °C; f = 1 MHz; I_E = i_e = 0 A

Fig 12. Common-base input capacitance as a function of emitter-base voltage; typical values

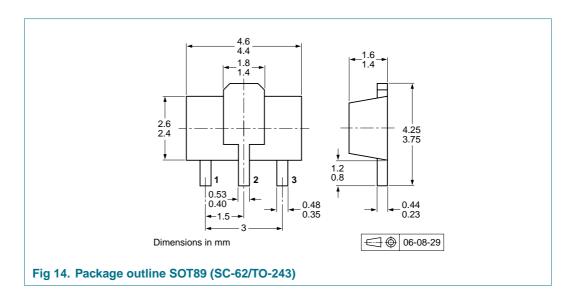


 T_{amb} = 25 °C; f = 1 MHz; I_E = i_e = 0 A

Fig 13. Common-base output capacitance as a function of collector-base voltage; typical values

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

8. Package outline

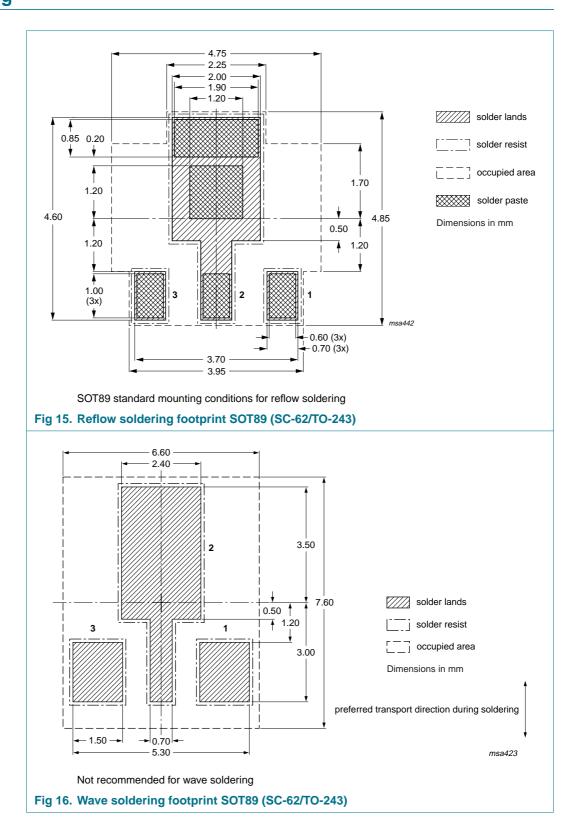


9. Packing information

Please refer to packing information on www.nexperia.com.

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

10. Soldering



20 V, 3 A NPN low V_{CEsat} (BISS) transistor

11. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
2PD2150_2	20070102	Product data sheet	-	2PD2150_1		
Modifications:		of this data sheet has beer of NXP Semiconductors.	redesigned to comply v	vith the new identity		
	 Legal texts 	have been adapted to the	new company name who	ere appropriate.		
	● <u>Table 1 "Qu</u>	iick reference data": I _C colle	ector current added			
	Table 1 "Quick reference data": I _{CM} peak collector current maximum value adapted					
	Table 1 "Quick reference data": V _{CEsat} collector-emitter saturation voltage added					
	 <u>Table 5 "Limiting values"</u>: V_{CEO} collector-emitter voltage maximum value adapted 					
	 <u>Table 5 "Limiting values"</u>: I_C collector current maximum value adapted 					
	 <u>Table 5 "Limiting values"</u>: I_{CM} peak collector current maximum value adapted 					
	 <u>Table 5 "Limiting values"</u>: P_{tot} total power dissipation for ceramic PCB condition added 					
	Figure 1 "Power derating curves": adapted					
	 <u>Table 6 "Thermal characteristics"</u>: adapted 					
	 <u>Table 6 "Thermal characteristics"</u>: R_{th(j-a)} thermal resistance from junction to ambient for ceramic PCB condition added 					
	 Figure 2: t_p pulse time redefined to pulse duration 					
	• Figure 3: ac	dded				
	 Table 7 "Ch 	aracteristics": V _{CEsat} collec	tor-emitter saturation vol	tage typical value added		
	• Table 7 "Ch	aracteristics": f _T transition f	requency conditions slig	htly changed		
	Table 7 "Characteristics": Cib common-base input capacitance added					
	 Table 7 "Characteristics": Cob common-base output capacitance added 					
	• Figure 4, 6, 10, 11, 12, 13 and 16: added					
		8 and 9: adapted				
	• Section 12	"Legal information": update	d			
2PD2150_1	20050422	Product data sheet	-	-		

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

12.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia accepts no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by Nexperia. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20 V, 3 A NPN low V_{CEsat} (BISS) transistor

13. Contents

Product profile
General description
Features
Applications
Quick reference data
Pinning information 2
Ordering information
Marking
Limiting values
Thermal characteristics 3
Characteristics 5
Package outline
Packing information
Soldering
_
Revision history
Legal information 12
Data sheet status
Definitions
Disclaimers
Trademarks
Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

All rights reserved.

Date of release: 2 January 2007 Document identifier: 2PD2150