IP5311CX5

Dual-channel integrated passive filter network with ESD protection to IEC 61000-4-2 level 4

Rev. 2 — 23 December 2010 Product data sheet

1. Product profile

1.1 General description

IP5311CX5 is a dual-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals in the 10 MHz to 6000 MHz frequency band. In addition, IP5311CX5 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±15 kV contact according the IEC 61000-4-2 model, far exceeding standard level 4.

The device is optimized for loudspeaker applications using speakers of 10 Ω impedance and above.

IP5311CX5 is fabricated using monolithic silicon technology and integrates several resistors, bidirectional diodes and two high density capacitors in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP5311CX5 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

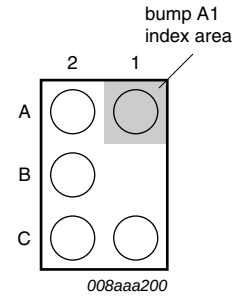
- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- Dual-channel integrated RC filter network with high density capacitors (2 × 5 nF)
- Integrated ESD protection withstanding ±15 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.4 mm pitch

1.3 Applications

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems

2. Pinning information

2.1 Pinning



transparent top view,
solder balls facing down

Fig 1. Pin configuration for WLCSP5

2.2 Pin description

Table 1. Pinning

Pin	Description
A1	filter channel 1 internal 2 kV amplifier connection
A2	filter channel 1 external 15 kV speaker connection
C1	filter channel 2 internal 2 kV amplifier connection
C2	filter channel 2 external 15 kV speaker connection
B1	not connected (missing ball)
B2	ground

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP5311CX5/LF[1]	WLCSP5	wafer level chip-size package; 5 bumps; 1.16 × 0.8 × 0.61 mm	IP5311CX5/LF
IP5311CX5/LF/P[2]	WLCSP5	wafer level chip-size package; 5 bumps; 1.16 × 0.8 × 0.61 mm	IP5311CX5/LF/P

[1] Lead-free.

[2] Lead-free and sol pearls.

4. Functional diagram

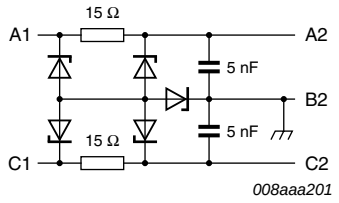


Fig 2. Schematic diagram IP5311CX5

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			−0.5	+4.5	V
V_{ESD}	electrostatic discharge voltage	pins A2 and C2 to ground				
		contact discharge	[1]	−15	+15	kV
		air discharge	[1]	−15	+15	kV
		IEC 61000-4-2 level 4; pins A2 and C2 to ground				
		contact discharge		−8	+8	kV
		air discharge		−15	+15	kV
		IEC 61000-4-2 level 1; pins A1 and C1 to ground				
		contact discharge		−2	+2	kV
		air discharge		−2	+2	kV
I_{ch}	channel current (DC)			-	92	mA
P_{ch}	channel power dissipation	continuous power		-	100	mW
P_{tot}	total power dissipation	continuous power		-	200	mW
T_{stg}	storage temperature			−55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			−35	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance			13.5	15	16.5	Ω
C_1	capacitance 1	high density; $V_{bias(DC)}$ = 0 V; f = 100 kHz		4	5	6	nF
C_2	capacitance 2			4	5	6	nF
C_d	diode capacitance	$V_{bias(DC)}$ = 0 V; f = 100 kHz	[1]	-	14	-	pF
V_{BR}	breakdown voltage	positive direction; I_{test} = 1 mA		14	16.5	-	V
		negative direction; I_{test} = −1 mA		-	−16.5	−14	V
I_{LR}	reverse leakage current	per channel; V_I = 3.0 V		-	-	60	nA
		per channel; V_I = −3.0 V		−60	-	-	nA

[1] Guaranteed by design.

7. Application information

7.1 Insertion loss

The insertion loss measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP5311CX5 is shown in Figure 3.

The insertion loss of both channels at frequencies up to 6 GHz is displayed in Figure 4.

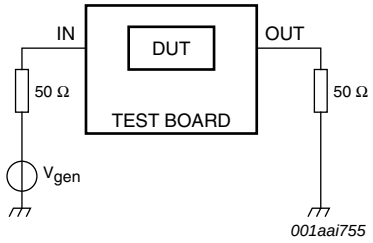
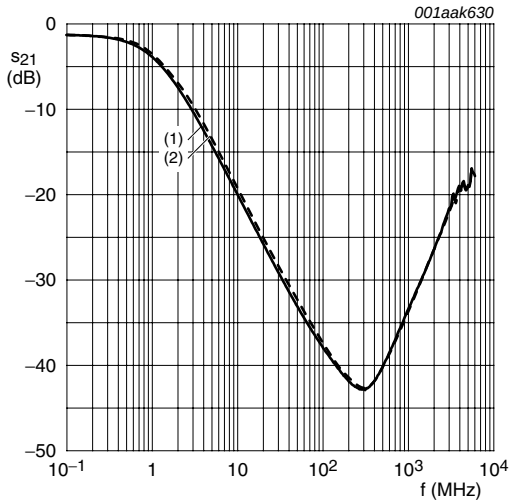


Fig 3. Frequency response measurement configuration



(1) Channel 1 (pins A1 and A2).

(2) Channel 2 (pins C1 and C2).

Fig 4. Measured insertion loss magnitudes

7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NWA system for evaluation of the IP5311CX5 is shown in Figure 5.

The measured crosstalk within the IP5311CX5 in a 50 Ω NWA system from one channel to the other channel is shown in Figure 6. In all cases, unused connections are terminated with 50 Ω to ground.

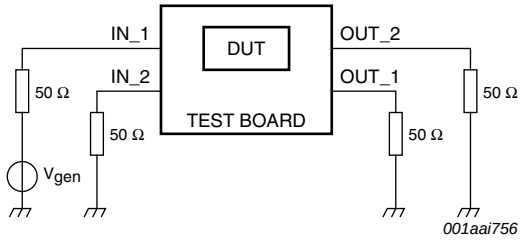
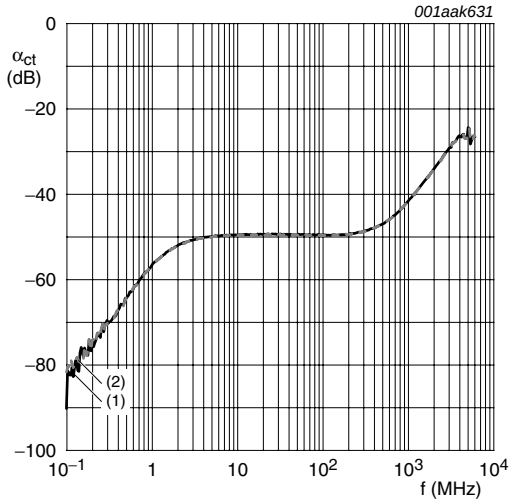


Fig 5. Crosstalk measurement configuration



(1) Channel 1 to channel 2 (pins A1 and C2).

(2) Channel 2 to channel 1 (pins A2 and C1).

Fig 6. Measured crosstalk between adjacent channels

7.3 Voltage dependency of high density capacitors

The high density capacitors integrated in IP5311CX5 show a voltage dependency similar to some higher value discrete ceramic capacitors.

When used in an average mobile application, the typical voltage swing across the capacitance will be in the range of −0.5 V to +4 V. In this event, the capacitor values change proportional to the bias voltage as depicted in Figure 7.

The measurement is performed several times, starting at the 'starting point' at 0 V, increasing to 4 V (arrow 1), decreasing to −0.5 V (following arrow 2) and back to +4 V (arrow 3).

When measuring the capacitance over voltage for voltage swings of e.g. −20 V to +20 V, a hysteresis in the capacitance over $V_{bias(DC)}$ can be observed (see Figure 8), which is inherent to the integration process for the high density capacitors in this product.

Again, the measurement starts at 'starting point', following arrow 1 up to $V_{bias(DC)}$ = 20 V, from there along arrow 2 down to $V_{bias(DC)}$ = −20 V and back via arrow 3 and arrow 4.

Values of C_1 and C_2 specified in Table 4 are based on measurements at the starting point.

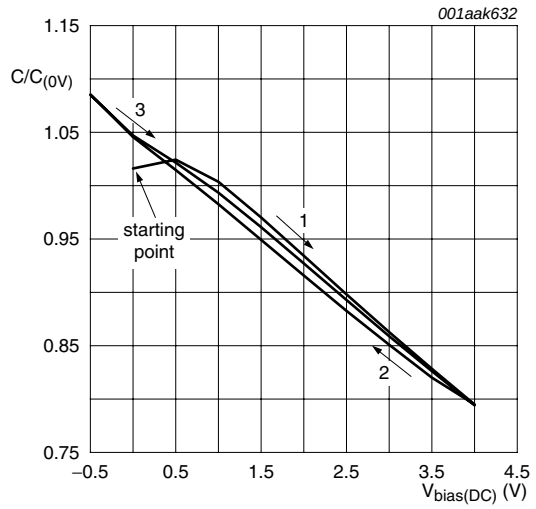


Fig 7. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-0.5\ V \leq V_{bias(DC)} \leq +4\ V$

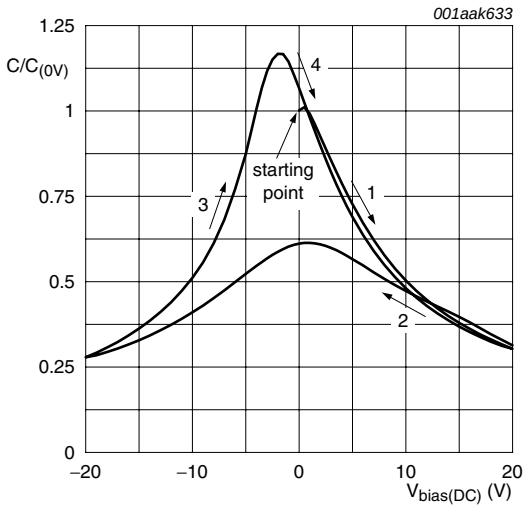


Fig 8. Relative capacitance $C/C_{(0V)}$ of high density capacitors for $-20\ V \leq V_{bias(DC)} \leq +20\ V$

8. Package outline

WLCSP5: wafer level chip-size package; 5 bumps (2 x 3 - B1)

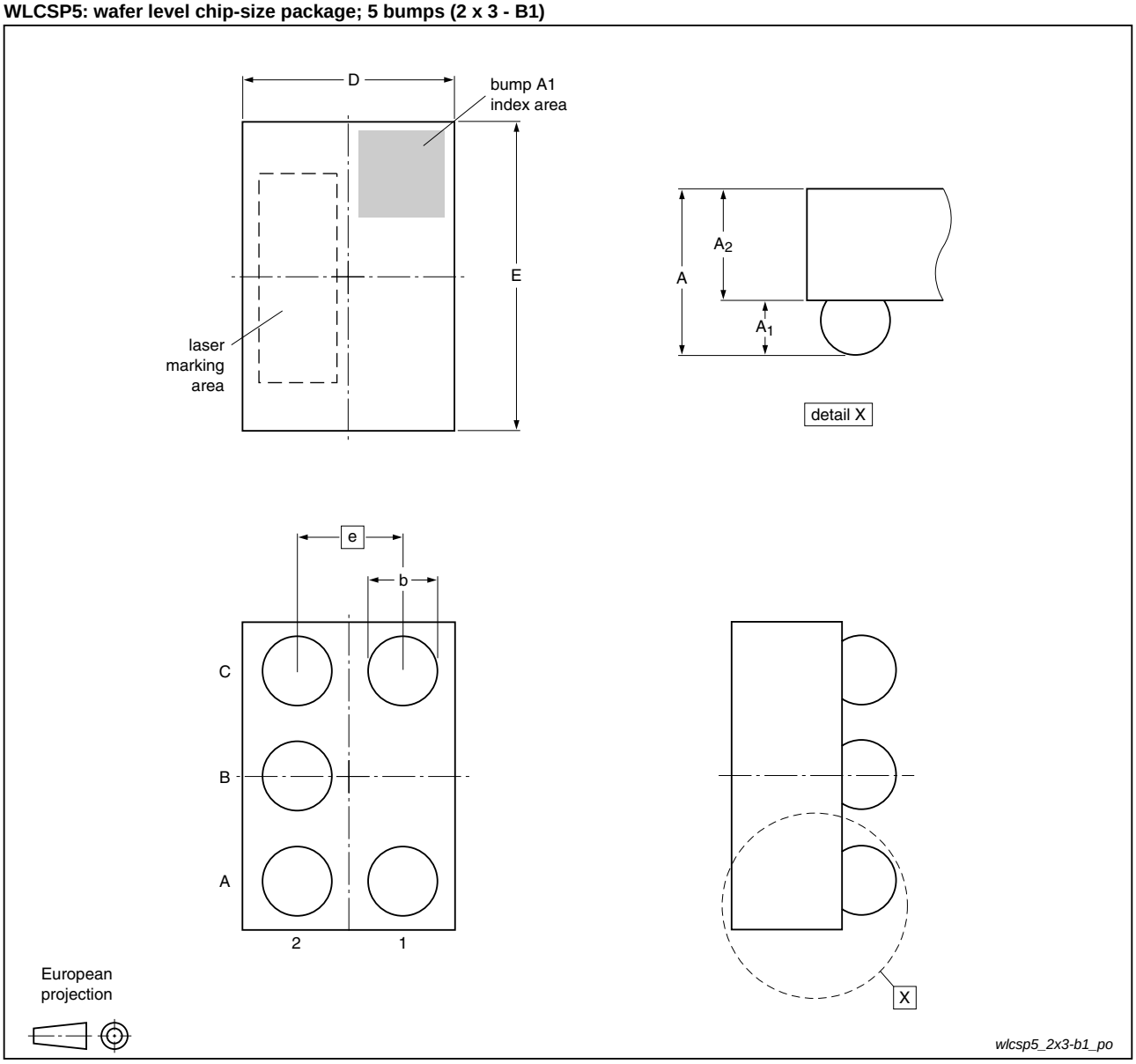


Fig 9. Package outline IP5311CX5/LF (WLCSP5)

Table 5. Dimensions for Figure 9

Symbol	Min	Typ	Max	Unit
A	0.57	0.61	0.65	mm
A_1	0.18	0.20	0.22	mm
A_2	0.39	0.41	0.43	mm
b	0.21	0.26	0.31	mm
D	0.75	0.80	0.85	mm
E	1.11	1.16	1.21	mm
e	-	0.4	-	mm

9. Design and assembly recommendations

9.1 PCB design guidelines

It is recommended, for optimum performance, to use a Non-Solder Mask Defined (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. Refer to Table 6 for the recommended PCB design parameters.

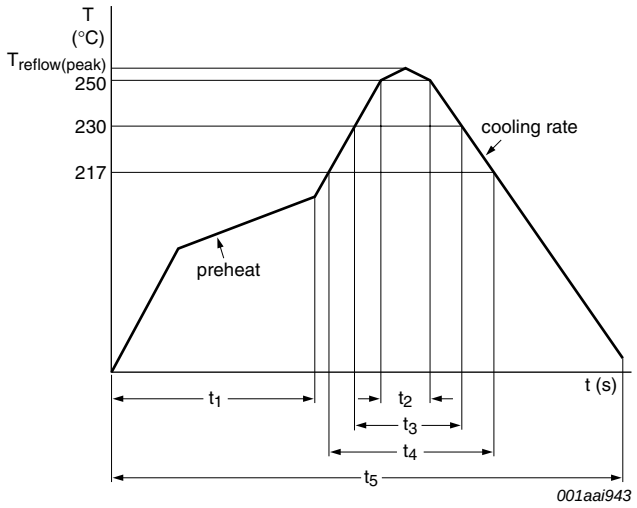
Table 6. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 7. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	325 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %); Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 10



The device is capable of withstanding at least three reflows of this profile.

Fig 10. Pb-free solder reflow profile

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
DUT	Device Under Test
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
LAN	Local Area Network
NSMD	Non-Solder Mask Defined
NWA	NetWork Analyzer
PCB	Printed-Circuit Board
PCS	Personal Communication System
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP5311CX5 v.2	20101223	Product data sheet	-	IP5311CX5 v.1
Modifications:	• Figure 1: changed • Figure 9: changed			
IP5311CX5 v.1	20091130	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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