

1. Product : Transistors with leadfree plating

2. Compliance standards : JEDEC STANDARD

3. Method : JEDEC, JESD201A, JESD22A121 standard.

(1) Sample size

A minimum of 96 terminations from a minimum quantity of 3 plating lots, 2 samples from each lot per each described precondition treatments per stress test.

* In case of big terminal component, it can be reduced a number of socket,

(2) Class level

Class 3: Mission/Life critical applications such as military and aerospace
Pure tin and high tin content alloys are not typically acceptable

Class 2: Business critical applications such as Telecom Infrastructure equipment,
High-end Servers, Automotive, etc.

Class 1: Industrial / consumer products

Class 1A: Consumer products

(3) Test procedures

Stress Type		Precondition Treatment	Total Duration	
			Class 1 and 2 Products	Class 1A Products
Temperature Cycling	-55 +0/-10 °C 85 +10/-0 °C	Depend on Components	1500cyc	1000cyc
Temperature / Humidity Storage	30 ±2°C 60 ±3% RH		4000hr	1000hr
High Temperature Humidity Storage	55 ±3°C 85 ±3% RH		4000hr	1000hr

(4) Criteria

Component Type	Class 2	Class 1	Class 1A
2 Lead SMD Components	40 μ m for Temperature/Humidity Storage and High Temperature/Humidity Storage	67μ m	50 μ m for Temperature Cycling and High Temperature/Humidity Storage 20 μ m for Temperature/Humidity
Multi-Leaded Components		67μ m	
High Frequency Components		50μ m	
Components with a minimum lead-to-lead gap >320 μ m	45 μ m for Temperature Cycling	100μ m	75μ m

4. Whisker Test result

(1) Samples : Leadfree plating products were selected as samples.

The samples are selected for each kind of plating material, terminal material and plating method (electrical, dip)

(2) Criteria : It could be verified anti whisker or not, which is satisfied with criteria of JESD201A Class 2, 1, 1A.

(3) Result : It can be confirmed anti whisker which is satisfied by Class 2, 1, 1A as in the following next page.

Test result (Transistor)

Package	Frame material		External lead treatment		NG Judge (pcs)
	Base material	Internal lead plating	Method	Composition ratio	
VMT3 EMT5 EMT6 WEMT6 UMT5 UMT6	FeNi42Alloy	Cu plating	Electricity plating	Sn-2Cu	0
VMT3 VMT6 EMT3F UMT3F SST3	FeNi42Alloy	Cu plating	Electricity plating	Sn	0
EMT3 UMT3 SMT3 SMT5 SMT6 SST3	FeNi42Alloy	Cu plating	Dip	Sn-3Ag-0.5Cu	0
TUMT3 TUMT5 TUMT6 TSMT8 TSST8 SOP8 MPT3 MPT6 CPT3 TCPT3 LPTS LPTL TO247	Cu	-	Electricity plating	Sn-2Cu	0
VML0806 VML1006 HUML2020 HSML3030 TO252 TO3PF SOP8 HSOP8 HSMT8 TSMT3 TSMT5 TSMT6 TSMT8 MPT3	Cu	-	Electricity plating	Sn	0
TSMT3 TSMT5 TSMT6 TO-220FM TO-220FN	Cu	-	Dip	Sn-3Ag-0.5Cu	0

Notes

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