



PJQ2405-AU

20V P-Channel Enhancement Mode MOSFET

Voltage -20 V **Current** -7.2A

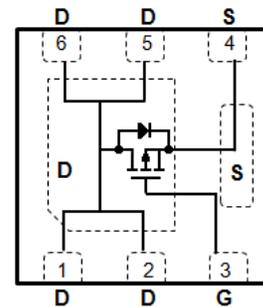
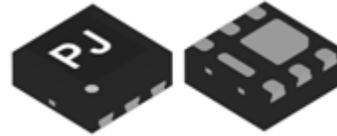
Features

- $R_{DS(ON)}$, $V_{GS}@-4.5V$, $I_D@-7.2A < 32m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-2.5V$, $I_D@-5.0A < 39m\Omega$
- $R_{DS(ON)}$, $V_{GS}@-1.8V$, $I_D@-2.5A < 48m\Omega$
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- AEC-Q101 qualified
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case : DFN2020B-6L Package
- Terminals : Solderable per MIL-STD-750, Method 2026
- Approx. Weight : 0.0003 ounces, 0.0086 grams

DFN2020B-6L



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS	
Drain-Source Voltage	V_{DS}	-20	V	
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current (Note 4)	I_D	-7.2	A	
Pulsed Drain Current (Note 1)	I_{DM}	-28.8		
Power Dissipation	P_D	$T_a=25^\circ\text{C}$	2.8	W
		Derate above 25°C	22	mW/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$	
Typical Thermal Resistance	$R_{\theta JA}$	44.6	$^\circ\text{C}/\text{W}$	
- Junction to Ambient, $t < 10s$ (Note 4,5)				



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Electrical Characteristics (T_A=25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250uA	-20	-	-	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.35	-0.6	-0.9	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-7.2A	-	25	32	mΩ
		V _{GS} =-2.5V, I _D =-5A	-	30	39	
		V _{GS} =-1.8V, I _D =-2.5A	-	35	48	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V	-	-	-1	uA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V	-	-	±100	nA
Dynamic (Note 6)						
Total Gate Charge	Q _g	V _{DS} =-10V, I _D =-7.2A, V _{GS} =-4.5V (Note 2,3)	-	18.9	-	nC
Gate-Source Charge	Q _{gs}		-	2.8	-	
Gate-Drain Charge	Q _{gd}		-	4.2	-	
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ	-	1785	-	pF
Output Capacitance	C _{oss}		-	152	-	
Reverse Transfer Capacitance	C _{rss}		-	125	-	
Turn-On Delay Time	t _{d(on)}	V _{DS} =-10V, I _D =-7.2A, V _{GEN} =-4.5V, R _L =10Ω R _G =6Ω (Note 2,3)	-	12	-	ns
Turn-On Rise Time	t _r		-	68	-	
Turn-Off Delay Time	t _{d(off)}		-	82	-	
Turn-Off Fall Time	t _f		-	35	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I _s	---	-	-	-1.5	A
Diode Forward Voltage	V _{SD}	I _s =-1A, V _{GS} =0V	-	-0.64	-1.2	V

NOTES :

1. Pulse width ≤ 300us, Duty cycle ≤ 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.
4. The maximum current rating is package limited.
5. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.



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TYPICAL CHARACTERISTIC CURVES

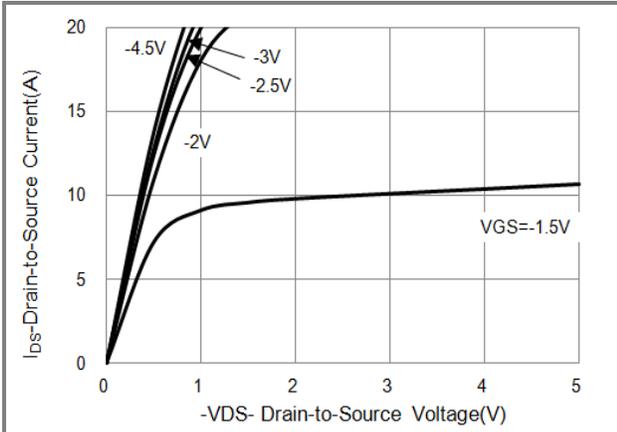


Fig.1 On-Region Characteristics

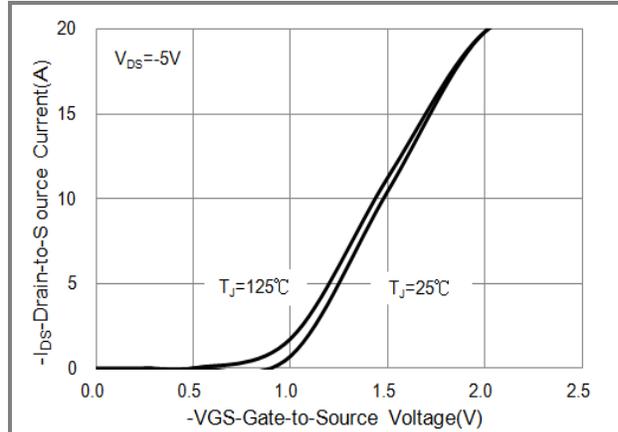


Fig.2 Transfer Characteristics

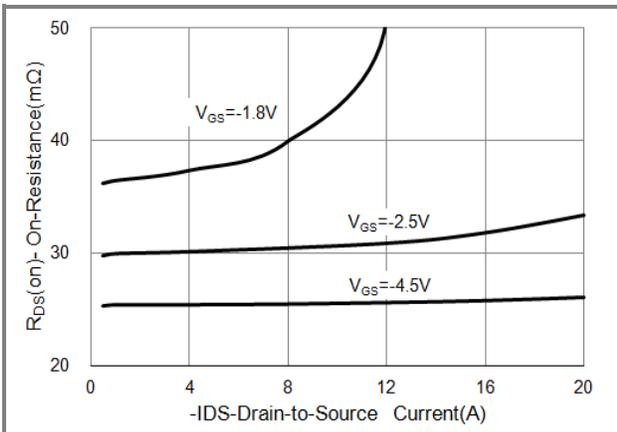


Fig.3 On-Resistance vs. Drain Current

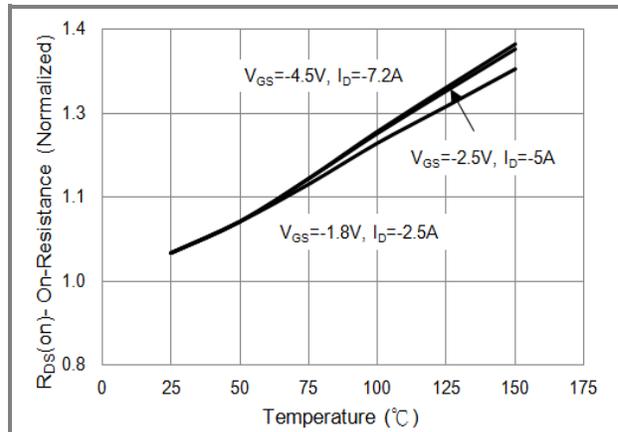


Fig.4 On-Resistance vs. Junction temperature

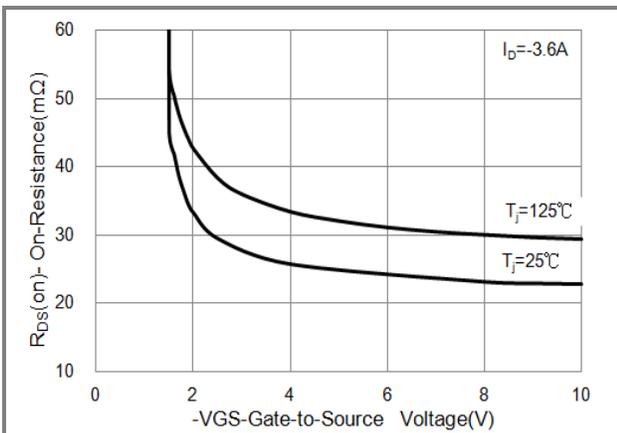


Fig.5 On-Resistance Variation with V_{GS}

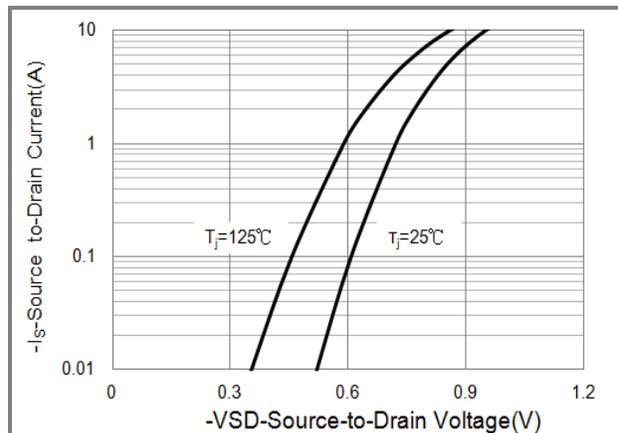


Fig.6 Body Diode Characteristics



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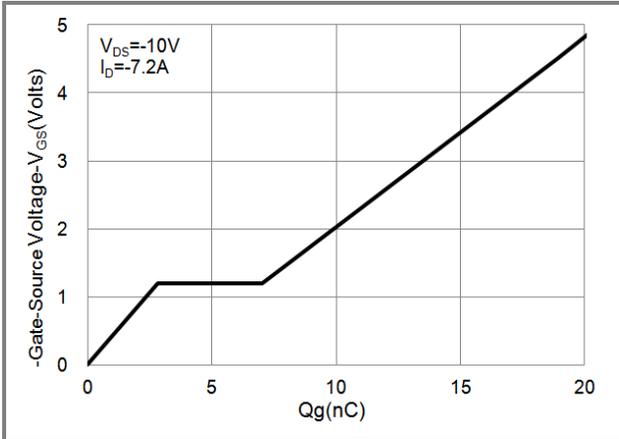


Fig.7 Gate-Charge Characteristics

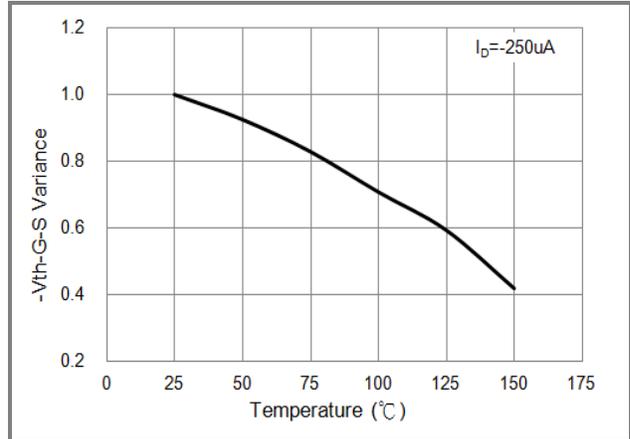


Fig.8 Threshold Voltage Variation with Temperature

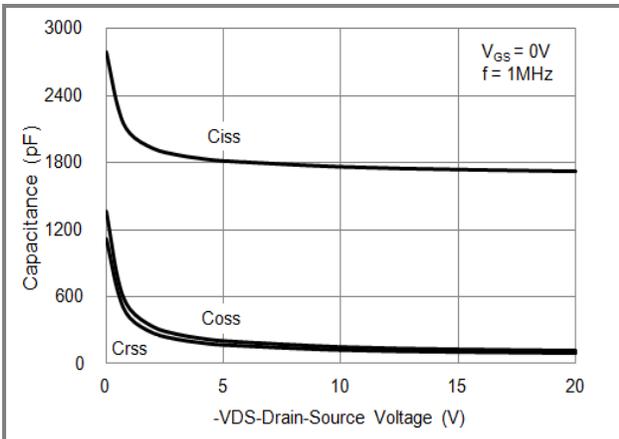


Fig.9 Capacitance vs. Drain-Source Voltage



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