CDB4349

Evaluation Board for CS4349

Features

- Stand-Alone or PC GUI Board Control
- CS8416 Receives S/PDIF-Compatible Digital Audio
- Headers for External PCM Audio Input
- Demonstrates Recommended Layout and Grounding Arrangements.
- Requires Only a Digital Signal Source and Power Supplies for a Complete Digital-to-Analog Converter System

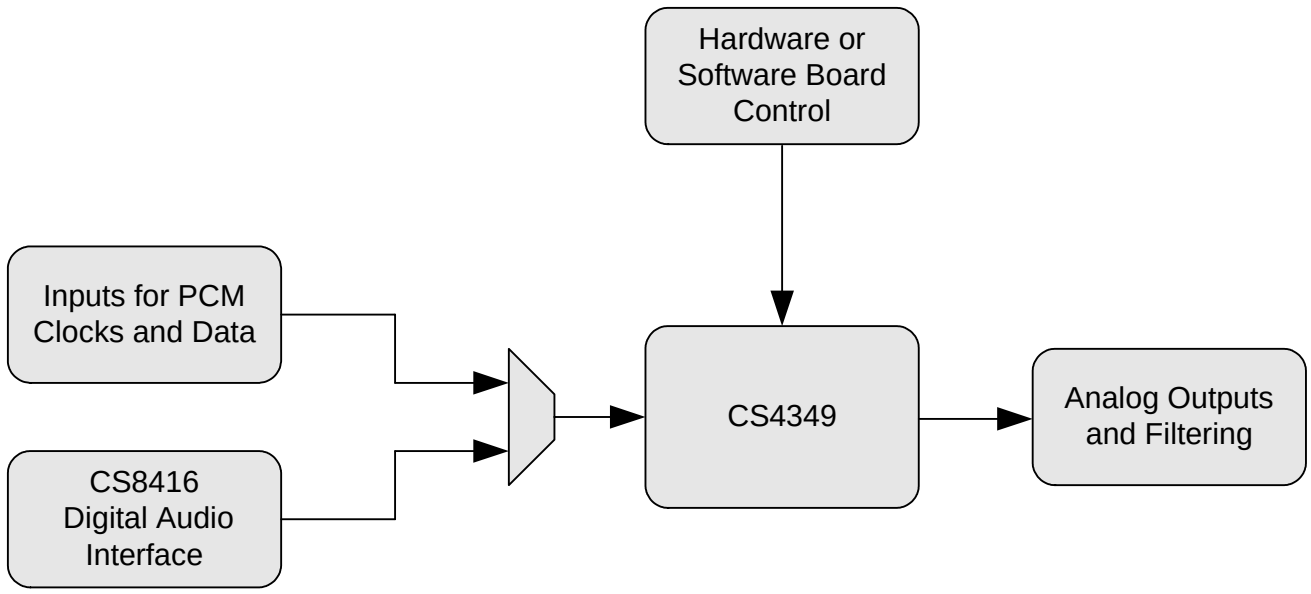
Description

The CDB4349 evaluation board is an excellent platform for quickly evaluating the CS4349 24-bit, 24-pin, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS4349 (only required for Control Port Mode), and a power supply. Analog line-level outputs are provided via RCA phono jacks.

The CS8416 digital audio receiver IC provides the system timing necessary to operate the digital-to-analog converter and will accept S/PDIF-compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4349	Evaluation Board



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1. CDB4349 SYSTEM OVERVIEW

The CDB4349 evaluation board is an excellent platform for quickly evaluating the CS4349. The CS8416 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply external PCM clocks and data through headers for system development.

The CDB4349 schematic has been partitioned into 6 pages, shown in Figures 35 through 40. Each schematic page is represented in the system diagram shown in Figure 34. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS4349 DIGITAL-TO-ANALOG CONVERTER

A description of the CS4349 is included in the CS4349 datasheet, available at http://www.cirrus.com/en/products/pro/detail/P1116.html.

3. CS8416 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8416 digital audio receiver (Figure 38). The outputs of the CS8416 include a serial bit clock, serial data, and a left-right clock. The CS8416 data format is selected through switch S1. The operation of the CS8416 and a discussion of the digital audio interface is included in the CS8416 datasheet, available at http://www.cirrus.com/en/products/pro/detail/P1005.html.

The CDB4349 has been designed so that the input can be either optical or coaxial (see Figure 39). However, both inputs cannot be driven simultaneously.

After the CS8416 serial format is changed either through S1 in Stand-Alone Mode, or though the CDB4349 GUI in PC Mode, a reset is required. The CS8416 can be manually reset using ‘HARDWARE RESET’ (S2) in Stand-Alone Mode, or through software when operating the CDB4349 in PC Mode.

4. INPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow external PCM data input through header J10. The schematic for the clock/data input is shown in Figure 37. In Stand-Alone Mode, switch position 6 of S4 selects the source as either CS8416 (open) or header J10 (closed). In PC Mode, the PCM source is selected through software.

5. INPUT FOR CONTROL DATA

The evaluation board can be run in either a Stand-Alone Mode or with a PC. Stand-Alone Mode does not require the use of a PC, and the mode pins are configured using switch positions 1 through 5 of S4 and switch positions 1 and 2 of S1. PC Mode uses software to set up the CS4349 through I²C® or SPI™ interface using the PC’s serial port or USB port. When the serial port (RS232) or USB is attached and the CDB4349 software is running, PC Mode is automatically selected.

Header J38 offers the option for external input of RST and SPI/I²C clocks and data. The board is set up from the factory to use the on-board microcontroller in conjunction with software available at http://www.cirrus.com/en/products/software/msaudio.html. To use an external control source, remove the shunts on J38 and place a ribbon cable so the signal lines are on the center row and the grounds are on the right side. R89 and R90 should be populated with 2 kΩ resistors when using an external I²C source which does not already provide pull-ups.

6. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by three binding posts (GND, +12V, and -12V), as shown in Figure 40. The '+12V' and '-12V' terminals supply the active output filters. The +3.3 V and +5.0 V circuitry is powered by regulators fed by the '+12V' terminal. Headers J3, J4, and J7 allow the user to either select +3.3 V or +5.0 V supplies for the various CS4349 voltage supply pins. Alternatively, the user can remove the shunts on J3, J4, and J7, and provide an external power supply.

WARNING: Refer to the CS4349 datasheet for maximum allowable voltage levels. Operation outside of this range can cause permanent damage to the device.

7. GROUNDING AND POWER SUPPLY DECOUPLING

As with any high-performance converter, the CS4349 requires careful attention to power supply and grounding arrangements in order to optimize performance. Figure 35 details the connections to the CS4349 while Figures 41, 42, and 43 show the component placement and top and bottom layout. The decoupling capacitors are located as close to the CS4349 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

8. ANALOG OUTPUT FILTERING

The passive output filter on the CDB4349 has been designed according to the CS4349 datasheet.

9. BOARD CONNECTIONS AND SETTINGS

Board connections and settings are shown in Table 1, Table 2, and Table 3.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
GND	Input	Ground connection from power supply
+12V	Input	+12 V positive supply for the on-board filtering
-12V	Input	-12 V negative supply for the on-board filtering
S/PDIF IN - J1	Input	Digital audio interface input via coax
S/PDIF IN - OPT1	Input	Digital audio interface input via optical
PCM INPUT - J10	Input	Input for master, serial, left/right clocks and serial data
POUTA, POUTB	Output	RCA line level analog outputs from passive output stage

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
J3, J4, J7	Selects Supply Voltage for CS4349	+5V *+3.3V	Supplies +5.0 V to associated CS4349 supply *Supplies +3.3 V to associated CS4349 supply
J38	Selects source of control data	*PC CONTROL shunts removed	*Control from PC and on-board microcontroller External control input using center and right columns
J27	C2 micro programming	-	Reserved for factory use only

Table 2. CDB4349 Jumper Settings

*Default Factory Settings.

SWITCH (Note 1)	PURPOSE	POSITION	FUNCTION SELECTED
S2	Resets CS8416 and CS4349		The CS8416 must be reset if switch S1 is changed
S1	CS8416 Format Select SFSEL[1:0]	1, 2	Default: SFSEL[1:0] = 00 (Closed). See CS8416 datasheet for details.
S4	CS4349 Format Select DIF[2:0]	1, 2, 3	Default: DIF[2:0] = 000 (Closed). See CS4349 datasheet for details.
	CS4349 De-emphasis Select	4	open = De-emphasis enabled *closed = De-emphasis disabled.
	CS4349 Popguard® Enable	5	open = Popguard enabled *closed = Popguard disabled.
	Selects PCM source for CS4349	6	*open = CS8416 closed = PCM Header J10

Table 3. CDB4349 Switch Settings

*Default Factory Settings.

Note:

1. Switch settings take effect in Stand-Alone Mode only.

10.PERFORMANCE PLOTS

Test conditions (unless otherwise specified): T_A = 25° C; Measurement bandwidth is 20 Hz to 20 kHz (unweighted); VA = 5 V; VLC = VLS = 3.3 V; Input signal is a 0 dBFS 1 kHz sine wave; Input data resolution is 24 bits, Left-Justified; Channel A output = blue traces; Channel B output = green traces.

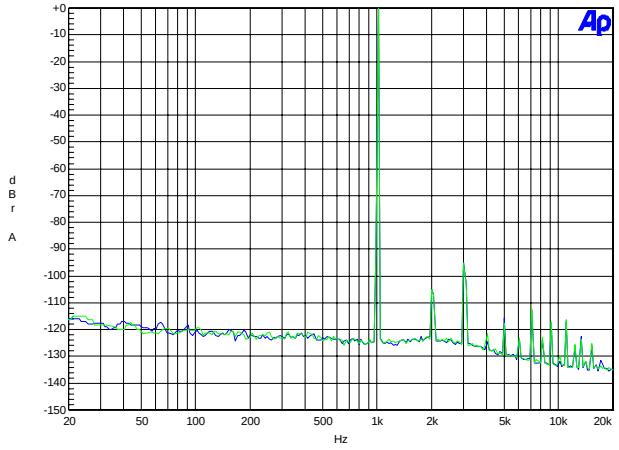


Figure 1. FFT 0 dBFS, FS = 48 kHz

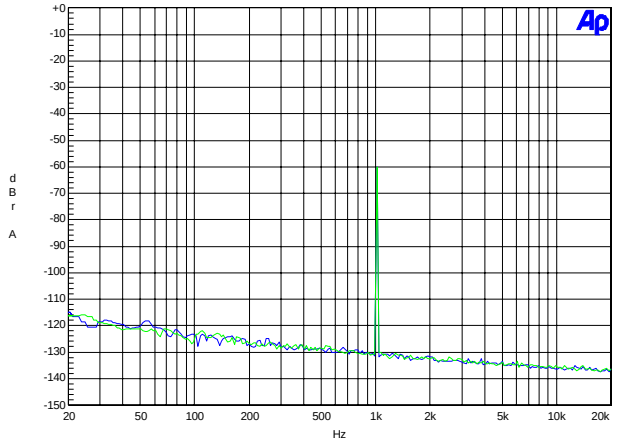


Figure 2. FFT -60 dBFS, FS = 48 kHz

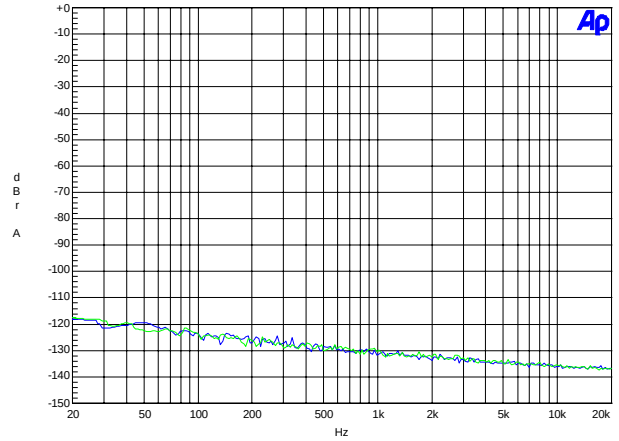


Figure 3. FFT No Input, FS = 48 kHz

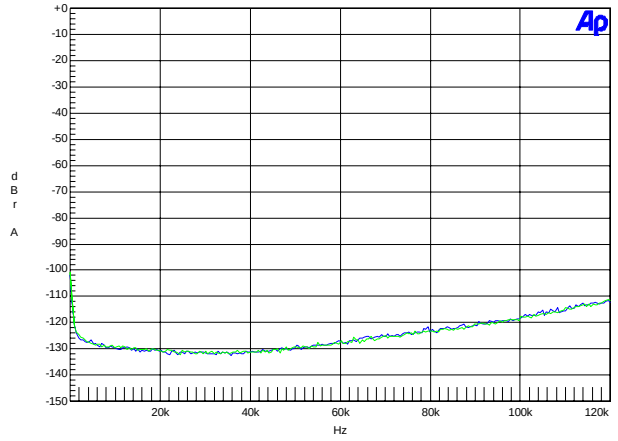


Figure 4. FFT No Input Out of Band, FS = 48 kHz

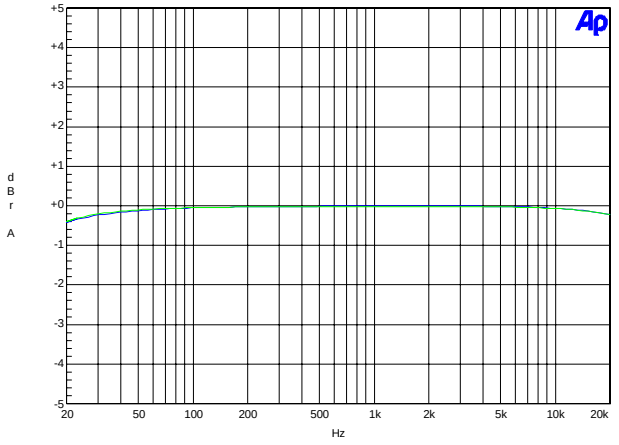


Figure 5. Frequency Response 0 dBFS, FS = 48 kHz

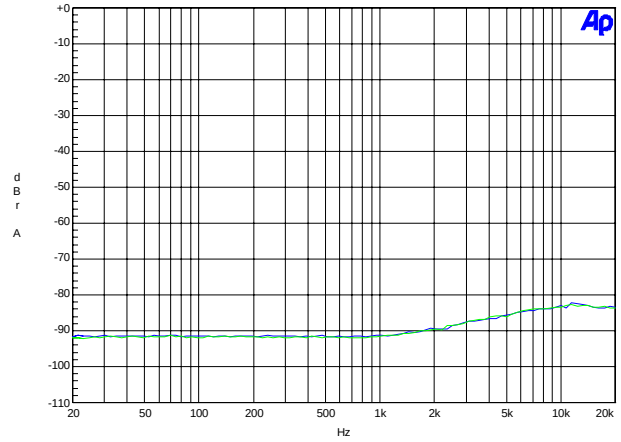


Figure 6. THD+N vs Frequency 0 dBFS, FS = 48 kHz

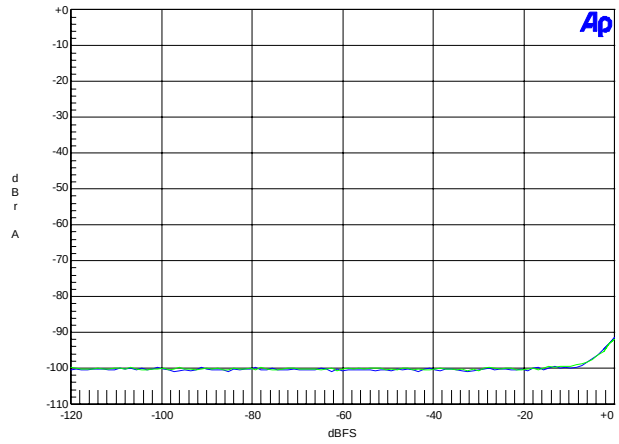


Figure 7. THD+N vs Level 1 kHz, FS = 48 kHz

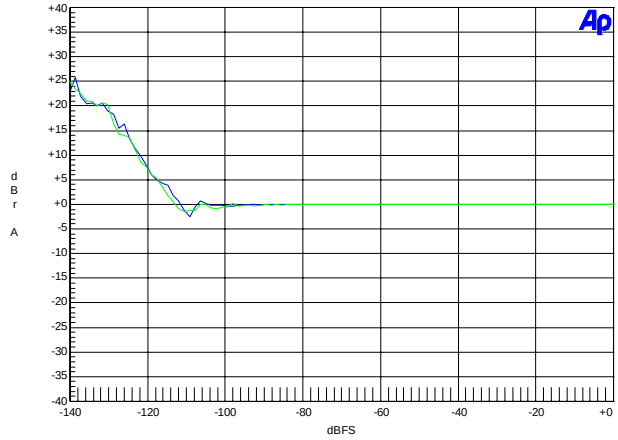


Figure 8. Fade-to-Noise Linearity 1 kHz, FS = 48 kHz

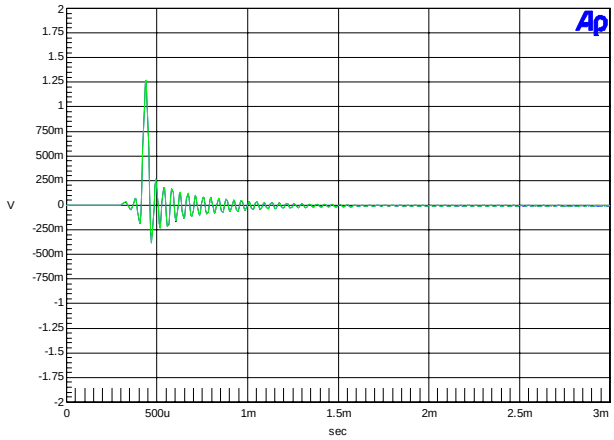


Figure 9. Impulse Response, FS = 48 kHz

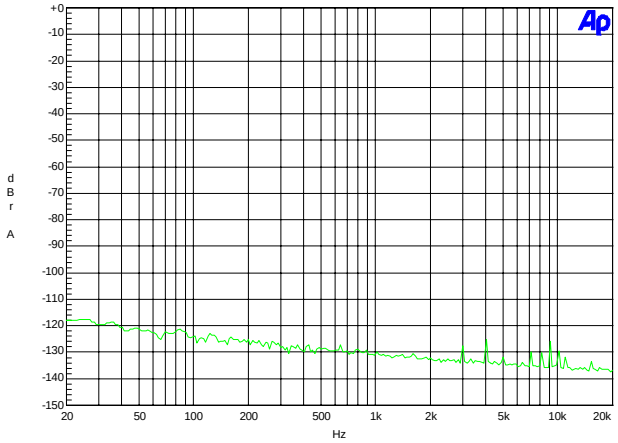


Figure 10. FFT Crosstalk Ch. A to Ch. B 1 kHz, FS = 48 kHz

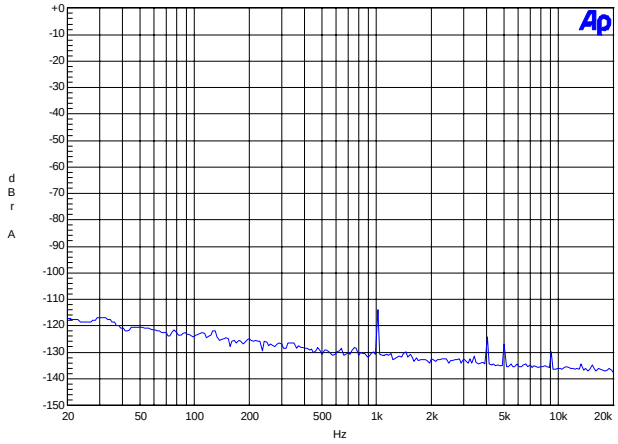


Figure 11. FFT Crosstalk Ch. B to Ch. A 1 kHz, FS = 48 kHz

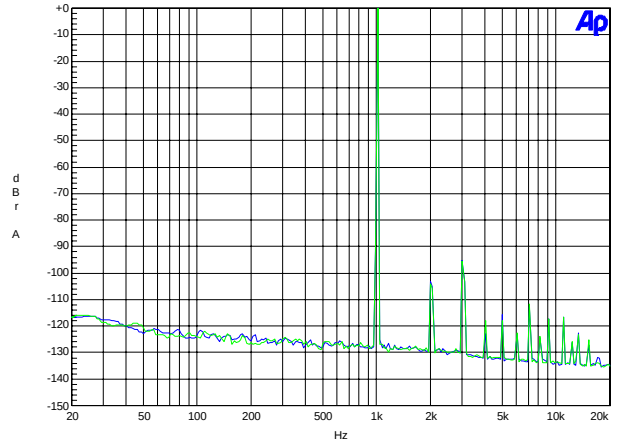


Figure 12. FFT 0 dBFS, FS = 96 kHz

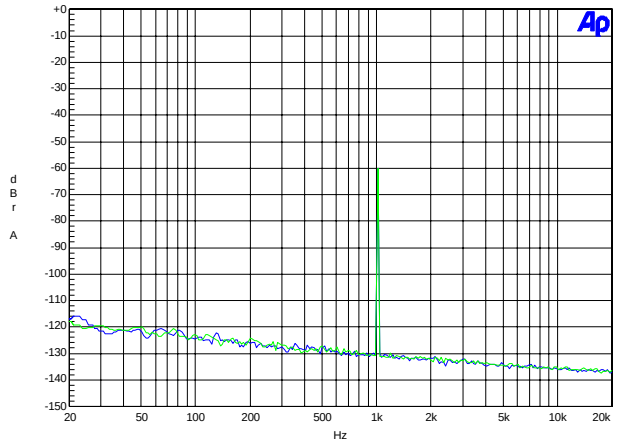


Figure 13. FFT -60 dBFS, FS = 96 kHz

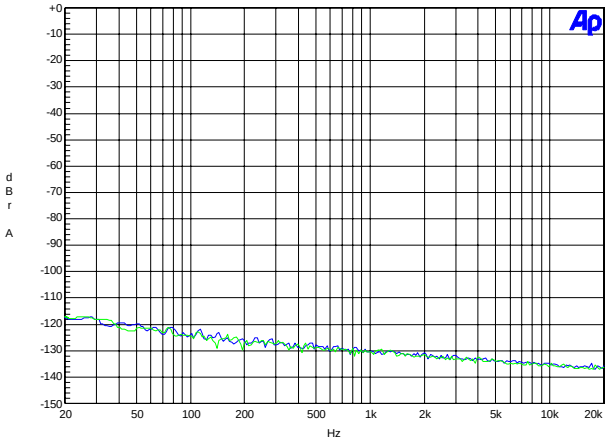


Figure 14. FFT No Input, FS = 96 kHz

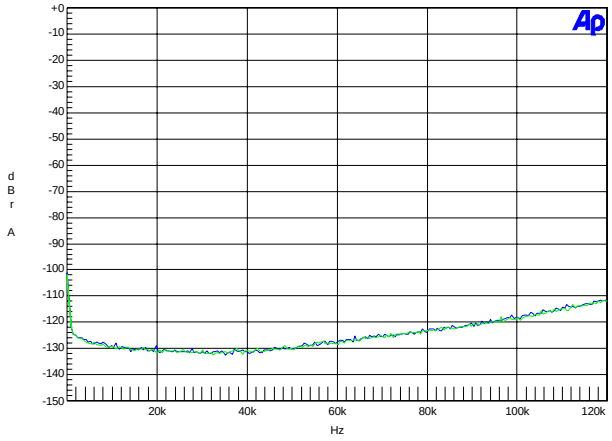


Figure 15. FFT No Input Out of Band, FS = 96 kHz

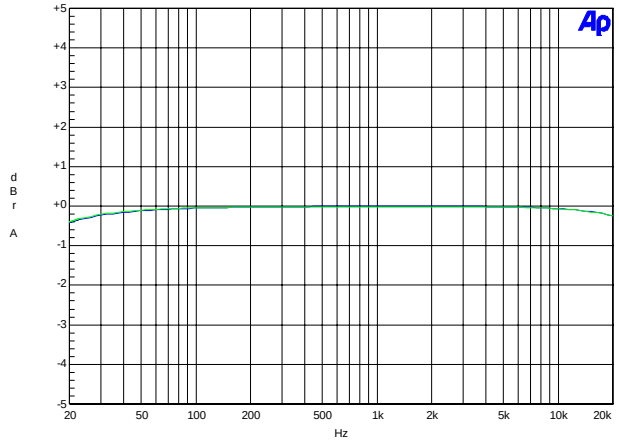


Figure 16. Frequency Response 0 dBFS, FS = 96 kHz

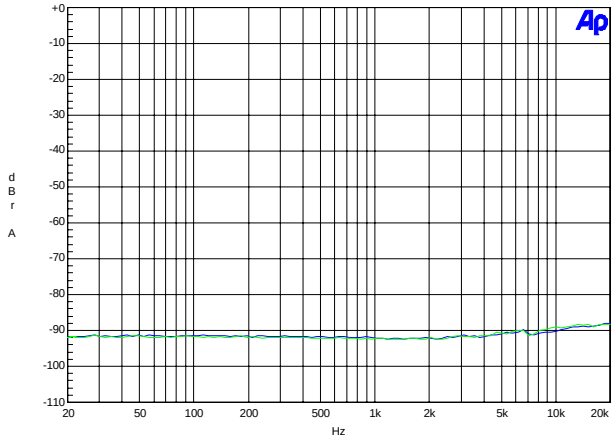


Figure 17. THD+N vs Frequency 0 dBFS, FS = 96 kHz

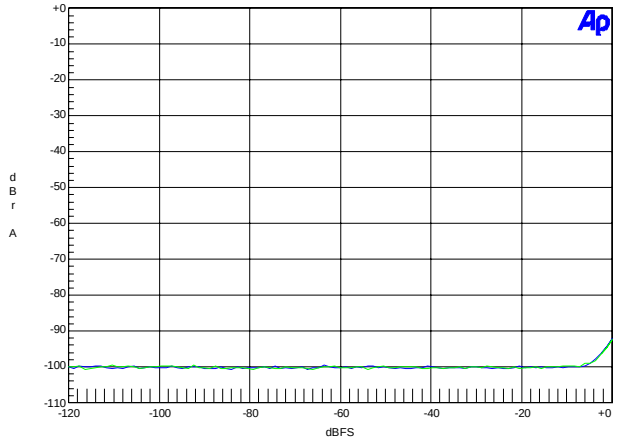


Figure 18. THD+N vs Level 1 kHz, FS = 96 kHz

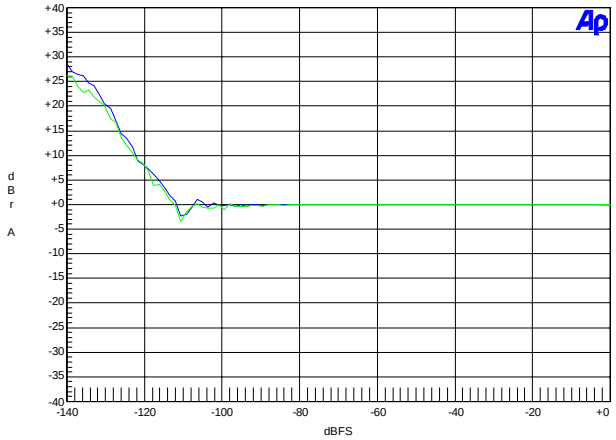


Figure 19. Fade-to-Noise Linearity 1 kHz, FS = 96 kHz

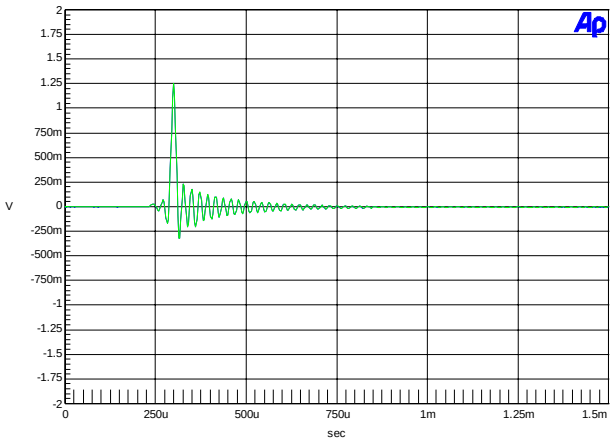


Figure 20. Impulse Response, FS = 96 kHz

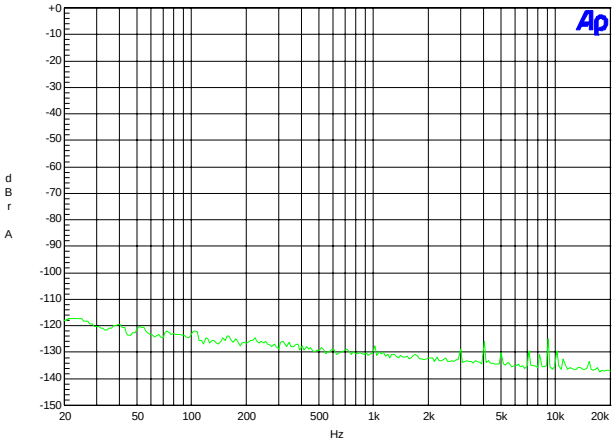


Figure 21. FFT Crosstalk Ch. A to Ch. B 1 kHz, FS = 96 kHz

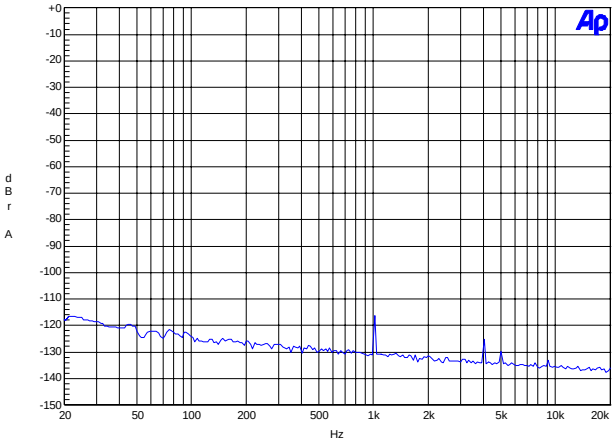


Figure 22. FFT Crosstalk Ch. B to Ch. A 1 kHz, FS = 96 kHz

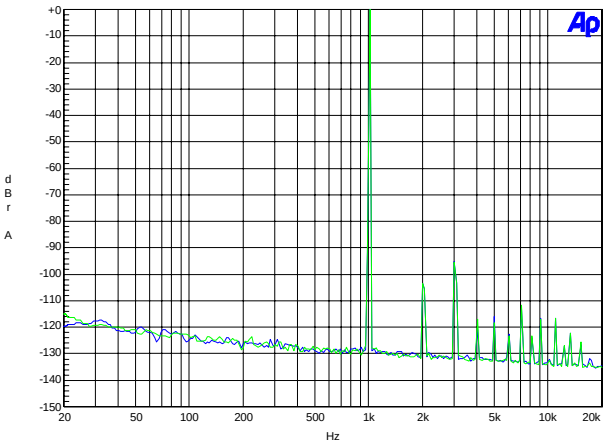


Figure 23. FFT 0 dBFS, FS = 192 kHz

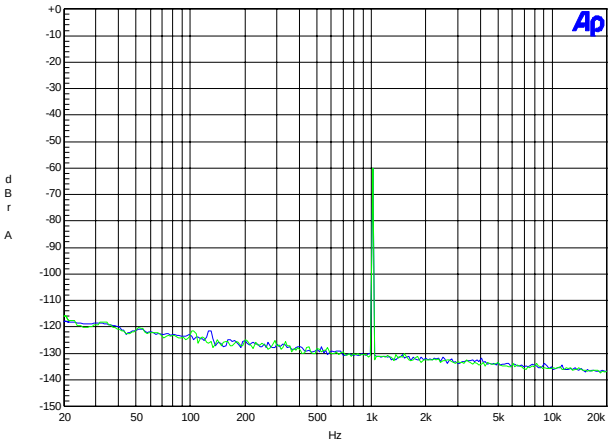


Figure 24. FFT -60 dBFS, FS = 192 kHz

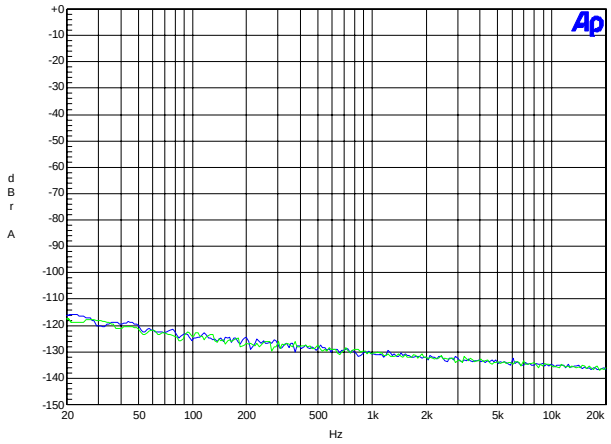


Figure 25. FFT No Input, FS = 192 kHz

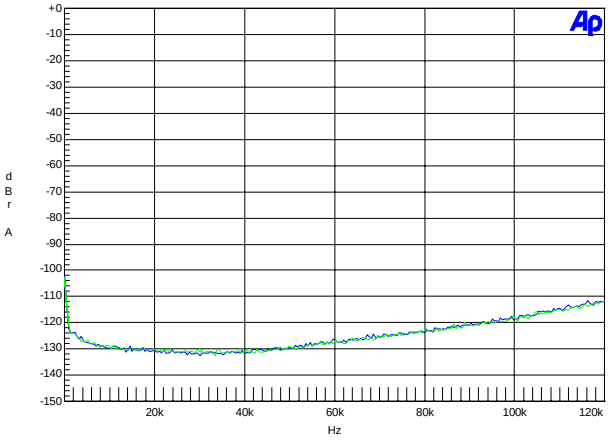


Figure 26. FFT No Input Out of Band, FS = 192 kHz

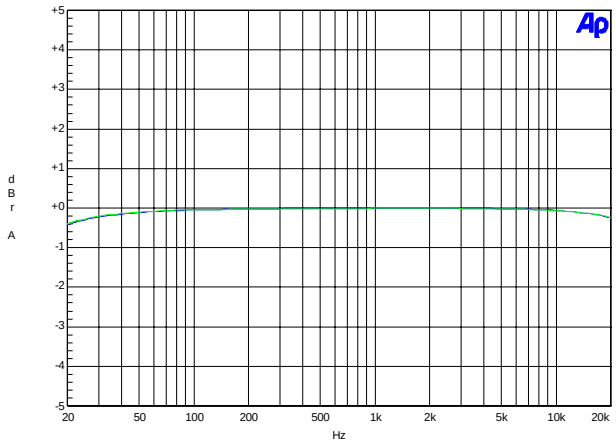


Figure 27. Frequency Response 0 dBFS, FS = 192 kHz

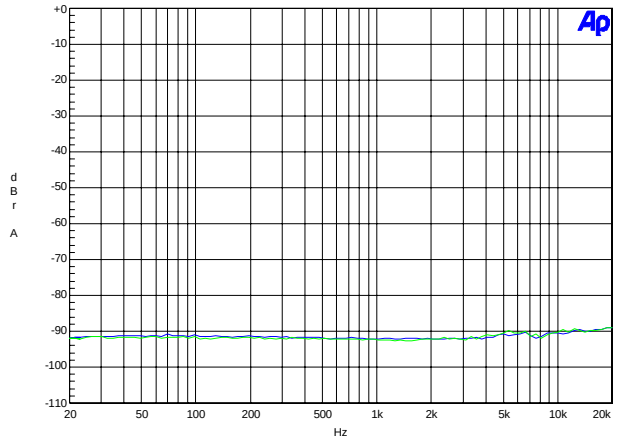


Figure 28. THD+N vs Frequency 0 dBFS, FS = 192 kHz

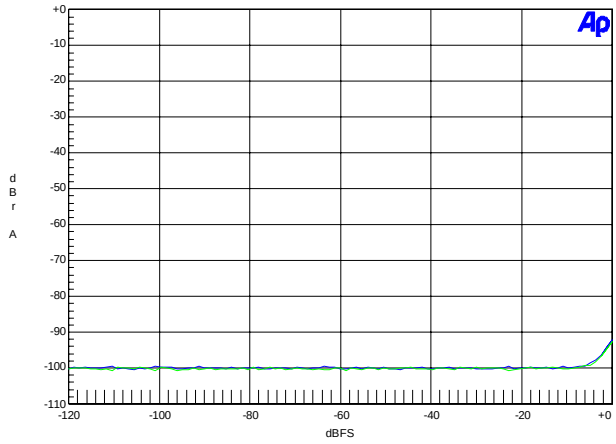


Figure 29. THD+N vs Level 1 kHz, FS = 192 kHz

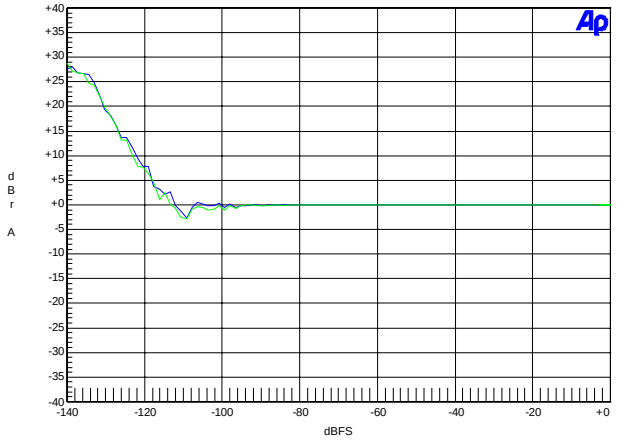


Figure 30. Fade-to-Noise Linearity 1 kHz, FS = 192 kHz

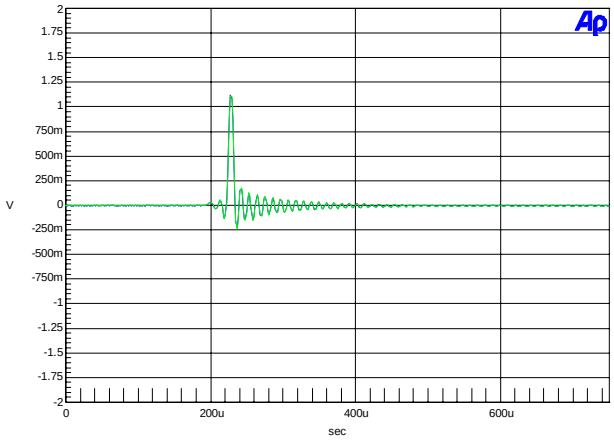


Figure 31. Impulse Response, FS = 192 kHz

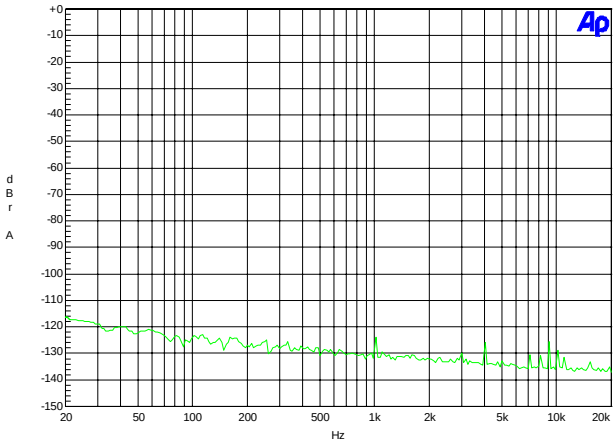


Figure 32. FFT Crosstalk Ch. A to Ch. B 1 kHz, FS = 192 kHz

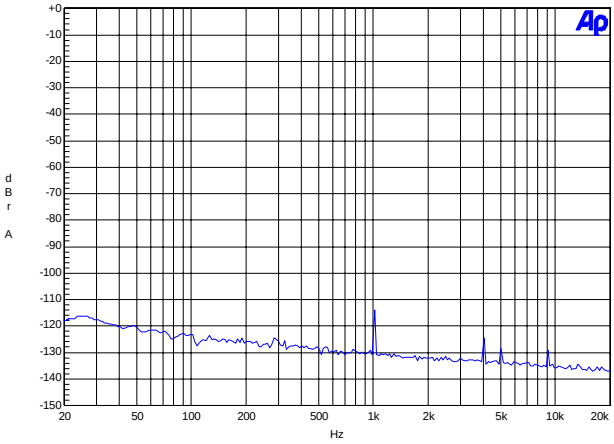


Figure 33. FFT Crosstalk Ch. B to Ch. A 1 kHz, FS = 192 kHz

11.SCHEMATICS

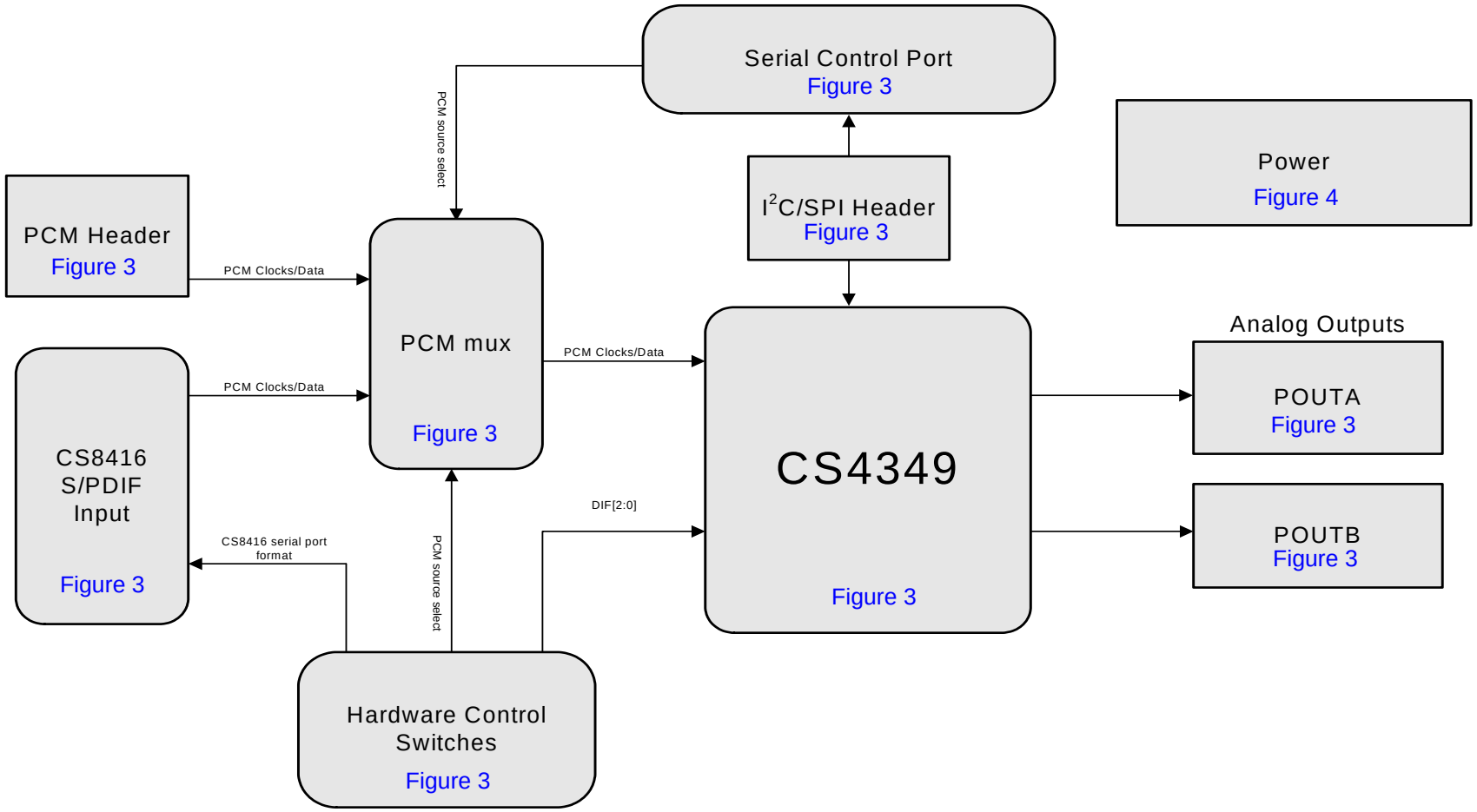


Figure 34. System Block Diagram and Signal Flow

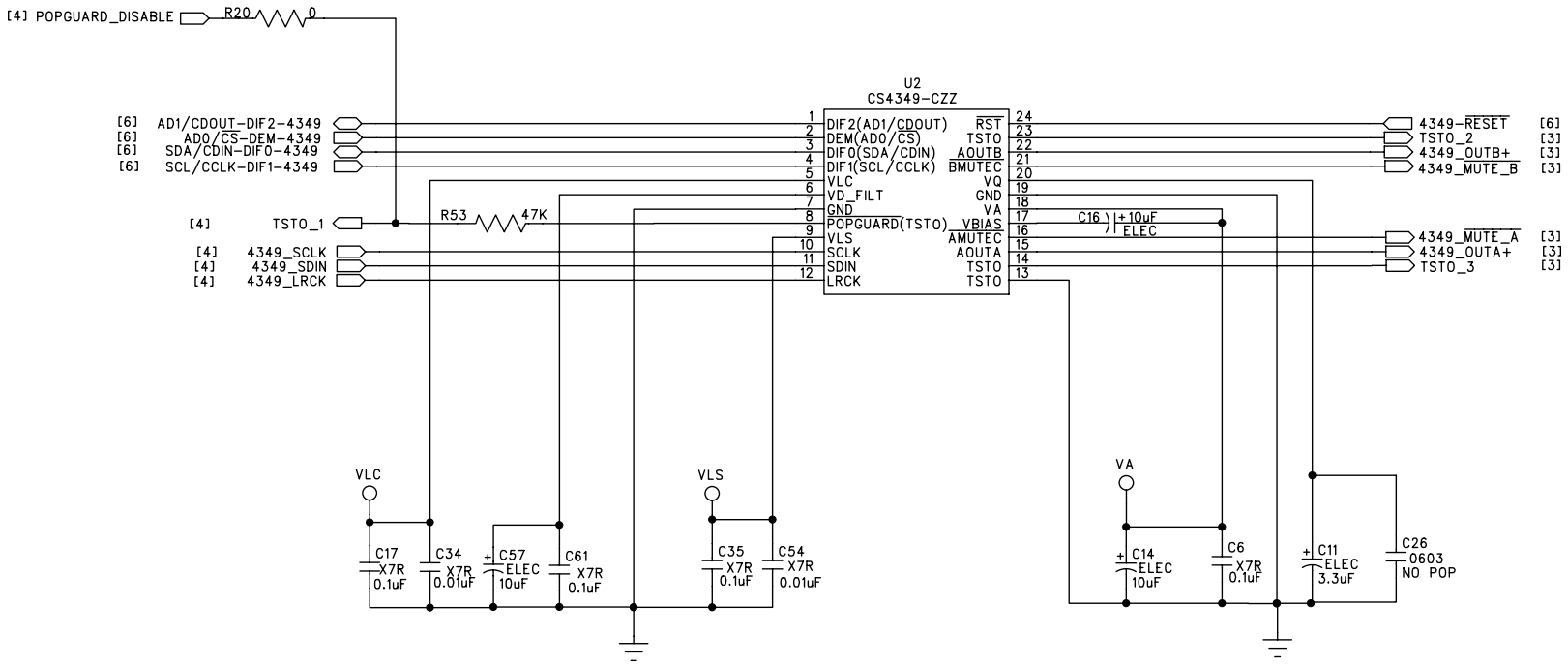


Figure 35. CS4349

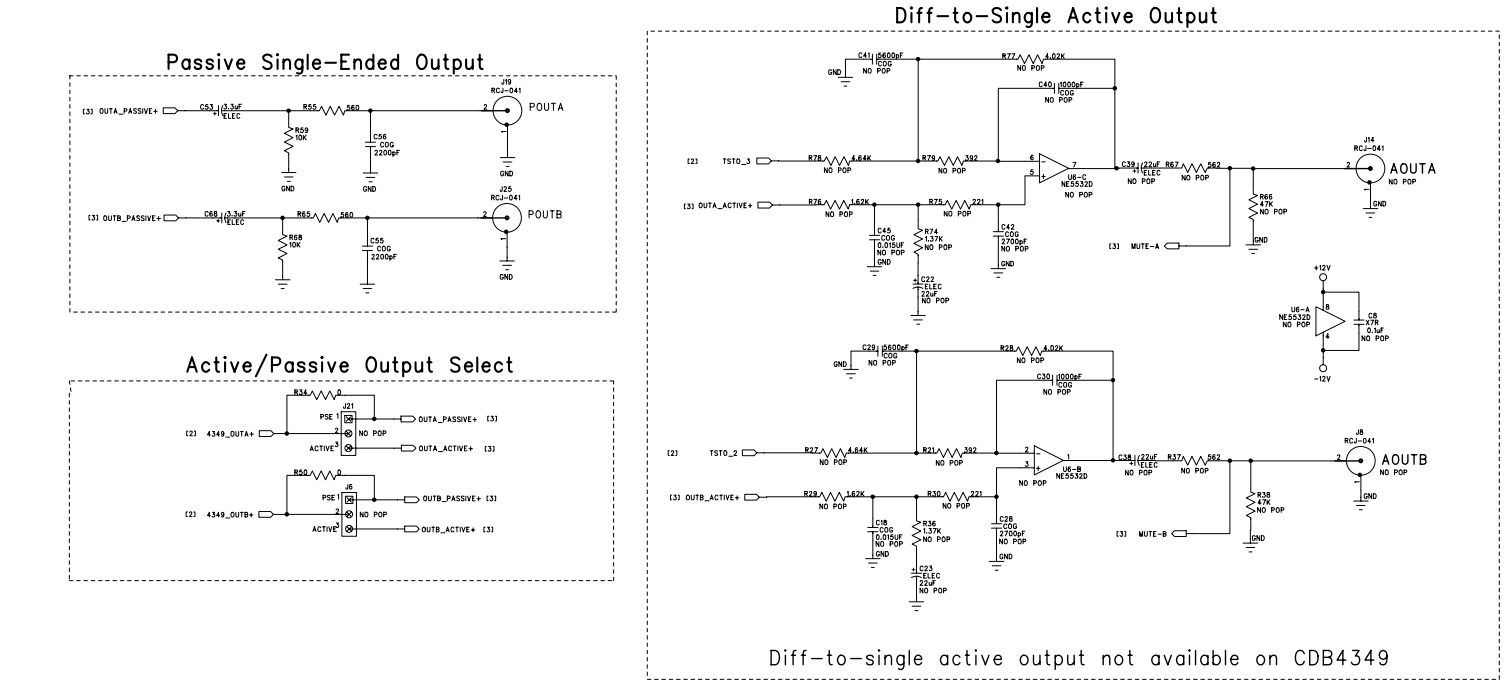
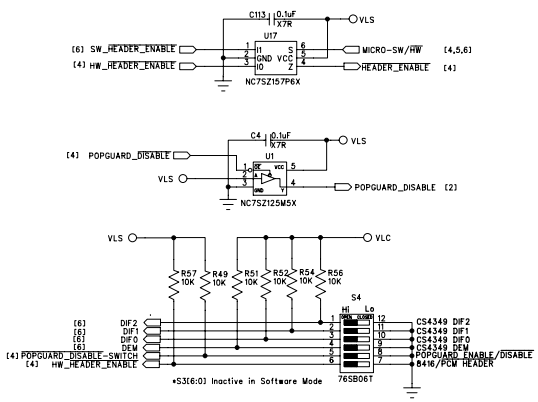


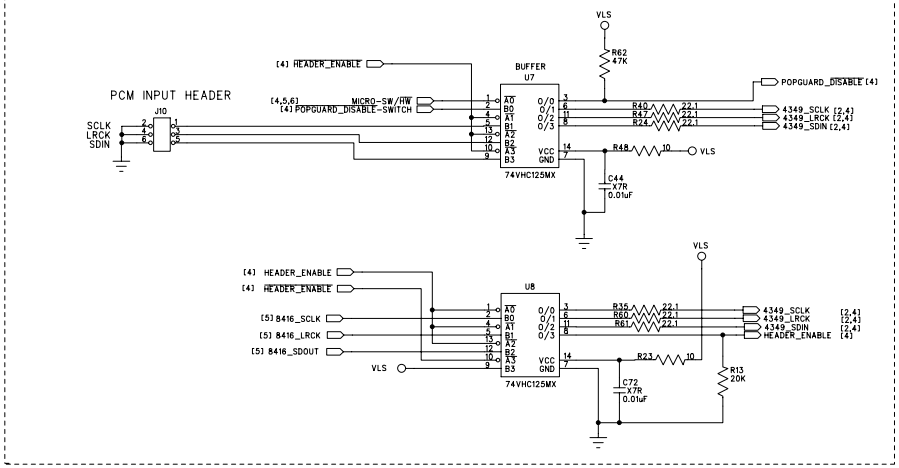
Figure 36. Analog Outputs

Control Signal Mux and Switch



DAC DIF[2:0]	
000	Left Justified
001	I2S
010	Right Justified 16-bit
011	Right Justified 24-bit
100	TDM slot 1
101	TDM slot 2
110	TDM slot 3
111	TDM slot 4

PCM Input Header Clock/Data Mux and Level Shift



RMCK Output Header

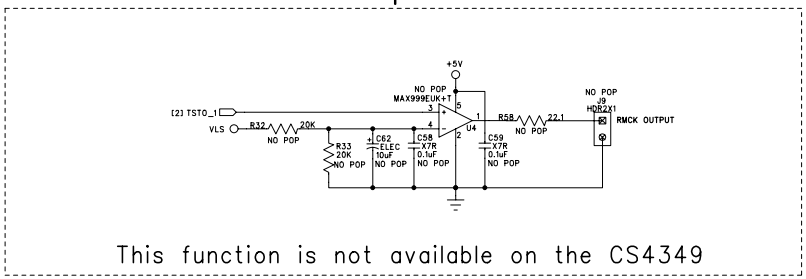
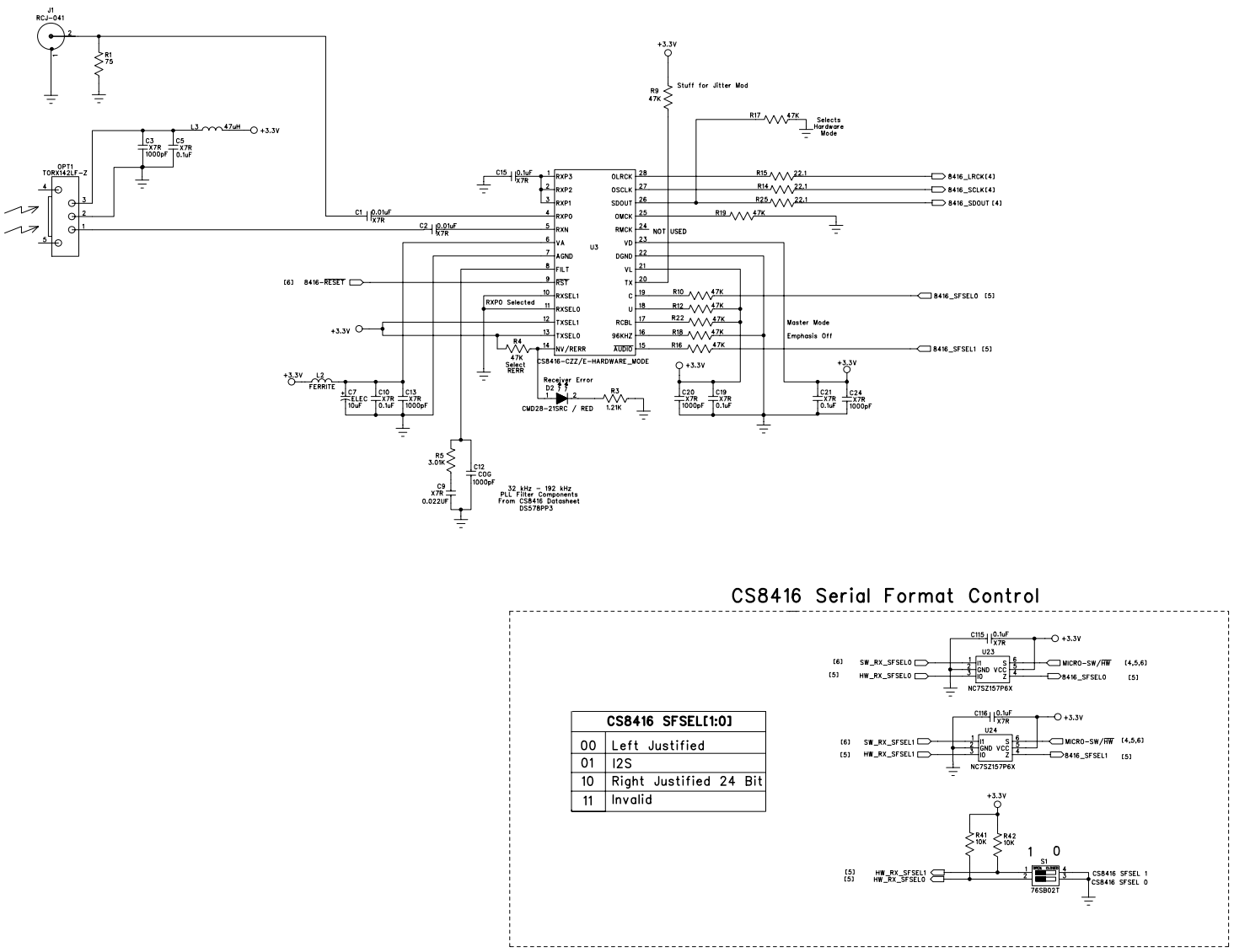


Figure 37. PCM Input Header and Hardware Control



CS8416 Serial Format Control

CS8416 SFSEL[1:0]	
00	Left Justified
01	I2S
10	Right Justified 24 Bit
11	Invalid

Figure 38. CS8416 S/PDIF Input

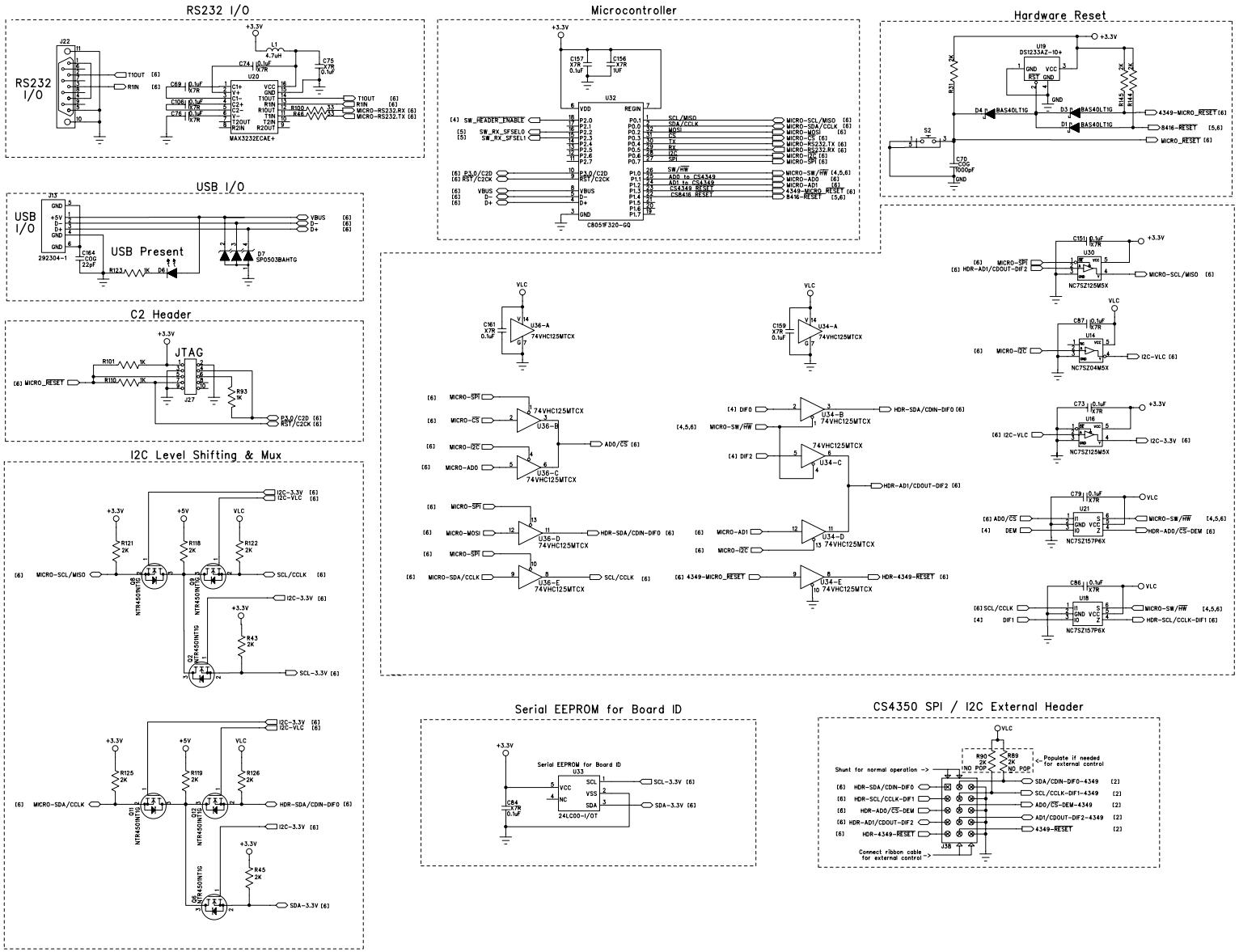
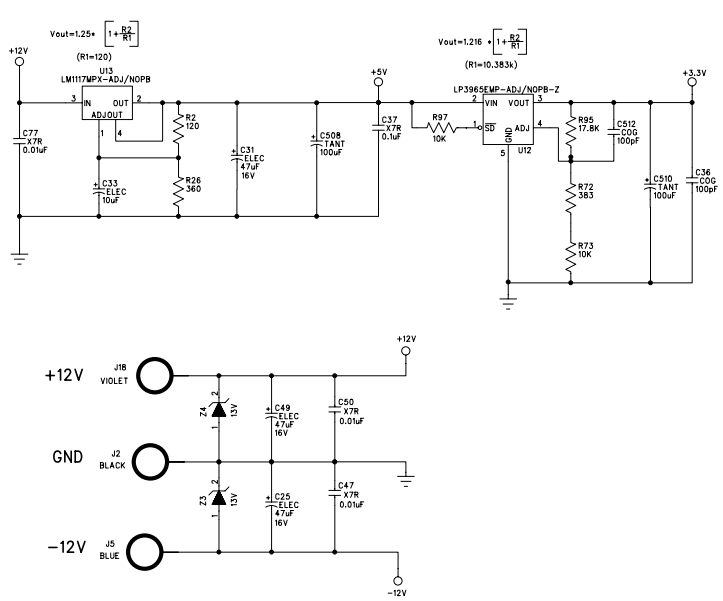
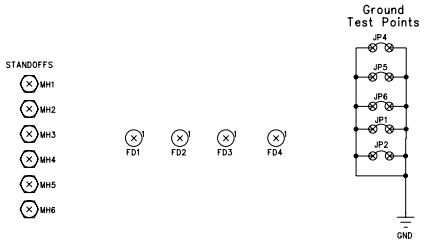
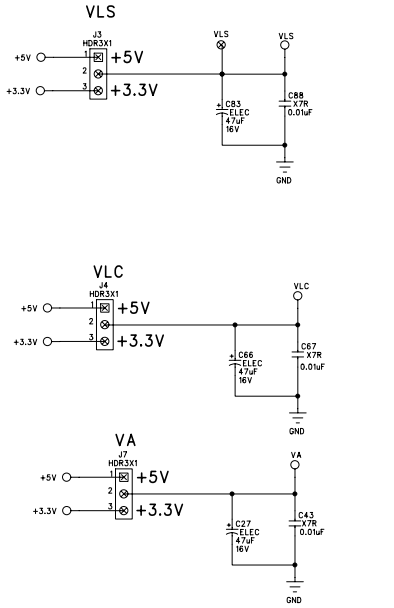


Figure 39. Control Port







Remove Shunt For External Voltage Supply Connection

Figure 40. Power

12.LAYOUT

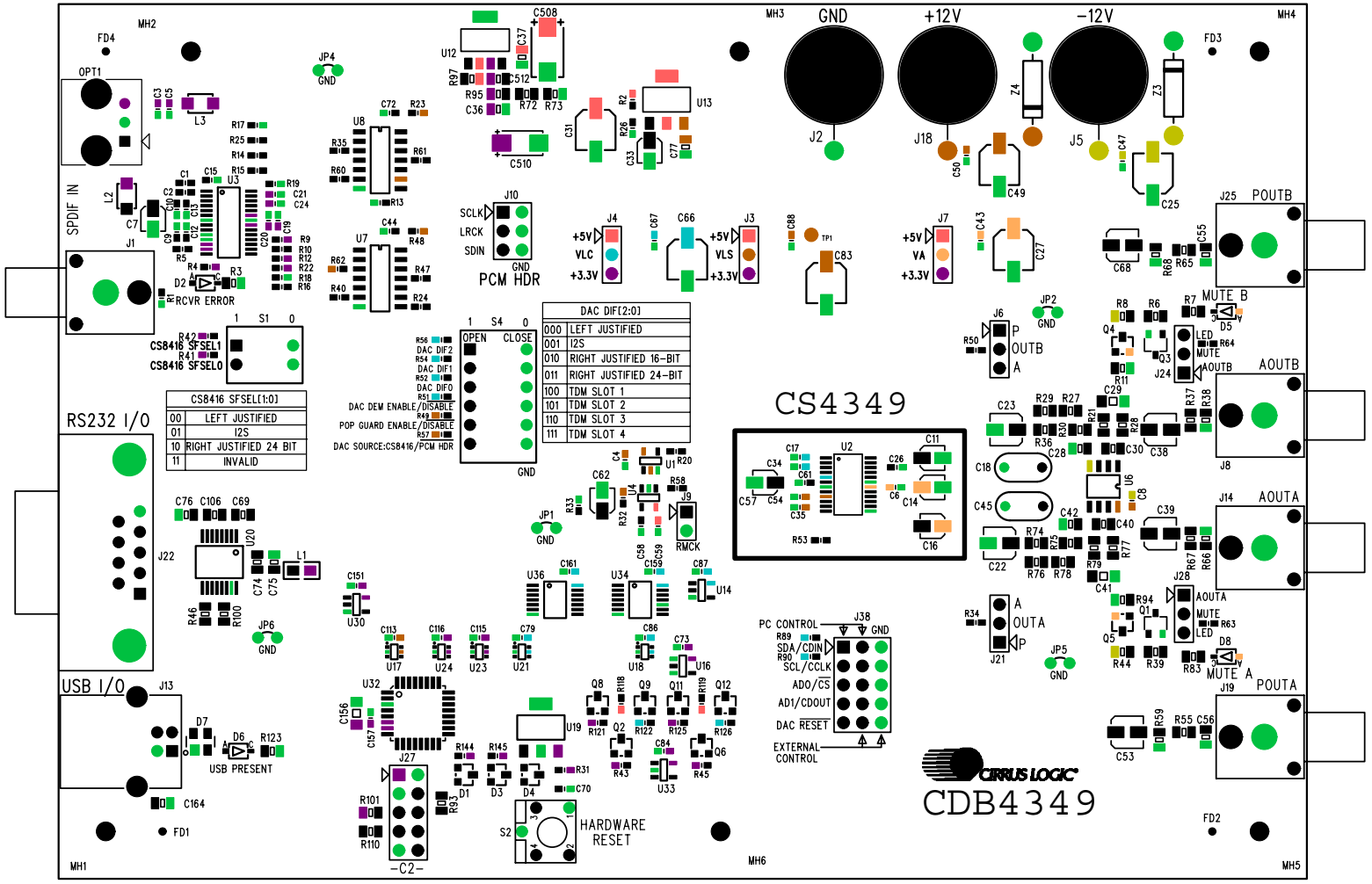


Figure 41. Silkscreen Top

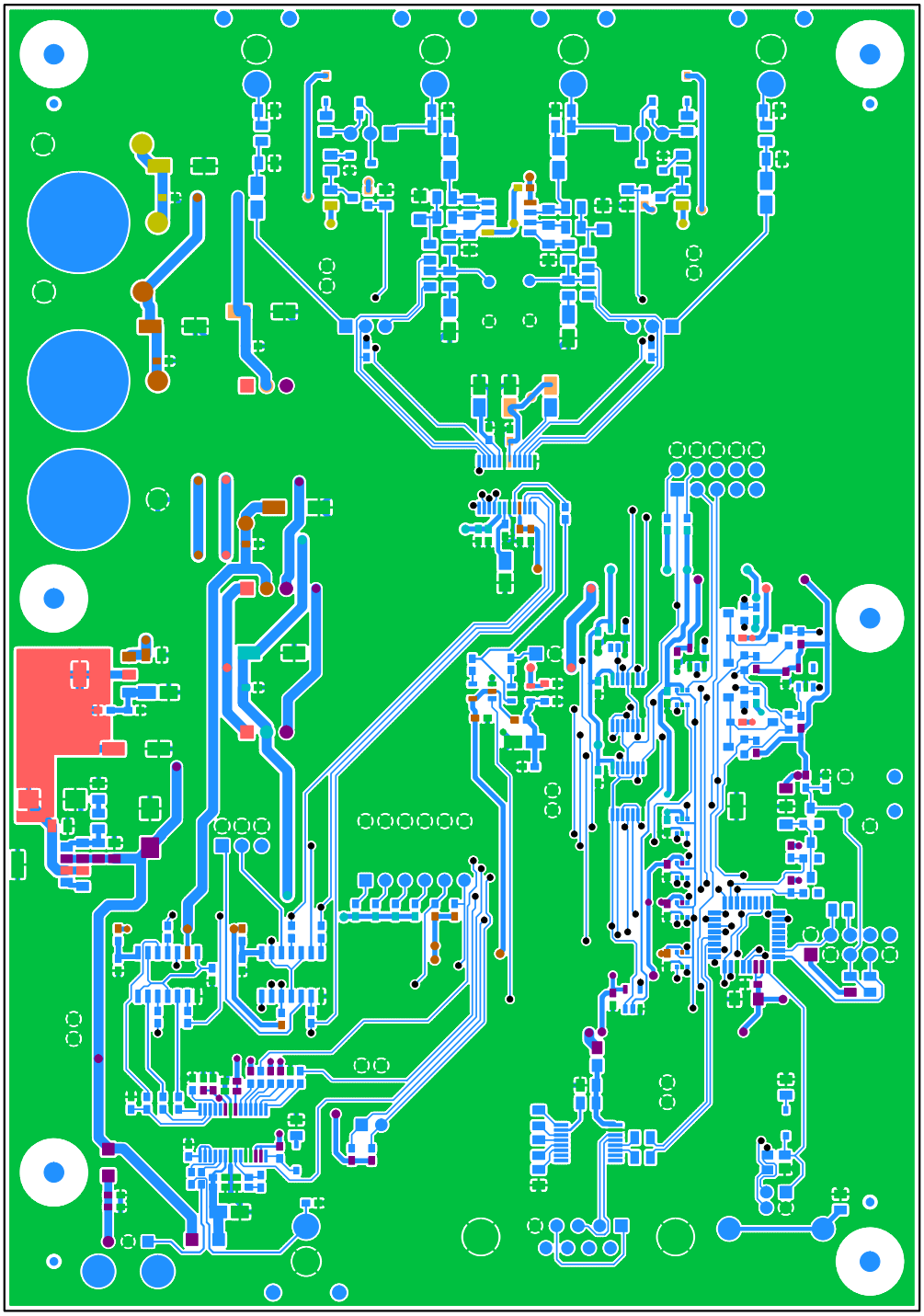


Figure 42. Top Side

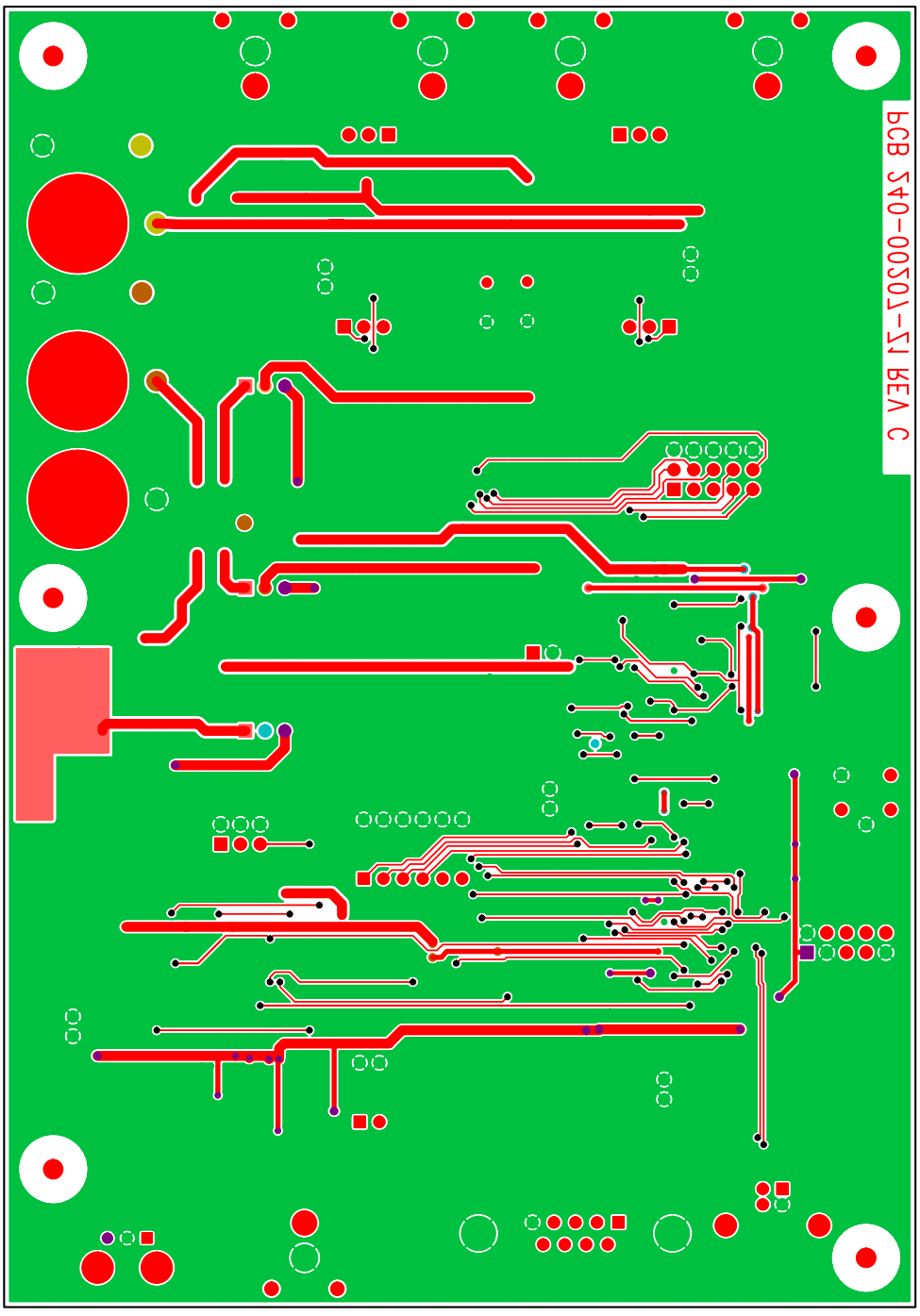


Figure 43. Bottom Side

13.REVISION HISTORY

Release	Date	Changes
DB1	June 2007	Initial Evaluation Board Datasheet Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to **www.cirrus.com**