



PSMN1R5-30BLE

N-channel 30 V 1.5 mΩ logic level MOSFET in D2PAK

12 October 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Enhanced forward biased safe operating area for superior linear mode operation
- Very low R_{DSon} for low conduction losses

1.3 Applications

- Electronic fuse
- Hot swap
- Load switch
- Soft start

1.4 Quick reference data

Table 1. Quick reference data

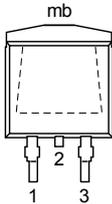
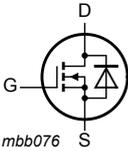
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---|-----|-----|------|------|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | | - | - | 30 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1 | [1] | - | - | 120 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 2 | | - | - | 401 | W |
| Static characteristics | | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | | - | 1.3 | 1.5 | mΩ |
| | | $V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | | - | 1.7 | 1.85 | mΩ |
| Dynamic characteristics | | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 14 ; Fig. 15 | | - | 33.2 | - | nC |
| $Q_{G(tot)}$ | total gate charge | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 14 ; Fig. 15 | | - | 228 | - | nC |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--|--|-----|-----|------|------|
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 120\text{ A}$; $V_{sup} \leq 30\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$; Fig. 3 | - | - | 1990 | mJ |

[1] Capped at 120A due to package

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|--|
| 1 | G | gate |  <p>D2PAK (SOT404)</p> |  <p><i>mbb076</i></p> |
| 2 | D | drain[1] | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|---------------|---------|--|---------|
| | Name | Description | |
| PSMN1R5-30BLE | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|---------------|
| PSMN1R5-30BLE | PSMN1R5-30BLE |

5. Limiting values

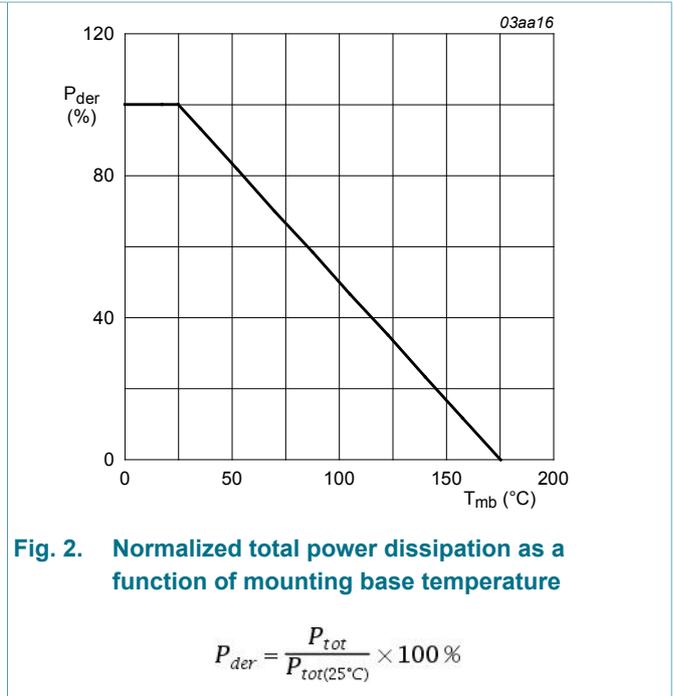
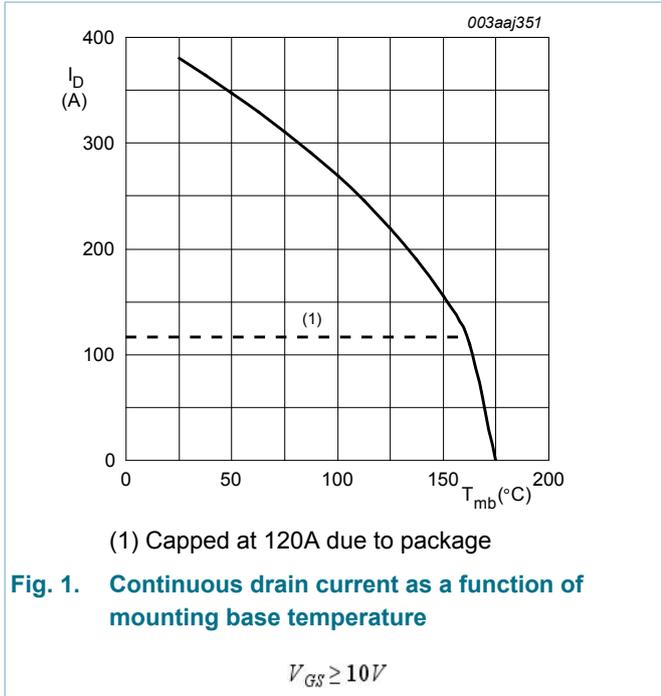
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------|---|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$ | - | 30 | V |
| V_{DGR} | drain-gate voltage | $T_j \leq 175\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$ | - | 30 | V |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|------|
| V _{GS} | gate-source voltage | | | -20 | 20 | V |
| I _D | drain current | V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 1 | [1] | - | 120 | A |
| | | V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 1 | [1] | - | 120 | A |
| I _{DM} | peak drain current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 4 | | - | 1521 | A |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; Fig. 2 | | - | 401 | W |
| T _{stg} | storage temperature | | | -55 | 175 | °C |
| T _j | junction temperature | | | -55 | 175 | °C |
| T _{sld(M)} | peak soldering temperature | | | - | 260 | °C |
| Source-drain diode | | | | | | |
| I _S | source current | T _{mb} = 25 °C | [1] | - | 120 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | | - | 1521 | A |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 120 A; V _{sup} ≤ 30 V; unclamped; R _{GS} = 50 Ω; Fig. 3 | | - | 1990 | mJ |

[1] Capped at 120A due to package



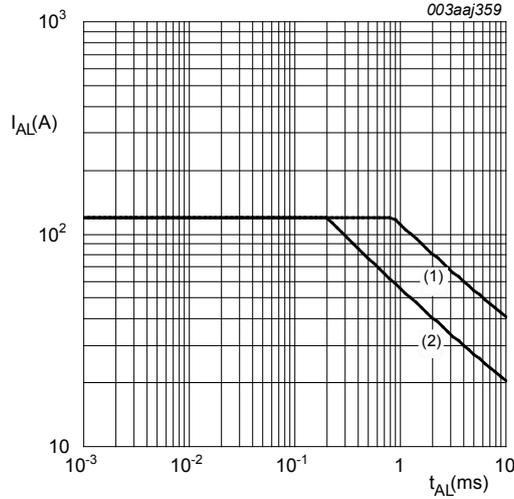


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (int)} = 25^{\circ}C$; (2) $T_{j (int)} = 100^{\circ}C$

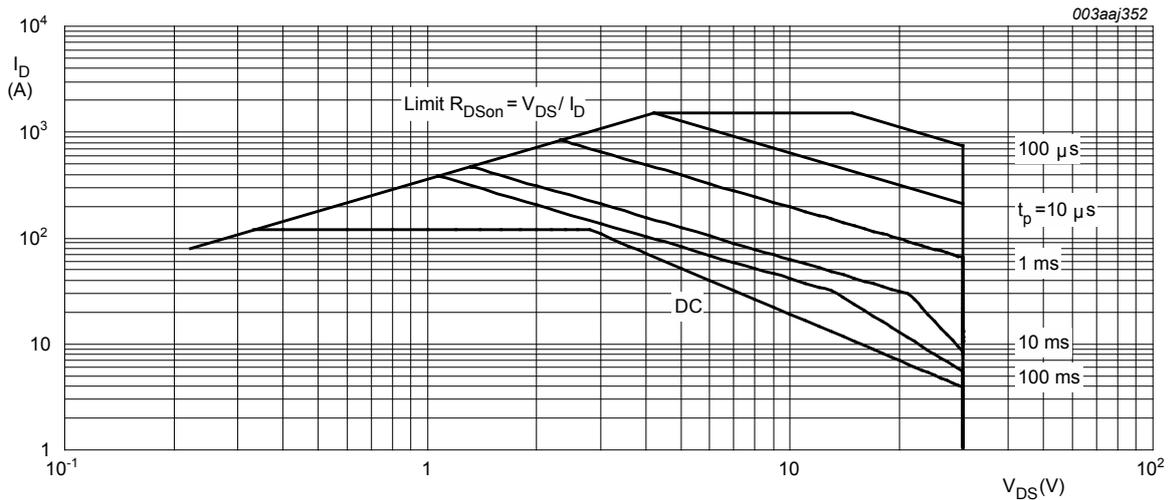


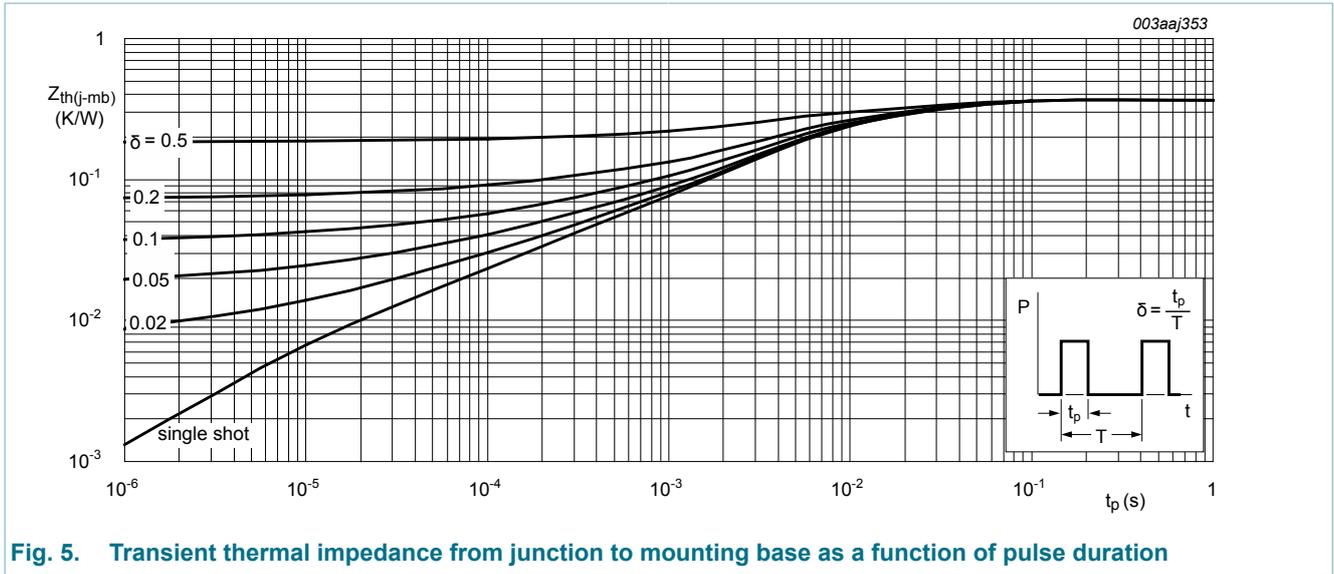
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | 0.3 | 0.37 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; FR4 board | - | 50 | - | K/W |



7. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|--|-----|-----|------|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 27 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 30 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10 | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 11; Fig. 10 | 1.3 | 1.7 | 2.15 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10 | - | - | 2.45 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.5 | 10 | μA |
| | | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 100 \text{ }^\circ C$ | - | - | 200 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| | | $V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12 | - | 1.3 | 1.5 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C;$ Fig. 12; Fig. 13 | - | - | 2.1 | mΩ |
| | | $V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12 | - | 1.7 | 1.85 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 13 | - | - | 2.9 | mΩ |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|-------|-----|------|
| R _G | internal gate resistance (AC) | f = 1 MHz | 0.5 | 1.1 | 2.2 | Ω |
| Dynamic characteristics | | | | | | |
| Q _{G(tot)} | total gate charge | I _D = 25 A; V _{DS} = 15 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15 | - | 228 | - | nC |
| | | I _D = 25 A; V _{DS} = 15 V; V _{GS} = 4.5 V; Fig. 14 ; Fig. 15 | - | 108 | - | nC |
| | | I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V | - | 210 | - | nC |
| Q _{GS} | gate-source charge | I _D = 25 A; V _{DS} = 15 V; V _{GS} = 4.5 V; Fig. 14 ; Fig. 15 | - | 31.8 | - | nC |
| Q _{GS(th)} | pre-threshold gate-source charge | | - | 21.5 | - | nC |
| Q _{GS(th-pl)} | post-threshold gate-source charge | | - | 10.3 | - | nC |
| Q _{GD} | gate-drain charge | | - | 33.2 | - | nC |
| V _{GS(pl)} | gate-source plateau voltage | I _D = 25 A; V _{DS} = 15 V; Fig. 14 ; Fig. 15 | - | 2.5 | - | V |
| C _{iss} | input capacitance | V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz; | - | 14934 | - | pF |
| C _{oss} | output capacitance | T _j = 25 °C; Fig. 16 | - | 2741 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 1168 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 15 V; R _L = 0.6 Ω; V _{GS} = 4.5 V; | - | 100.6 | - | ns |
| t _r | rise time | R _{G(ext)} = 4.7 Ω; T _j = 25 °C | - | 156.1 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 191.8 | - | ns |
| t _f | fall time | | - | 99.2 | - | ns |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain voltage | I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17 | - | 0.78 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 25 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; | - | 62.5 | - | ns |
| Q _r | recovered charge | V _{DS} = 15 V | - | 96.8 | - | nC |

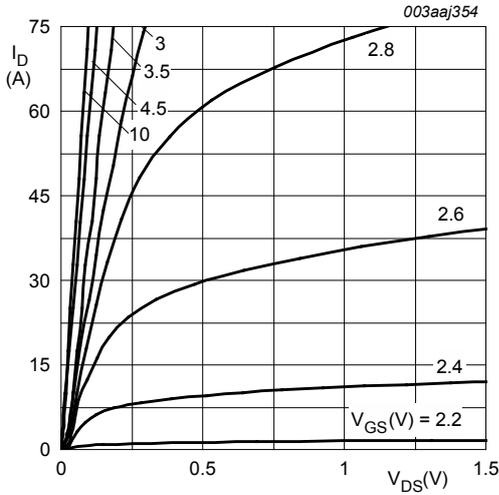


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ C$

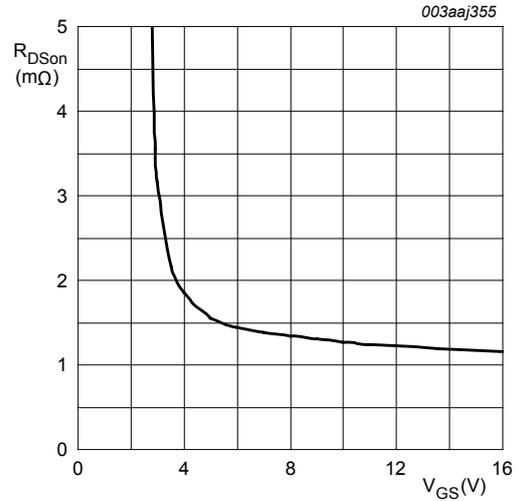


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ C; I_D = 25 A$

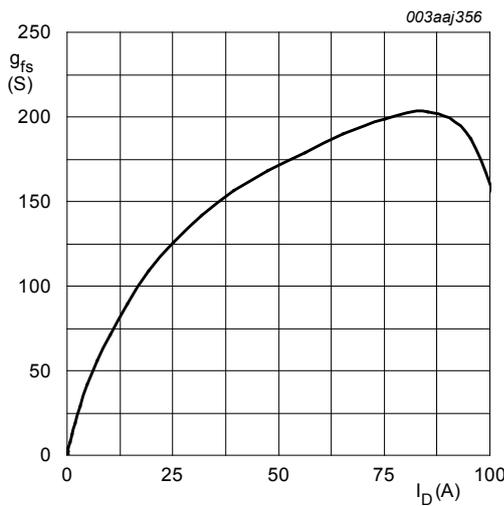


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^\circ C; V_{DS} = 10 V$

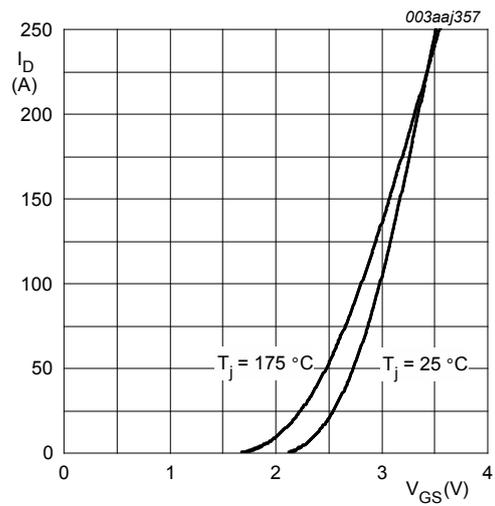


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10 V$

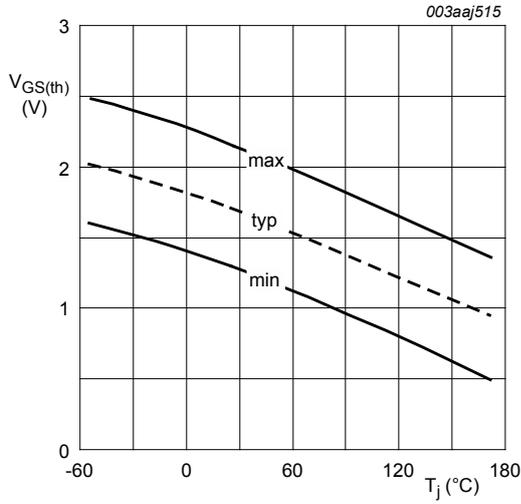


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$V_{DS} = V_{GS}$$

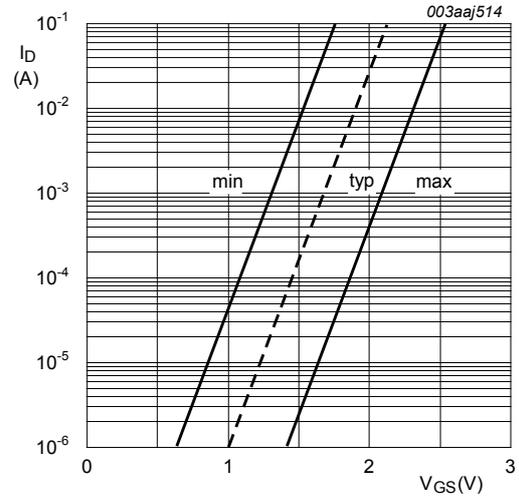


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

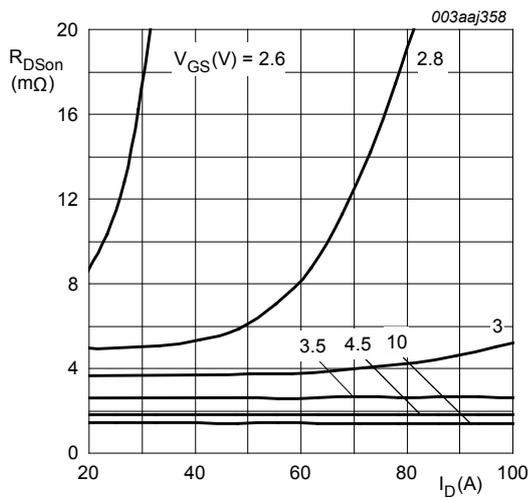


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

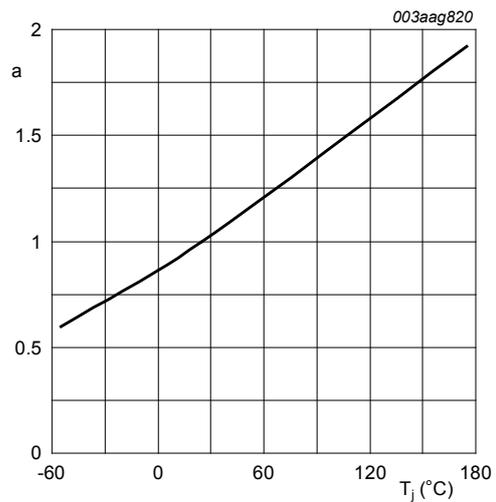


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

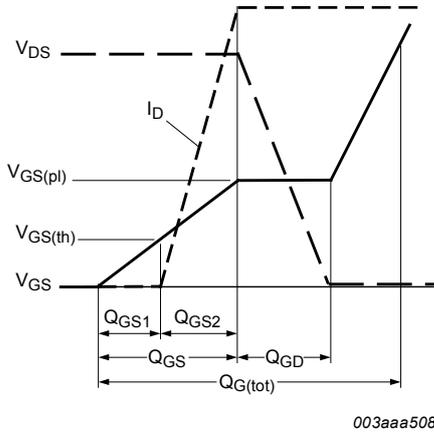


Fig. 14. Gate charge waveform definitions

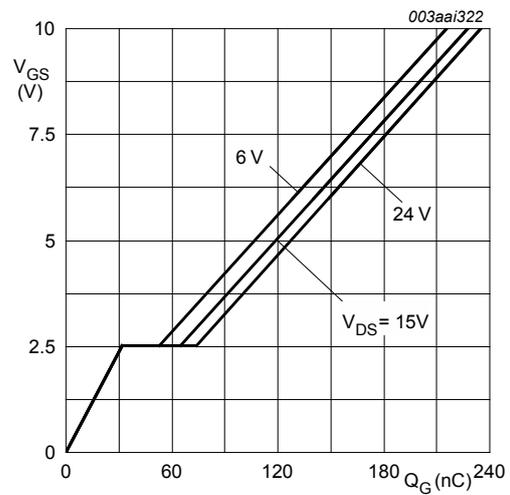


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

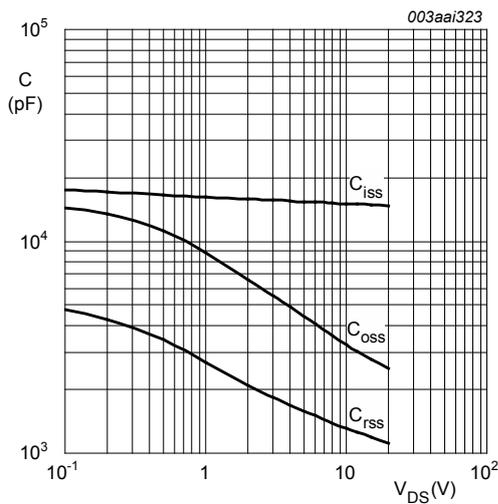


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

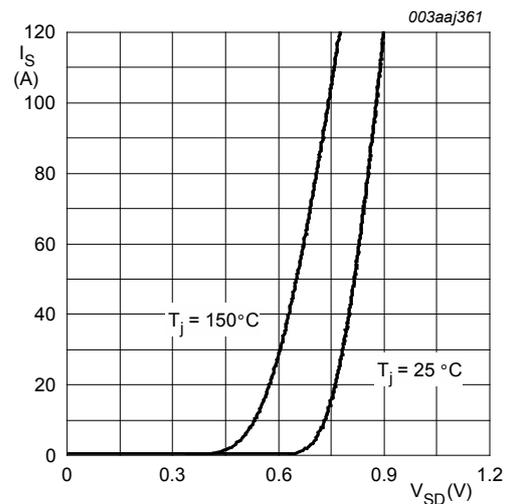


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

8. Package outline

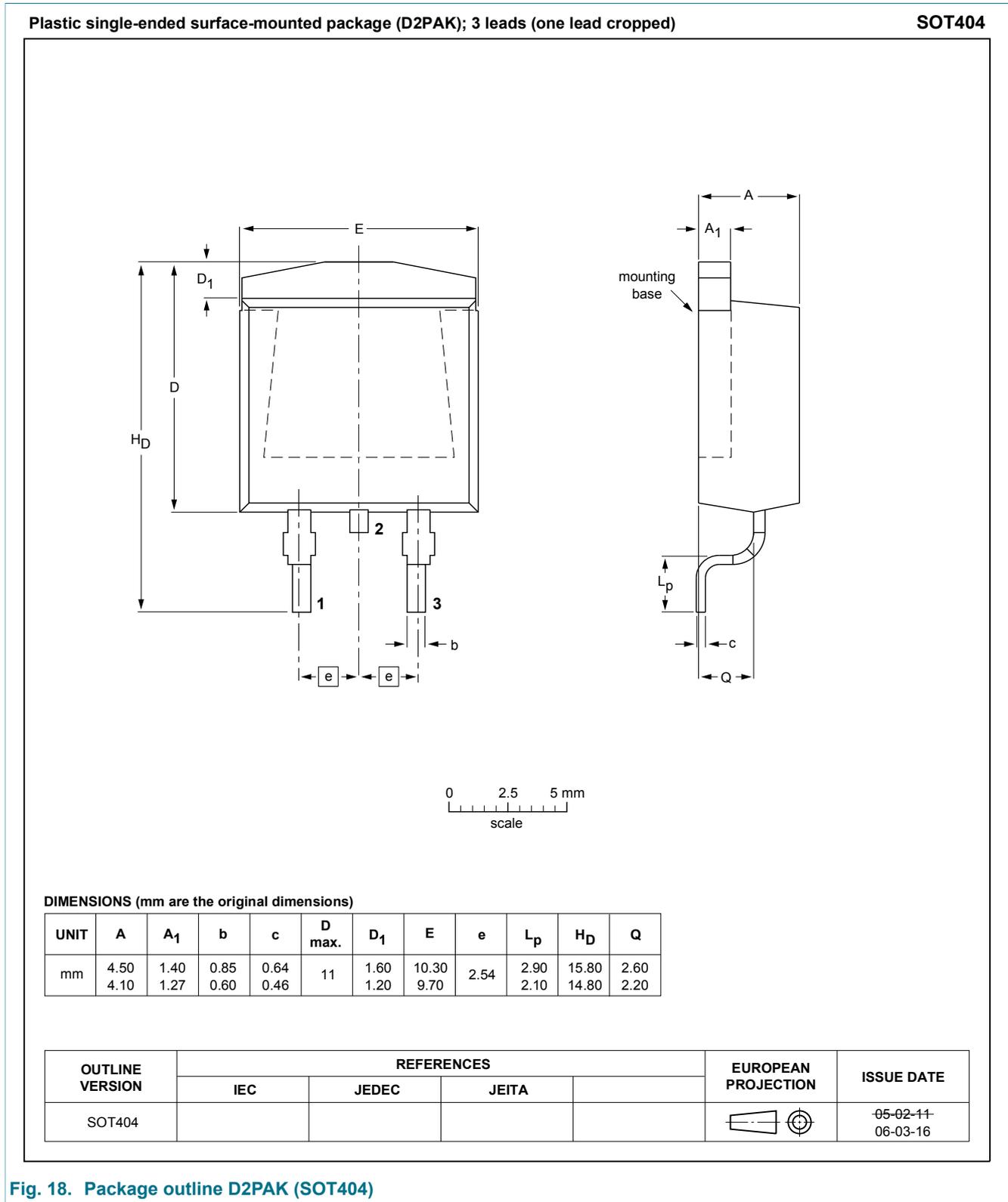


Fig. 18. Package outline D2PAK (SOT404)

9. Legal information

9.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

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