

## CY7C1046D

# 4-Mbit (1 M × 4) Static RAM

#### **Features**

- Pin- and function-compatible with CY7C1046B
- High speed
- ⊐ t<sub>AA</sub> = 10 ns
- CMOS for optimum speed and power
- Low active power □ I<sub>CC</sub> = 90 mA at 10 ns
- Low CMOS standby power □ I<sub>SB2</sub> = 10 mA
- Data retention at 2.0 V
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in lead-free 400-mil-wide 32-pin SOJ package

#### **Functional Description**

The CY7C1046D is a high-performance CMOS static RAM organized as 1M words by 4 bits. Easy memory expansion is

provided by an <u>active LOW</u> Chip Enable ( $\overline{CE}$ ), an active LOW Output Enable ( $\overline{OE}$ ), and tri-state drivers. <u>Writing to the device is</u> accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. Data on the four I/O pins (I/O<sub>0</sub> through I/O<sub>3</sub>) is then written into the location specified on the address pins (A<sub>0</sub> through A<sub>19</sub>).

<u>Rea</u>ding from the device is <u>ac</u>complished by taking Chip Enable  $(\overline{CE})$  and Output Enable  $(\overline{OE})$  LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins ( $I/O_0$  through  $I/O_3$ ) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1046D is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

The CY7C1046D device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

#### Logic Block Diagram



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### **Selection Guide**

Description	–10	Unit
Maximum Access Time	10	ns
Maximum Operating Current	90	mA
Maximum CMOS Standby Current (mA)	10	mA

#### **Pin Configuration**

	10 2 3 4 5 6 7 8 9	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
	-	
	6	
	7	
V <sub>CC</sub>	8	25 🗌 GND
GND [	9	24 🗌 V <sub>CC</sub>
I/O <sub>1</sub> [	10	23 🗌 I/Õ <sub>2</sub>
WE	11	22 🗋 A <sub>14</sub>
$A_5 \Box$	12	21 🗋 A <sub>13</sub>
A <sub>6</sub>	13	20 🗌 A <sub>12</sub>
$A_7 \square$	14	19 🛛 A <sub>11</sub>
A <sub>8</sub>	15	18 🛛 A <sub>10</sub>
A <sub>9</sub> ⊑	16	17 🗆 NC

Figure 1. 32-pin SOJ pinout (Top View)



#### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature65 °C to +150 °C
Ambient temperature with power applied55 °C to +125 °C
Supply voltage on $V_{CC}$ to relative GND $^{[1]}$ 0.5 V to +6.0 V
DC voltage applied to outputs in high Z state $^{[1]}$ 0.5 V to V_{CC} + 0.5 V

DC input voltage <sup>[1]</sup>	–0.5 V to $V_{CC}$ + 0.5 V
Current into outputs (LOW)	20 mA
Static discharge voltage (per MIL-STD-883, method 3015)	> 2001 V
Latch up current	> 200 mA

### **Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	–40 °C to +85 °C	4.5 V–5.5 V

#### **Electrical Characteristics**

Over the Operating Range

Deveryoter	arameter Description Test Conditions			-	10	l lmit
Parameter	Description			Min	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	$V_{CC}$ = Min, $I_{OH}$ = -4.0 mA		2.4	-	V
		$V_{CC} = Max$ , $I_{OH} = -0.1 \text{ mA}$		_	3.4 <sup>[2]</sup>	
V <sub>OL</sub>	Output LOW voltage	$V_{CC}$ = Min, $I_{OL}$ = 8.0 mA		_	0.4	V
V <sub>IH</sub>	Input HIGH voltage			2.0	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW voltage [1]			-0.5	0.8	V
I <sub>IX</sub>	Input leakage current	$GND \le V_{IN} \le V_{CC}$		-1	+1	μA
I <sub>OZ</sub>	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , output disable	d	-1	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$V_{CC} = Max, f = f_{MAX} = 1/t_{RC}$	100 MHz	_	90	mA
			83 MHz	_	80	
			66 MHz	_	70	
			40 MHz	_	60	
I <sub>SB1</sub>	Automatic CE Power-Down Current – TTL inputs	$\begin{array}{l} \text{Max } V_{CC}, \ \overline{CE} \geq V_{IH}, V_{IN} \geq V_{IH} \text{ or} \\ V_{IN} \leq V_{IL}, \ f = f_{MAX} \end{array}$		-	20	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current – CMOS inputs	$\begin{array}{l} \mbox{Max V}_{CC}, \ \overline{CE} \geq V_{CC} - 0.3 \ \mbox{V}, \\ \mbox{V}_{IN} \geq V_{CC} - 0.3 \ \mbox{V}, \ \mbox{or V}_{IN} \leq 0.3 \ \mbox{V}, \ \mbox{f} \end{array}$	= 0	-	10	mA

Notes

V<sub>IL</sub> (min) = -2.0 V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 2 V for pulse durations of less than 20 ns.
Please note that the maximum V<sub>OH</sub> limit does not exceed minimum CMOS V<sub>IH</sub> of 3.5V. If you are interfacing this SRAM with 5V legacy processors that require a minimum V<sub>IH</sub> of 3.5V, please refer to Application Note AN6081 for technical details and options you may consider.



#### Capacitance

Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 \text{ °C}, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	8	pF
C <sub>OUT</sub>	I/O capacitance		8	pF

#### **Thermal Resistance**

Parameter <sup>[3]</sup>	Description	Test Conditions	SOJ Package	Unit
JA	Thermal resistance (junction to ambient)	Still Air, soldered on a $3 \times 4.5$ inch, four-layer printed circuit board	53.44	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		38.25	°C/W

#### **AC Test Loads and Waveforms**



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except high Z) are tested using the load conditions shown in (a). High Z characteristics are tested for all speeds using the test load shown in (c).



#### **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions <sup>[5]</sup>	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		2.0	_	V
I <sub>CCDR</sub>	Data retention current	$V_{CC} = V_{DR} = 2.0 \text{ V}, \overline{CE} \ge V_{CC} - 0.3 \text{ V},$	_	10	mA
t <sub>CDR</sub> <sup>[6]</sup>	Chip deselect to data retention time	$V_{\text{IN}} \ge V_{\text{CC}} - 0.3 \text{ V or } V_{\text{IN}} \le 0.3 \text{ V}$	0	_	ns
t <sub>R</sub> <sup>[7]</sup>	Operation recovery time		t <sub>RC</sub>	I	ns

#### **Data Retention Waveform**





Notes

- 5. No inputs may exceed V<sub>CC</sub> + 0.3 V. 6. Tested initially and after any design or process changes that may affect these parameters. 7. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub>  $\geq$  50 µs or stable at V<sub>CC(min)</sub>  $\geq$  50 µs.



#### **Switching Characteristics**

Over the Operating Range

Parameter [8]	Description	7C104	6D-10	Unit	
Parameter <sup>101</sup>	Description	Min	Max	Unit	
Read Cycle			•		
t <sub>power</sub>	V <sub>CC</sub> (typical) to the first access <sup>[9]</sup>	100	-	μS	
t <sub>RC</sub>	Read cycle time	10	-	ns	
t <sub>AA</sub>	Address to data valid	-	10	ns	
t <sub>OHA</sub>	Data hold from address change	3	-	ns	
t <sub>ACE</sub>	CE LOW to data valid	-	10	ns	
t <sub>DOE</sub>	OE LOW to data valid	-	5	ns	
t <sub>LZOE</sub>	OE LOW to low Z <sup>[11]</sup>	0	-	ns	
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[10, 11]</sup>	-	5	ns	
t <sub>LZCE</sub>	CE LOW to low Z <sup>[11]</sup>	3	-	ns	
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[10, 11]</sup>	-	5	ns	
t <sub>PU</sub>	CE LOW to power-up	0	-	ns	
t <sub>PD</sub>	CE HIGH to power-down	-	10	ns	
Write Cycle <sup>[12,</sup>	13]	·			
t <sub>WC</sub>	Write cycle time	10	-	ns	
t <sub>SCE</sub>	CE LOW to write end	7	-	ns	
t <sub>AW</sub>	Address set-up to write end	7	-	ns	
t <sub>HA</sub>	Address hold from write end	0	-	ns	
t <sub>SA</sub>	Address set-up to write start	0	-	ns	
t <sub>PWE</sub>	WE pulse width	7	-	ns	
t <sub>SD</sub>	Data set-up to write end	6	-	ns	
t <sub>HD</sub>	Data hold from write end	0	-	ns	
t <sub>LZWE</sub>	WE HIGH to low Z <sup>[11]</sup>	3	-	ns	
t <sub>HZWE</sub>	WE LOW to high Z <sup>[10, 11]</sup>	-	5	ns	

Notes

Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
t<sub>POWER</sub> gives the minimum amount of time that the power supply should be at stable, typical V<sub>CC</sub> values until the first memory access can be performed.
t<sub>HZCE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured when the outputs enter a high impedance state.

At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



#### **Switching Waveforms**



Notes

<sup>14.</sup> Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ . 15. WE is HIGH for read cycle.

<sup>16.</sup> Address valid prior to or coincident with  $\overline{CE}$  transition LOW.



#### Switching Waveforms (continued)



Figure 7. Write Cycle No. 2 (WE Controlled, OE HIGH During Write) <sup>[17, 18]</sup>



**Notes** 17. Data I/O is high impedance if  $\overline{OE} = V_{|H}$ . 18. If  $\overline{CE}$  goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state. 19. During this period the I/Os are in the output state and input signals should not be applied.



#### Switching Waveforms (continued)



Figure 8. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW) [20]

Notes \_\_\_\_\_\_\_ 20. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state. 21. During this period the I/Os are in the output state and input signals should not be applied.



# **Truth Table**

CE	OE	WE	I/O <sub>0</sub> –I/O <sub>3</sub>	Mode	Power
Н	Х	Х	High Z	Power-down	Standby (I <sub>SB</sub> )
L	L	Н	Data Out	Read	Active (I <sub>CC</sub> )
L	Х	L	Data In	Write	Active (I <sub>CC</sub> )
L	Н	Н	High Z	Selected, outputs disabled	Active (I <sub>CC</sub> )



#### **Ordering Information**

_	peed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
	10	CY7C1046D-10VXI	51-85033	32-pin (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact your local Cypress sales representative for availability of these parts.

#### **Ordering Code Definitions**





#### **Package Diagrams**

Figure 9. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033

32 Lead (400 MIL) Molded SOJ V33



51-85033 \*E



#### Acronyms

Acronym	Description		
CMOS	Complementary Metal Oxide Semiconductor		
CE	Chip Enable		
I/O	Input/Output		
OE	Output Enable		
SOJ	Small-Outline J-leaded		
SRAM	Static Random Access Memory		
TTL	Transistor-Transistor Logic		
WE	Write Enable		

#### **Document Conventions**

#### Units of Measure

Symbol	Unit of Measure	
°C	degree Celsius	
MHz	megahertz	
μs	microsecond	
μA	microampere	
mA	milliampere	
ns	nanosecond	
%	percent	
pF	picofarad	
V	volt	
W	watt	





# **Document History Page**

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	307613	See ECN	RKF	New data sheet.
*A	399070	See ECN	NXR	Changed from Advance to Preliminary Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -20 speed bin Removed L-Version Redefined I <sub>CC</sub> values for Com'l and Ind'l temperature ranges I <sub>CC</sub> (Com'l): Changed from 70 and 55 mA to 75 and 70 mA for 12 and 15 ns speed bins respectively I <sub>CC</sub> (Ind'l): Changed from 80, 70 and 55 mA to 90, 85 and 80 mA for 10, 12 and 15 ns speed bins respectively Added Industrial Operating Range Changed reference voltage level for measurement of Hi-Z parameters from $\pm$ 500 mV to $\pm$ 200 mV Changed V <sub>CC</sub> to 3 V in the Input pulse waveform at the AC Test Loads and Waveforms on page # 3 Changed t <sub>SCE</sub> from 8 to 7 ns for -10 speed bin Added 10 ns parts in the Ordering Information table Changed part names from V33 to V324 in the Ordering Information Table Shaded Ordering Information Table
*B	459072	See ECN	NXR	Converted from Preliminary to Final. Removed -12 and -15 Speed bins Removed Commercial Operating Range product information. Changed Maximum Rating for supply voltage from 7V to 6V Changed the Capacitance value of input pins and I/O pins from 6 pF to 8 pF Updated the Thermal Resistance table. Changed t <sub>HZWE</sub> from 6 ns to 5 ns Added footnote #4 and 11 Updated footnote #7 on High-Z parameter measurement Updated the Ordering Information and replaced Package Name column with Package Diagram in the Ordering Information table.
*C	3059162	10/14/2010	PRAS	Added Ordering Code Definitions. Updated Package Diagrams.
*D	3098812	12/01/2010	PRAS	Added Acronyms and Units of Measure. Minor edits and updated in new template.
*Е	3446913	11/24/2011	TAVA	Removed Note referring to SRAM System Guidelines application note on page 1. Updated test conditions for IIX parameter.
*F	4039540	06/25/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition " $V_{CC} = Max$ , $I_{OH} = -0.1$ mA" for $V_{OH}$ parameter and added maximum value corresponding to that Test Condition. Added Note 2 and referred the same note in maximum value for $V_{OH}$ parameter corresponding to Test Condition " $V_{CC} = Max$ , $I_{OH} = -0.1$ mA".
*G	4574311	11/20/2014	MEMJ	Added related documentation hyperlink in page 1. Updated Figure 9 in Package Diagrams (spec 51-85033 *D to *E).



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