



Click here for the 3D model.

Dimensions	
D	10.16mm +/-0.635mm
L	6.35mm MIN
Н	2.54mm NOM
F	1.397mm +/-0.25mm
А	5.3mm MAX
В	7.078mm MAX
С	10.16mm +/-0.635mm
E	11.18mm MAX
К	0.5mm NOM

Packaging Specifications		
Packaging	Waffle, Box	
Packaging Quantity	50	

General Information		
Series	KPS-MCC Indust COG HT200C	
Style	Leaded Stacked Chip	
Description	Low ESR, Stacked Ceramic Chips	
Features	200C, Low ESR, High Thermal Stability, Bulk Capacitance	
RoHS	No	
Prop 65	A WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov.	
SCIP Number	89f79324-98a2-425d-914d-1725e977d89a	
Termination	60/40 Solder Coated	
Lead	Straight Leads	
AEC-Q200	No	
Notes	Number of chips in this stack: 2.	

Specifications				
Capacitance	0.12 uF			
Capacitance Tolerance	5%			
Voltage DC	1000 VDC			
Dielectric Withstanding Voltage	1200 VDC			
Temperature Range	-55/+200°C			
Temperature Coefficient	COG			
Dissipation Factor	0.1% 1 kHz 25C			
Aging Rate	0% Loss/Decade Hour			
Insulation Resistance	8.33 GOhms			

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