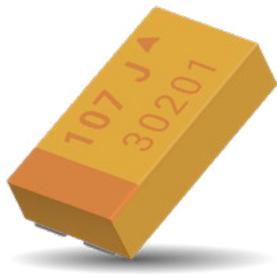


# TLN Series

## Tantalum Solid Electrolytic Chip Capacitors - Undertab Series



### FEATURES

- Undertab Terminations Layout:
  - High Volumetric Efficiency
  - High PCB Assembly Density
  - High Capacitance in Smaller Dimensions
- 3x Reflow 260°C Compatible
- 100% Surge Current Tested
- Consumer Applications (e.g. PCMCIA/USB Wireless Express Cards, Mobiles, MP3 etc.)
- 3 Case Sizes Available
- CV Range: 47-220µF / 4-10V



### APPLICATIONS

- Mobile Phones
- Tablets
- MP3/4 Players

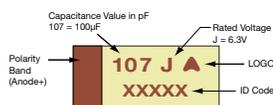
### CASE DIMENSIONS:

millimeters (inches)

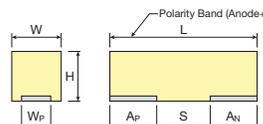
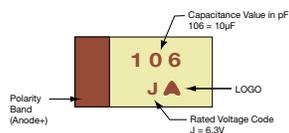
Code	EIA Code	EIA Metric	L±0.20 (0.008)	W+0.20 (0.008) -0.10 (0.004)	H max.	Wp±0.10 (0.004)	Wn±0.10 (0.004)	Ap±0.10 (0.004)	An±0.10 (0.004)	S Min.
M	0805	2012-09	2.05 (0.081)	1.30 (0.051)	0.90 (0.035)	1.00 (0.039)	1.00 (0.039)	0.85 (0.033)	0.85 (0.033)	0.40 (0.016)
N	0805	2012-10	2.05 (0.081)	1.30 (0.051)	1.00 (0.039)	1.00 (0.039)	1.00 (0.039)	0.85 (0.033)	0.85 (0.033)	0.40 (0.016)
T	1210	3528-12	3.50 (0.138)	2.80 (0.110)	1.20 (0.047)	2.50 (0.098)	2.10 (0.083)	1.15 (0.045)	1.35 (0.053)	1.00 (0.039)

### MARKING

#### T, CASE



#### M, N CASE



### HOW TO ORDER

**TLN**  
Type

**N**  
Case Size  
See table above

**107**  
Capacitance Code  
pF code: 1st two digits represent significant figures, 3rd digit represents multiplier (number of zeros to follow)

**M**  
Tolerance  
M = ±20%

**004**  
Rated DC Voltage  
004 = 4Vdc  
006 = 6.3Vdc  
010 = 10Vdc

**R**  
Packaging  
R = Pure Tin 7" Reel  
S = Pure Tin 13" Reel

**5200**  
ESR in mΩ

### TECHNICAL SPECIFICATIONS

Technical Data:	All technical data relate to an ambient temperature of +25°C				
Capacitance Range:	47 µF to 220 µF				
Capacitance Tolerance:	±20%				
Rated Voltage (V <sub>R</sub> )	-55°C ≤ +40°C:	4	6.3	10	
Category Voltage (V <sub>C</sub> )	at 85°C:	2	3.2	5	
Category Voltage (V <sub>C</sub> )	at 125°C:	0.8	1.3	2	
Temperature Range:	-55°C to +125°C with category voltage				
Reliability:	0.2% per 1000 hours at 85°C, 0.5xV <sub>R</sub> with 0.1Ω/V series impedance with 60% confidence level				

# TLN Series

## Tantalum Solid Electrolytic Chip Capacitors - Undertab Series

### CAPACITANCE AND RATED VOLTAGE RANGE (LETTER DENOTES CASE SIZE)

Capacitance		Rated Voltage DC to 40°C / 0.5DC to 85°C / 0.2DC to 125°C		
µF	Code	4V (G)	6.3V (J)	10V (A)
47	476			M(6000)/N(6000)
100	107	N(5200)		
150	157			T(1500)
220	227	T(1500)	T(1500)	T(1300)

Released ratings, (ESR ratings in mOhms in parentheses)

Note: Voltage ratings are minimum values. KYOCERA AVX reserves the right to supply higher voltage ratings in the same case size, to the same reliability standards.

### RATINGS & PART NUMBER REFERENCE

Part Number	Case Size	Capacitance (µF)	Rated Voltage (V)	Rated Temperature (°C)	Category Voltage (V)	Category Temperature (°C)	Maximum Surge Current (A)	DCL Max. (µA)	ESR Max. @ 100kHz (mΩ)	100kHz RMS Current (mA)			MSL
										25°C	85°C	125°C	
<b>4 Volt @ 40°C</b>													
TLNN107M004#5200	N	100	4	40	0.8	125	0.4	20	5200	88	79	35	3
TLNT227M004#1500	T	220	4	40	0.8	125	1.0	17.6	1500	216	194	86	3
<b>6.3 Volt @ 40°C</b>													
TLNT227M006#1500	T	220	6.3	40	1.3	125	1.6	26.4	1500	216	194	86	3
<b>10 Volt @ 40°C</b>													
TLNM476M010#6000	M	47	10	40	2	125	0.8	9.4	6000	82	73	33	3
TLNN476M010#6000	N	47	10	40	2	125	0.8	9.4	6000	82	73	33	3
TLNT157M010#1500	T	150	10	40	2	125	2.6	30	1500	216	194	86	3
TLNT227M010#1300	T	220	10	40	2	125	2.9	44	1300	232	209	93	3

Moisture Sensitivity Level (MSL) is defined according to J-STD-020.

All technical data relates to an ambient temperature of +25°C. Capacitance is measured at 120Hz, 0.5V RMS with a maximum DC bias of 2.2 volts.

DCL is measured at rated voltage after 5 minutes.

ESR allowed to move up to 1.25 times catalogue limit post mounting

DCL allowed to move up to 2.00 times catalogue limit post mounting

For typical weight and composition see page 259.

**NOTE: KYOCERA AVX reserves the right to supply higher voltage ratings or tighter tolerance part in the same case size, to the same reliability standards.**

# TLN Series

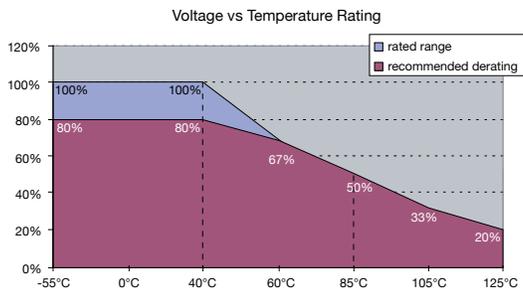
## Tantalum Solid Electrolytic Chip Capacitors - Undertab Series



### QUALIFICATION TABLE

TEST	TLN series (Temperature range -55°C to +125°C)									
	Condition			Characteristics						
Endurance	Apply rated voltage (Ur) at 40°C and / or category voltage (Uc) at 85°C for 2000 hours through a circuit impedance of $\leq 0.1\Omega/V$ . Stabilize at room temperature for 1-2 hours before measuring.			Visual examination	no visible damage					
				DCL	2 x initial limit					
				$\Delta C/C$	within +5/-30% of initial value					
				ESR	1.25 x initial limit					
Humidity	Store at 65°C and 90-95% relative humidity for 500 hours, with no applied voltage. Stabilize at room temperature and humidity for 1-2 hours before measuring.			Visual examination	no visible damage					
				DCL	2 x initial limit					
				$\Delta C/C$	within $\pm 10\%$ of initial value					
				ESR	1.25 x initial limit					
Temperature Stability	Step	Temperature°C	Duration(min)		+20°C	-55°C	+20°C	+85°C	+125°C	+20°C
	1	+20	15							
	2	-55	15	DCL	2 x IL*	n/a	2 x IL*	20 x IL*	25 x IL*	2 x IL*
	3	+20	15	$\Delta C/C$	n/a	+5/-20%	$\pm 10\%$	+20/-0%	+25/-0%	$\pm 10\%$
	4	+85	15	ESR	1.25xIL*	2.5 x IL*	1.25 x IL*	1.25 x IL*	1.25 x IL*	1.25xIL*
	5	+125	15							
6	+20	15								
Surge Voltage	Apply 1.3x rated voltage (Ur) at 40°C for 1000 cycles of duration 6 min (30 sec charge, 5 min 30 sec discharge) through a charge / discharge resistance of 1000 $\Omega$			Visual examination	no visible damage					
				DCL	2 x initial limit					
				$\Delta C/C$	within $\pm 5\%$ of initial value					
				ESR	1.25 x initial limit					
Mechanical Shock	MIL-STD-202, Method 213, Condition C			Visual examination	no visible damage					
				DCL	initial limit					
				$\Delta C/C$	within $\pm 5\%$ of initial value					
				DF	initial limit					
				ESR	initial limit					
Vibration	MIL-STD-202, Method 204, Condition D			Visual examination	no visible damage					
				DCL	initial limit					
				$\Delta C/C$	within $\pm 5\%$ of initial value					
				DF	initial limit					
				ESR	initial limit					

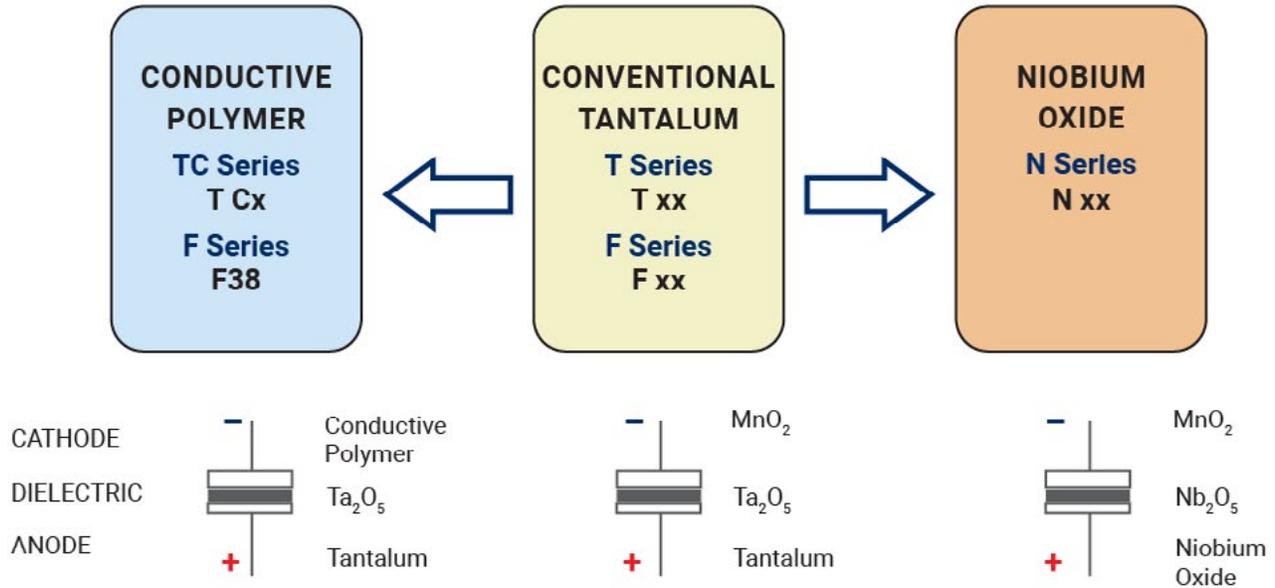
\*Initial Limit



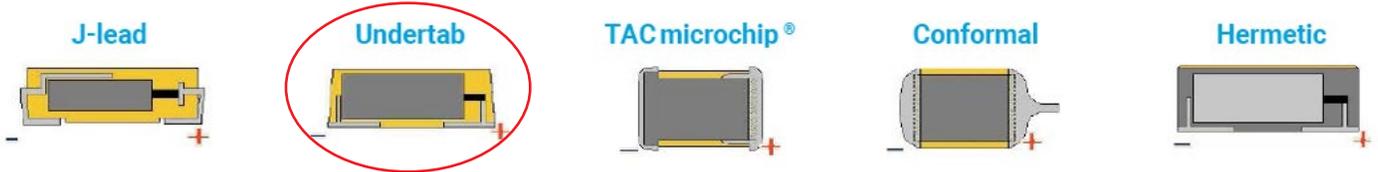
# TLN Series

## Tantalum Solid Electrolytic Chip Capacitors - Undertab Series

### SOLID ELECTROLYTIC CAPACITOR ROADMAP



### FIVE CAPACITOR CONSTRUCTION STYLES



### SERIES LINE UP : CONVENTIONAL SMD MnO<sub>2</sub>

