# **Power MOSFET**

# 23 A, 25 V, N-Channel DPAK

## **Features**

- Planar HD3e Process for Fast Switching Performance
- Low R<sub>DS(on)</sub> to Minimize Conduction Loss
- Low C<sub>iss</sub> to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- Pb-Free Packages are Available

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	25	Vdc
Gate-to-Source Voltage - Continuous	V <sub>GS</sub>	±20	Vdc
Thermal Resistance, Junction-to-Case Total Power Dissipation @ T <sub>C</sub> = 25°C Drain Current	R <sub>θJC</sub> P <sub>D</sub>	5.6 22.3	°C/W W
- Continuous @ T <sub>C</sub> = 25°C, Chip - Continuous @ T <sub>C</sub> = 25°C, Limited by Package	I <sub>D</sub> I <sub>D</sub>	23 17.1	A A
- Single Pulse	I <sub>DM</sub>	40	Α
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	76	°C/W
Total Power Dissipation @ T <sub>A</sub> = 25°C Drain Current – Continuous @ T <sub>A</sub> = 25°C	P <sub>D</sub> I <sub>D</sub>	1.64 4.5	W A
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	110	°C/W
Total Power Dissipation @ T <sub>A</sub> = 25°C Drain Current – Continuous @ T <sub>A</sub> = 25°C	P <sub>D</sub> I <sub>D</sub>	1.14 3.8	W A
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to 150	°C
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. When surface mounted to an FR4 board using 0.5 sq in pad size.
- When surface mounted to an FR4 board using minimum recommended pad size.

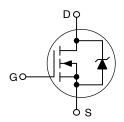


## ON Semiconductor®

## http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
25 V	32 m $\Omega$	23 A

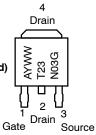
### **N-CHANNEL**



## MARKING DIAGRAMS

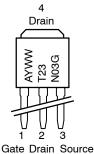


DPAK CASE 369AA (Surface Mounted) STYLE 2





DPAK-3 CASE 369D (Straight Lead) STYLE 2



T23N03 = Device Code A = Assembly Location

Y = Year
WW = Work Week
G = Pb-Free Package

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise specified)

Cha	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS		-	-	-	<u>-</u>	-
Drain-to-Source Breakdown Voltag (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μΑ Temperature Coefficient (Positive)	V(br) <sub>DSS</sub>	25 -	28 -	- -	Vdc mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)		I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0	Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) $ (V_{DS} = V_{GS},  I_D = 250  \mu Adc) $ Threshold Temperature Coefficient (Negative)			1.0 -	1.8 -	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resista $(V_{GS} = 4.5 \text{ Vdc}, I_D = 6 \text{ Add})$ $(V_{GS} = 10 \text{ Vdc}, I_D = 6 \text{ Add})$	R <sub>DS(on)</sub>	- -	50.3 32.3	60 45	mΩ	
Forward Transconductance (Note 3) $(V_{DS} = 10 \text{ Vdc}, I_D = 6 \text{ Add})$	9FS	-	13	-	Mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance		C <sub>iss</sub>	_	225	_	pF
Output Capacitance	$(V_{DS} = 20 \text{ Vdc}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz})$	C <sub>oss</sub>	-	108	_	
Transfer Capacitance		C <sub>rss</sub>	-	48	-	
SWITCHING CHARACTERISTICS (	(Note 4)					
Turn-On Delay Time		t <sub>d(on)</sub>	_	2.0	-	ns
Rise Time	(V <sub>GS</sub> = 10 Vdc, V <sub>DD</sub> = 10 Vdc,	t <sub>r</sub>	_	14.9	_	
Turn-Off Delay Time	$I_D = 6 \text{ Adc}, R_G = 3 \Omega$	t <sub>d(off)</sub>	_	9.9	_	
Fall Time		t <sub>f</sub>	_	2.0	_	
Gate Charge		Q <sub>T</sub>	- 3.76 -		_	nC
	(V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 6 Adc, V <sub>DS</sub> = 10 Vdc) (Note 3)	Q <sub>1</sub>	_	1.7	_	
	, , ,	$Q_2$	-	1.6	-	
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
Forward On-Voltage	$(I_S = 6 \text{ Adc}, V_{GS} = 0 \text{ Vdc}) \text{ (Note 3)}$ $(I_S = 6 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$	V <sub>SD</sub>	- -	0.87 0.74	1.2 -	Vdc
Reverse Recovery Time		t <sub>rr</sub>	-	8.7	-	ns
	(I <sub>S</sub> = 6 Adc, V <sub>GS</sub> = 0 Vdc,	t <sub>a</sub>	-	5.2	-	
	$dI_S/dt = 100 A/\mu s)$ (Note 3)	t <sub>b</sub>	-	3.5	_	

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

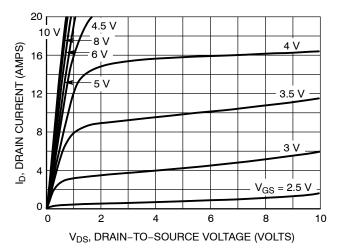


Figure 1. On-Region Characteristics

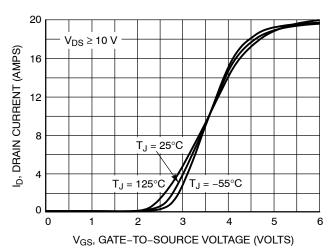


Figure 2. Transfer Characteristics

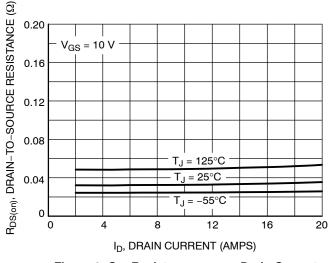


Figure 3. On-Resistance versus Drain Current and Temperature

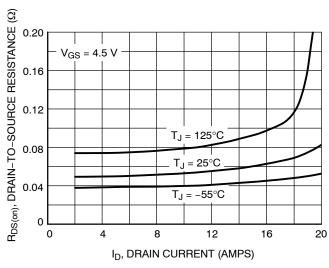


Figure 4. On-Resistance versus Drain Current and Temperature

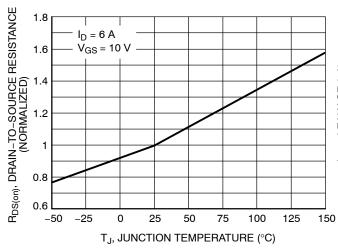


Figure 5. On–Resistance Variation with Temperature

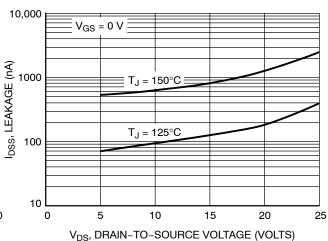


Figure 6. Drain-to-Source Leakage Current versus Voltage

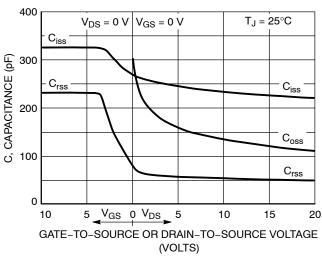


Figure 7. Capacitance Variation

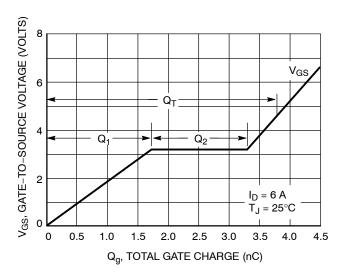


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

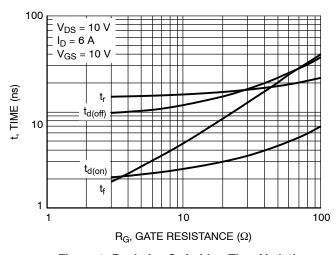


Figure 9. Resistive Switching Time Variation versus Gate Resistance

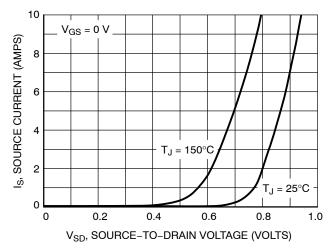


Figure 10. Diode Forward Voltage versus Current

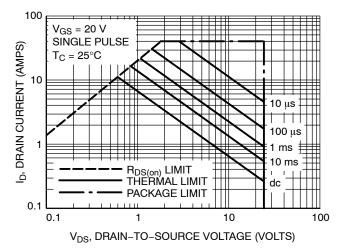


Figure 11. Maximum Rated Forward Biased Safe Operating Area

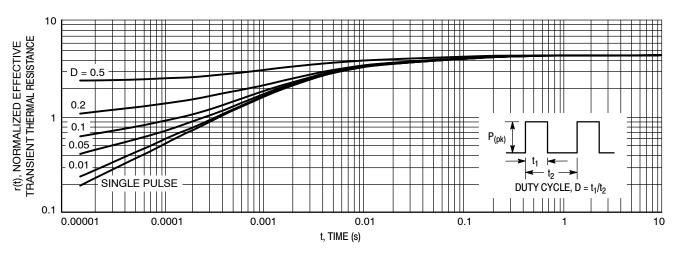


Figure 12. Thermal Response

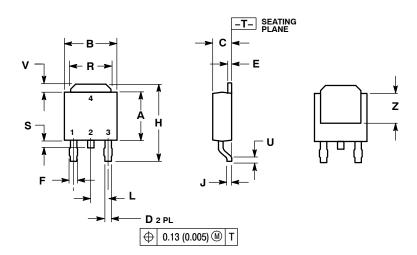
## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NTD23N03RG	DPAK (Pb-Free)	75 Units/Rail
NTD23N03R-1G	DPAK-3 (Pb-Free)	75 Units/Rail
NTD23N03RT4	DPAK	2500 Tape & Reel
NTD23N03RT4G	DPAK (Pb-Free)	2500 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

## **DPAK** CASE 369AA-01 ISSUE O

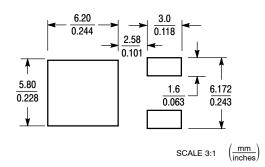


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
E	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
Н	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29	BSC
R	0.180	0.215	4.57	5.45
S	0.024	0.040	0.60	1.01
U	0.020		0.51	
V	0.035	0.050	0.89	1.27
Z	0.155		3.93	

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

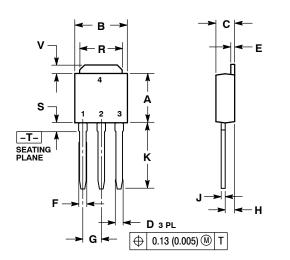
## **SOLDERING FOOTPRINT\***

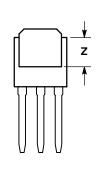


<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PACKAGE DIMENSIONS

DPAK-3 CASE 369D-01 **ISSUE B** 





### NOTES:

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090 BSC		2.29	BSC	
Н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
Κ	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
٧	0.035	0.050	0.89	1.27	
Z	0.155		3.93		

STYLE 2: PIN 1. GATE

- 2. DRAIN
- SOURCE DRAIN 3.

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