PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LH28F320S3HNS-L11

Flash Memory

16M (2MB × 8 / 1MB × 16)

(Model No.: LHF32K03)

Spec No.: EL108029A

Issue Date: December 17, 1998

SHARP

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To; ______________

SPECIFICATIONS

Product Type 32Mbit Flash Memory

LH28F320S3HNS-L11

Model No. (LHF32K03)

※This specifications contains 56 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

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BY: ______________

PRESENTED

BY: M. Okada
M. OKADA
Dept. General Manager

REVIEWED BY: PREPARED BY:

M. Kawaki T. Yoshida

Memory IC Engineering Dept. I
Systems LSI Development Center
Integrated Circuits Group
SHARP CORPORATION

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●Please direct all queries regarding the products covered herein to a sales representative of the company.

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Smart 3 Flash MEMORY

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  - **2.7V, 3.3V or 5V V_{PP}**
- **Common Flash Interface (CFI)**
  - **Universal & Upgradable Interface**
- **Scalable Command Set (SCS)**
- **High Speed Write Performance**
  - **32 Bytes x 2 plane Page Buffer**
  - **2.7 μs/Byte Write Transfer Rate**
- **High Speed Read Performance**
  - **110ns(3.3V±0.3V), 140ns(2.7V-3.6V)**
- **Operating Temperature**
  - **-40°C to +85°C**
- **High-Density Symmetrically-Blocked Architecture**
  - **Sixty-four 64-Kbyte Erasable Blocks**
- **Extended Cycling Capability**
  - **100,000 Block Erase Cycles**
  - **6.4 Million Block Erase Cycles/Chip**
- **Enhanced Automated Suspend Options**
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  - **56-Lead SSOP**
- **ETOX[TM]* V Nonvolatile Flash Technology**
- **CMOS Process (P-type silicon substrate)**
- **Not designed or rated as radiation hardened**

SHARP's LH28F320S3HNS-L11 Flash memory with Smart 3 technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code + data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F320S3HNS-L11 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F320S3HNS-L11 is conformed to the flash Scalable Command Set (SCS) and the Common Flash Interface (CFI) specification which enable universal and upgradable interface, enable the highest system/device data transfer rates and minimize device and system-level implementation costs.

The LH28F320S3HNS-L11 is manufactured on SHARP's 0.4μm ETOX[TM]* V process technology. It come in industry-standard package: the 56-Lead SSOP, ideal for board constrained applications.

*ETOX is a trademark of Intel Corporation.

1 INTRODUCTION

This datasheet contains LH28F320S3HNS-L11 specifications. Section 1 provides a flash memory overview. Sections 2, 3, 4, and 5 describe the memory organization and functionality. Section 6 covers electrical specifications.

1.1 Product Overview

The LH28F320S3HNS-L11 is a high-performance 32-Mbit Smart 3 Flash memory organized as 4MBx8/2MBx16. The 4MB of data is arranged in sixty-four 64-Kbyte blocks which are individually erasable, lockable, and unlockable in-system. The memory map is shown in Figure 3.

Smart 3 technology provides a choice of V_{CC} and V_{PP} combinations, as shown in Table 1, to meet system performance and power expectations. 2.7V V_{CC} consumes approximately one-fifth the power of 5V V_{CC}. V_{PP} at 2.7V and 3.3V eliminates the need for a separate 12V converter. In addition to flexible erase and program voltages, the dedicated V_{PP} pin gives complete data protection when $V_{PP} \leq V_{PPLK}$.

Table 1. V_{CC} and V_{PP} Voltage Combinations Offered by Smart 3 Technology

V_{CC} Voltage	V_{PP} Voltage
2.7V	2.7V, 3.3V, 5V
3.3V	3.3V, 5V

Internal V_{CC} and V_{PP} detection Circuitry automatically configures the device for optimized read and write operations.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

A block erase operation erases one of the device's 64-Kbyte blocks typically within 0.41s (3.3V V_{CC}, 5V V_{PP}) independent of other blocks. Each block can be independently erased 100,000 times (6.4 million block erases per device). Block erase suspend mode allows system software to suspend block erase to read or write data from any other block.

A word/byte write is performed in byte increments typically within 12.95µs (3.3V V_{CC}, 5V V_{PP}). A multi word/byte write has high speed write performance of 2.7µs/byte (3.3V V_{CC}, 5V V_{PP}). (Multi) Word/byte write suspend mode enables the system to read data or execute code from any other flash memory array location.

Individual block locking uses a combination of bits and WP#, Sixty-four block lock-bits, to lock and unlock blocks. Block lock-bits gate block erase, full chip erase and (multi) word/byte write operations. Block lock-bit configuration operations (Set Block Lock-Bit and Clear Block Lock-Bits commands) set and cleared block lock-bits.

The status register indicates when the WSM's block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is finished.

The STS output gives an additional indicator of WSM activity by providing both a hardware signal of status (versus software polling) and status masking (interrupt masking for background block erase, for example). Status polling using STS minimizes both CPU overhead and system power consumption. STS pin can be configured to different states using the Configuration command. The STS pin defaults to RY/BY# operation. When low, STS indicates that the WSM is performing a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration. STS-High Z indicates that the WSM is ready for a new command, block erase is suspended and (multi) word/byte write are inactive, (multi) word/byte write are suspended, or the device is in deep power-down mode. The other 3 alternate configurations are all pulse mode for use as a system interrupt.

The access time is 110ns (t_{AVQV}) over the extended temperature range (-40°C to +85°C) and V_{CC} supply voltage range of 3.0V-3.6V. At lower V_{CC} voltage, the access time is 140ns (2.7V-3.6V).

The Automatic Power Savings (APS) feature substantially reduces active current when the device is in static mode (addresses not switching). In APS mode, the typical I_{CCR} current is 3 mA at 3.3V V_{CC}.

When either CE_0# or CE_1#, and RP# pins are at V_{CC}, the I_{CC} CMOS standby mode is enabled. When the RP# pin is at GND, deep power-down mode is enabled which minimizes power consumption and provides write protection during reset. A reset time (t_{PHQV}) is required from RP# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHEL}) from RP#-high until writes to the CUI are recognized. With RP# at GND, the WSM is reset and the status register is cleared.

The device is available in 56-Lead SSOP (Shrink Small Outline Package). Pinout is shown in Figure 2.

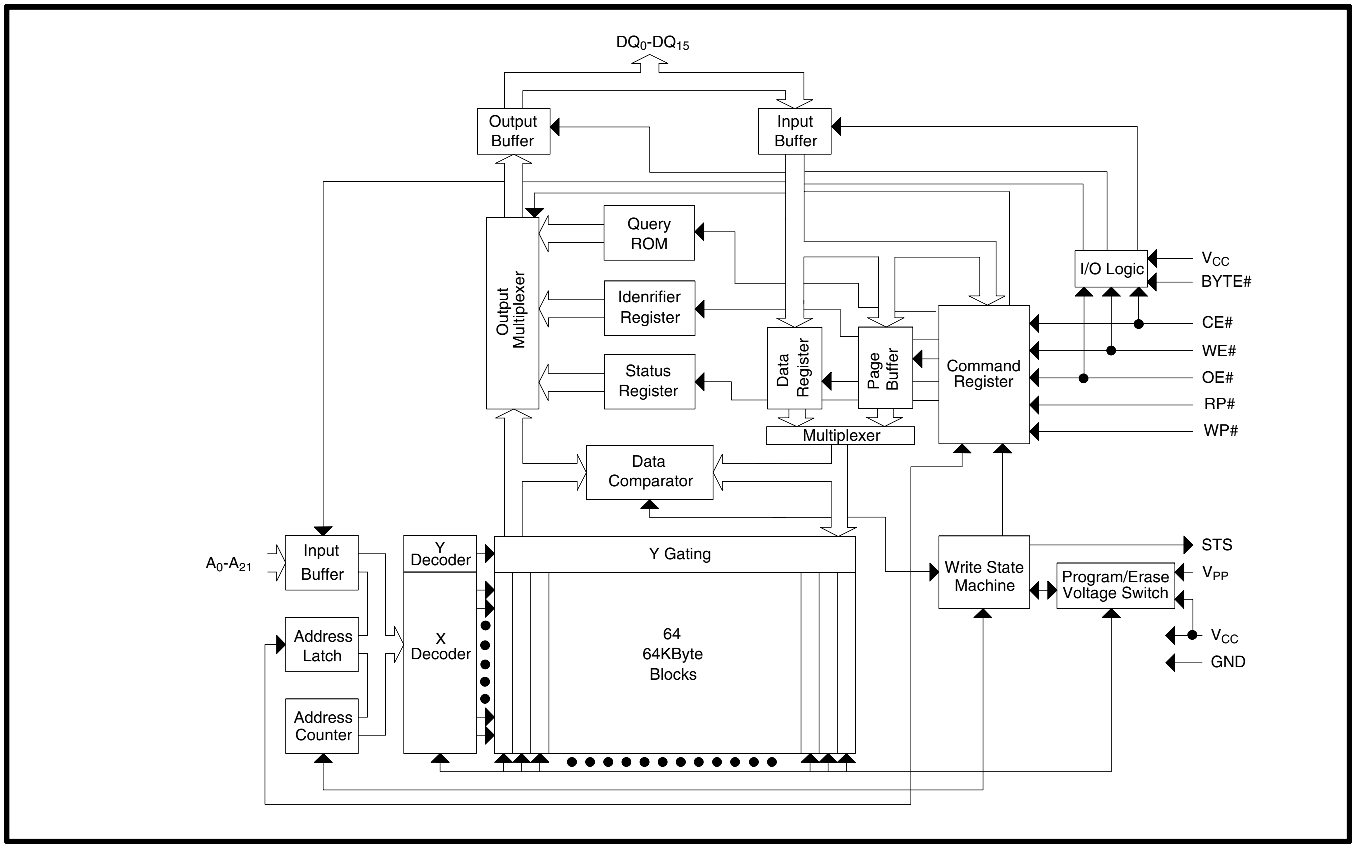


Figure 1. Block Diagram

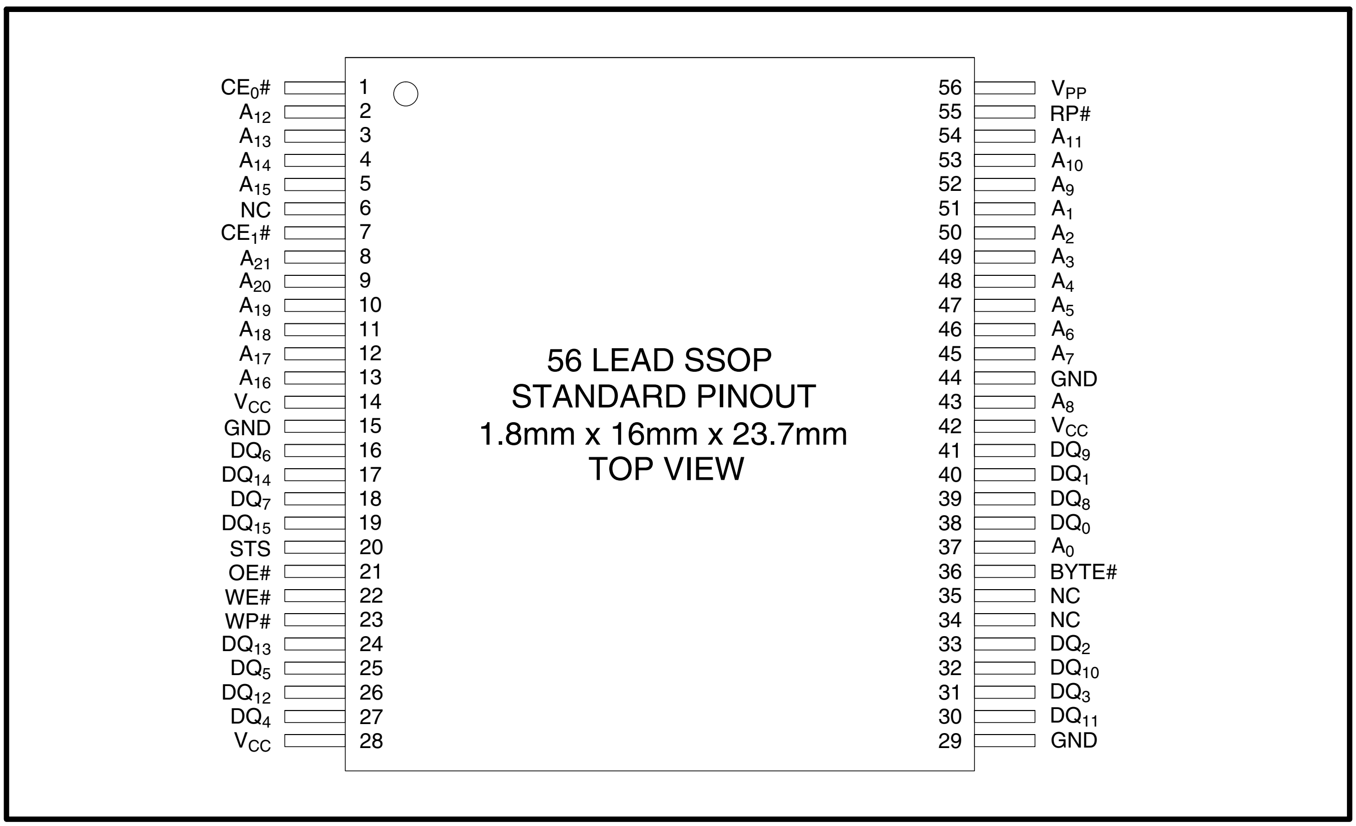


Figure 2. SSOP 56-Lead Pinout

Table 2. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{21}	INPUT	**ADDRESS INPUTS:** Inputs for addresses during read and write operations. Addresses are internally latched during a write cycle. A0: Byte Select Address. Not used in x16 mode(can be floated). A1-A4: Column Address. Selects 1 of 16 bit lines. A5-A15: Row Address. Selects 1 of 2048 word lines. A16-A21 : Block Address.
DQ_0-DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUTS:** DQ_0-DQ_7:Inputs data and commands during CUI write cycles; outputs data during memory array, status register, query, and identifier code read cycles. Data pins float to high-impedance when the chip is deselected or outputs are disabled. Data is internally latched during a write cycle. DQ_8-DQ_{15}:Inputs data during CUI write cycles in x16 mode; outputs data during memory array read cycles in x16 mode; not used for status register, query and identifier code read mode. Data pins float to high-impedance when the chip is deselected, outputs are disabled, or in x8 mode(Byte#=V_{IL}). Data is internally latched during a write cycle.
CE_0#, CE_1#	INPUT	**CHIP ENABLE:** Activates the device's control logic, input buffers decoders, and sense amplifiers. Either CE_0# or CE_1# V_{IH} deselects the device and reduces power consumption to standby levels. Both CE_0# and CE_1# must be V_{IL} to select the devices.
RP#	INPUT	**RESET/DEEP POWER-DOWN:** Puts the device in deep power-down mode and resets internal automation. RP# V_{IH} enables normal operation. When driven V_{IL}, RP# inhibits write operations which provides data protection during power transitions. Exit from deep power-down sets the device to read array mode.
OE#	INPUT	**OUTPUT ENABLE:** Gates the device's outputs during a read cycle.
WE#	INPUT	**WRITE ENABLE:** Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of the WE# pulse.
STS	OPEN DRAIN OUTPUT	**STS (RY/BY#):** Indicates the status of the internal WSM. When configured in level mode (default mode), it acts as a RY/BY# pin. When low, the WSM is performing an internal operation (block erase, full chip erase, (multi) word/byte write or block lock-bit configuration). STS High Z indicates that the WSM is ready for new commands, block erase is suspended, and (multi) word/byte write is inactive, (multi) word/byte write is suspended or the device is in deep power-down mode. For alternate configurations of the STATUS pin, see the Configuration command.
WP#	INPUT	**WRITE PROTECT:** Master control for block locking. When V_{IL}, Locked blocks can not be erased and programmed, and block lock-bits can not be set and reset.
BYTE#	INPUT	**BYTE ENABLE:** BYTE# V_{IL} places device in x8 mode. All data is then input or output on DQ_{0-7}, and DQ_{8-15} float. BYTE# V_{IH} places the device in x16 mode , and turns off the A_0 input buffer.
V_{PP}	SUPPLY	**BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE, BLOCK LOCK-BIT CONFIGURATION POWER SUPPLY:** For erasing array blocks, writing bytes or configuring block lock-bits. With $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration with an invalid V_{PP} (see DC Characteristics) produce spurious results and should not be attempted.
V_{CC}	SUPPLY	**DEVICE POWER SUPPLY:** Internal detection configures the device for 2.7V or 3.3V operation. To switch from one voltage to another, ramp V_{CC} down to GND and then ramp V_{CC} to the new voltage. Do not float any power pins. With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
GND	SUPPLY	**GROUND:** Do not float any ground pins.
NC		**NO CONNECT:** Lead is not internal connected; it may be driven or floated.

2 PRINCIPLES OF OPERATION

The LH28F320S3HNS-L11 Flash memory includes an on-chip WSM to manage block erase, full chip erase, (multi) word/byte write and block lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, and minimal processor overhead with RAM-Like interface timings.

After initial device power-up or return from deep power-down mode (see Bus Operations), the device defaults to read array mode. Manipulation of external memory control pins allow array read, standby, and output disable operations.

Status register, query structure and identifier codes can be accessed through the CUI independent of the V_{PP} voltage. High voltage on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. All functions associated with altering memory contents—block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, status, query and identifier codes—are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. The CUI contents serve as input to the WSM, which controls the block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification, and margining of data. Addresses and data are internally latch during write cycles. Writing the appropriate command outputs array data, accesses the identifier codes, outputs query structure or outputs status register data.

Interface software that initiates and polls progress of block erase, full chip erase, (multi) word/byte write and block lock-bit configuration can be stored in any block. This code is copied to and executed from system RAM during flash memory updates. After successful completion, reads are again possible via the Read Array command. Block erase suspend allows system software to suspend a block erase to read or write data from any other block. Write suspend allows system software to suspend a (multi) word/byte write to read data from any other flash memory array location.

2.1 Data Protection

Depending on the application, the system designer may choose to make the V_{PP} power supply switchable (available only when block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are required) or hardwired to $V_{PPH1/2/3}$. The device accommodates either design practice and encourages optimization of the processor-memory interface.

When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered. The CUI, with multi-step block erase, full chip erase, (multi) word/byte write and block lock-bit configuration command sequences, provides protection from unwanted operations even when high voltage is applied to V_{PP}. All write functions are disabled when V_{CC} is below the write lockout voltage V_{LKO} or when RP# is at V_{IL}. The device's block locking capability provides additional protection from inadvertent code or data alteration by gating block erase, full chip erase and (multi) word/byte write operations.

Top Address	Bottom Address	Block	Top Address	Bottom Address	Block
1FFFFF	1F0000	64-Kbyte Block 31	3FFFFF	3F0000	64-Kbyte Block 63
1EFFFF	1E0000	64-Kbyte Block 30	3EFFFF	3E0000	64-Kbyte Block 62
1DFFFF	1D0000	64-Kbyte Block 29	3DFFFF	3D0000	64-Kbyte Block 61
1CFFFF	1C0000	64-Kbyte Block 28	3CFFFF	3C0000	64-Kbyte Block 60
1BFFFF	1B0000	64-Kbyte Block 27	3BFFFF	3B0000	64-Kbyte Block 59
1AFFFF	1A0000	64-Kbyte Block 26	3AFFFF	3A0000	64-Kbyte Block 58
19FFFF	190000	64-Kbyte Block 25	39FFFF	390000	64-Kbyte Block 57
18FFFF	180000	64-Kbyte Block 24	38FFFF	380000	64-Kbyte Block 56
17FFFF	170000	64-Kbyte Block 23	37FFFF	370000	64-Kbyte Block 55
16FFFF	160000	64-Kbyte Block 22	36FFFF	360000	64-Kbyte Block 54
15FFFF	150000	64-Kbyte Block 21	35FFFF	350000	64-Kbyte Block 53
14FFFF	140000	64-Kbyte Block 20	34FFFF	340000	64-Kbyte Block 52
13FFFF	130000	64-Kbyte Block 19	33FFFF	330000	64-Kbyte Block 51
12FFFF	120000	64-Kbyte Block 18	32FFFF	320000	64-Kbyte Block 50
11FFFF	110000	64-Kbyte Block 17	31FFFF	310000	64-Kbyte Block 49
10FFFF	100000	64-Kbyte Block 16	30FFFF	300000	64-Kbyte Block 48
0FFFFF	0F0000	64-Kbyte Block 15	2FFFFF	2F0000	64-Kbyte Block 47
0EFFFF	0E0000	64-Kbyte Block 14	2EFFFF	2E0000	64-Kbyte Block 46
0DFFFF	0D0000	64-Kbyte Block 13	2DFFFF	2D0000	64-Kbyte Block 45
0CFFFF	0C0000	64-Kbyte Block 12	2CFFFF	2C0000	64-Kbyte Block 44
0BFFFF	0B0000	64-Kbyte Block 11	2BFFFF	2B0000	64-Kbyte Block 43
0AFFFF	0A0000	64-Kbyte Block 10	2AFFFF	2A0000	64-Kbyte Block 42
09FFFF	090000	64-Kbyte Block 9	29FFFF	290000	64-Kbyte Block 41
08FFFF	080000	64-Kbyte Block 8	28FFFF	280000	64-Kbyte Block 40
07FFFF	070000	64-Kbyte Block 7	27FFFF	270000	64-Kbyte Block 39
06FFFF	060000	64-Kbyte Block 6	26FFFF	260000	64-Kbyte Block 38
05FFFF	050000	64-Kbyte Block 5	25FFFF	250000	64-Kbyte Block 37
04FFFF	040000	64-Kbyte Block 4	24FFFF	240000	64-Kbyte Block 36
03FFFF	030000	64-Kbyte Block 3	23FFFF	230000	64-Kbyte Block 35
02FFFF	020000	64-Kbyte Block 2	22FFFF	220000	64-Kbyte Block 34
01FFFF	010000	64-Kbyte Block 1	21FFFF	210000	64-Kbyte Block 33
00FFFF	000000	64-Kbyte Block 0	20FFFF	200000	64-Kbyte Block 32

Figure 3. Memory Map

3 BUS OPERATION

The local CPU reads and writes flash memory in-system. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

3.1 Read

Information can be read from any block, identifier codes, query structure, or status register independent of the V_{PP} voltage. RP# must be at V_{IH}.

The first task is to write the appropriate read mode command (Read Array, Read Identifier Codes, Query or Read Status Register) to the CUI. Upon initial device power-up or after exit from deep power-down mode, the device automatically resets to read array mode. Five control pins dictate the data flow in and out of the component: CE# (CE_0#, CE_1#), OE#, WE#, RP# and WP#. CE_0#, CE_1# and OE# must be driven active to obtain data at the outputs. CE_0#, CE_1# is the device selection control, and when active enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and when active drives the selected memory data onto the I/O bus. WE# and RP# must be at V_{IH}. Figure 17, 18 illustrates a read cycle.

3.2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Output pins DQ_0-DQ_{15} are placed in a high-impedance state.

3.3 Standby

Either CE_0# or CE_1# at a logic-high level (V_{IH}) places the device in standby mode which substantially reduces device power consumption. DQ_0-DQ_{15} outputs are placed in a high-impedance state independent of OE#. If deselected during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration, the device continues functioning, and consuming active power until the operation completes.

3.4 Deep Power-Down

RP# at V_{IL} initiates the deep power-down mode.

In read modes, RP#-low deselects the memory, places output drivers in a high-impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t_{PHQV} is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase, full chip erase, (multi) word/byte write or block lock-bit configuration modes, RP#-low will abort the operation. STS remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written. Time t_{PHWL} is required after RP# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RP# during system reset. When the system comes out of reset, it expects to read from the flash memory. Automated flash memories provide status information when accessed during block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. SHARP's flash memories allow proper CPU initialization following a system reset through the use of the RP# input. In this application, RP# is controlled by the same RESET# signal that resets the system CPU.

3.5 Read Identifier Codes Operation

The read identifier codes operation outputs the manufacturer code, device code, block status codes for each block (see Figure 4). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block status codes identify locked or unlocked block setting and erase completed or erase uncompleted condition.

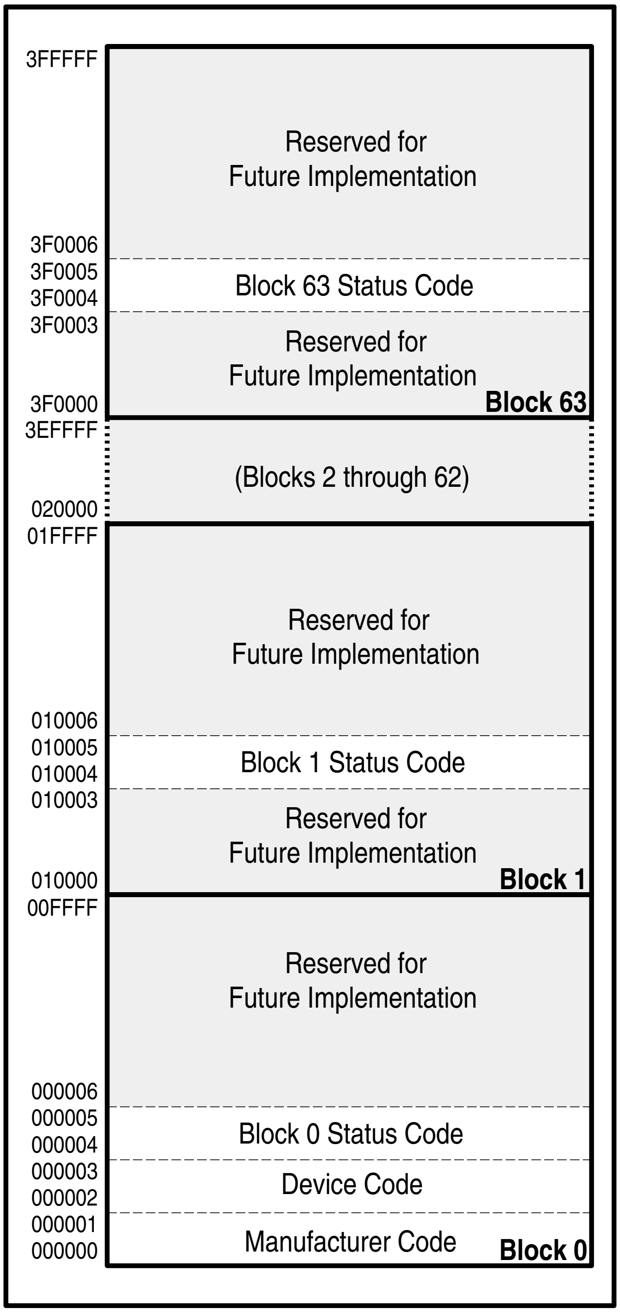


Figure 4. Device Identifier Code Memory Map

3.6 Query Operation

The query operation outputs the query structure. Query database is stored in the 48Byte ROM. Query structure allows system software to gain critical information for controlling the flash component. Query structure are always presented on the lowest-order data output (DQ_0-DQ_7) only.

3.7 Write

Writing commands to the CUI enable reading of device data and identifier codes. They also control inspection and clearing of the status register. When $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$, the CUI additionally controls block erase, full chip erase, (multi) word/byte write and block lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word/byte Write command requires the command and address of the location to be written. Set Block Lock-Bit command requires the command and block address within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is written when WE# and CE# are active. The address and data needed to execute a command are latched on the rising edge of WE# or CE# (whichever goes high first). Standard microprocessor write timings are used. Figures 19 and 20 illustrate WE# and CE#-controlled write operations.

4 COMMAND DEFINITIONS

When the V_{PP} voltage $\leq V_{PPLK,}$ Read operations from the status register, identifier codes, query, or blocks are enabled. Placing $V_{PPH1/2/3}$ on V_{PP} enables successful block erase, full chip erase, (multi) word/byte write and block lock-bit configuration operations.

Device operations are selected by writing specific commands into the CUI. Table 4 defines these commands.

Table 3. Bus Operations(BYTE#=V_{IH})

Mode	Notes	RP#	CE_0#	CE_1#	OE#	WE#	Address	V_{PP}	DQ_{0-15}	STS
Read	1,2,3,9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH}	V_{IH} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes	9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	High Z
Query	9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 7~11	X	Note 6	High Z
Write	3,7,8,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

Table 3.1. Bus Operations(BYTE#=V_{IL})

Mode	Notes	RP#	CE_0#	CE_1#	OE#	WE#	Address	V_{PP}	DQ_{0-7}	STS
Read	1,2,3,9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}	X
Output Disable	3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z	X
Standby	3	V_{IH}	V_{IH} V_{IH} V_{IL}	V_{IH} V_{IL} V_{IH}	X	X	X	X	High Z	X
Deep Power-Down	4	V_{IL}	X	X	X	X	X	X	High Z	High Z
Read Identifier Codes	9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Figure 4	X	Note 5	High Z
Query	9	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	See Table 7~11	X	Note 6	High Z
Write	3,7,8,9	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}	X

NOTES:

1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but not altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2/3}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2/3}$ voltages.
3. STS is V_{OL} (if configured to RY/BY# mode) when the WSM is executing internal block erase, full chip erase, (multi) word/byte write or block lock-bit configuration algorithms. It is floated during when the WSM is not busy, in block erase suspend mode with (multi) word/byte write inactive, (multi) word/byte write suspend mode, or deep power-down mode.
4. RP# at GND±0.2V ensures the lowest deep power-down current.
5. See Section 4.2 for read identifier code data.
6. See Section 4.5 for query data.
7. Command writes involving block erase, full chip erase, (multi) word/byte write or block lock-bit configuration are reliably executed when $V_{PP}=V_{PPH1/2/3}$ and $V_{CC}=V_{CC1/2}$.
8. Refer to Table 4 for valid D_{IN} during a write operation.
9. Don't use the timing both OE# and WE# are V_{IL}.

Table 4. Command Definitions(10)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array/Reset	1		Write	X	FFH			
Read Identifier Codes	≥2	4	Write	X	90H	Read	IA	ID
Query	≥2		Write	X	98H	Read	QA	QD
Read Status Register	2		Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Block Erase Setup/Confirm	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase Setup/Confirm	2		Write	X	30H	Write	X	D0H
Word/Byte Write Setup/Write	2	5,6	Write	WA	40H	Write	WA	WD
Alternate Word/Byte Write Setup/Write	2	5,6	Write	WA	10H	Write	WA	WD
Multi Word/Byte Write Setup/Confirm	≥4	9	Write	WA	E8H	Write	WA	N-1
Block Erase and (Multi) Word/byte Write Suspend	1	5	Write	X	B0H			
Confirm and Block Erase and (Multi) Word/byte Write Resume	1	5	Write	X	D0H			
Block Lock-Bit Set Setup/Confirm	2	7	Write	BA	60H	Write	BA	01H
Block Lock-Bit Reset Setup/Confirm	2	8	Write	X	60H	Write	X	D0H
STS Configuration Level-Mode for Erase and Write (RY/BY# Mode)	2		Write	X	B8H	Write	X	00H
STS Configuration Pulse-Mode for Erase	2		Write	X	B8H	Write	X	01H
STS Configuration Pulse-Mode for Write	2		Write	X	B8H	Write	X	02H
STS Configuration Pulse-Mode for Erase and Write	2		Write	X	B8H	Write	X	03H

NOTES:

1. BUS operations are defined in Table 3 and Table 3.1.
2. X=Any valid address within the device.
   IA=Identifier Code Address: see Figure 4.
   QA=Query Offset Address.
   BA=Address within the block being erased or locked.
   WA=Address of memory location to be written.
3. SRD=Data read from status register. See Table 14 for a description of the status register bits.
   WD=Data to be written at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   ID=Data read from identifier codes.
   QD=Data read from query database.
4. Following the Read Identifier Codes command, read operations access manufacturer, device and block status codes. See Section 4.2 for read identifier code data.
5. If the block is locked, WP# must be at V_{IH} to enable block erase or (multi) word/byte write operations. Attempts to issue a block erase or (multi) word/byte write to a locked block while RP# is V_{IH}.
6. Either 40H or 10H are recognized by the WSM as the byte write setup.
7. A block lock-bit can be set while WP# is V_{IH}.
8. WP# must be at V_{IH} to clear block lock-bits. The clear block lock-bits operation simultaneously clears all block lock-bits.
9. Following the Third Bus Cycle, inputs the write address and write data of 'N' times. Finally, input the confirm command 'D0H'.
10. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

4.1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the device defaults to read array mode. This operation is also initiated by writing the Read Array command. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend and (Multi) Word/byte Write Suspend command. The Read Array command functions independently of the V_{PP} voltage and RP# must be V_{IH}.

4.2 Read Identifier Codes Command

The identifier code operation is initiated by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Figure 4 retrieve the manufacturer, device, block lock configuration and block erase status (see Table 5 for identifier code values). To terminate the operation, write another valid command. Like the Read Array command, the Read Identifier Codes command functions independently of the V_{PP} voltage and RP# must be V_{IH}. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes

Code	Address A_{21}-A_0	Data
Manufacture Code	000000 000001	B0
Device Code	000002 000003	D4
Block Status Code	X0004(1) X0005(1)	
•Block is Unlocked		DQ_0=0
•Block is Locked		DQ_0=1
•Last erase operation completed successfully		DQ_1=0
•Last erase operation did not completed successfully		DQ_1=1
•Reserved for Future Use		DQ_{2-7}

NOTE:
1. X selects the specific block status code to be read. See Figure 4 for the device identifier code memory map.

4.3 Read Status Register Command

The status register may be read to determine when a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration is complete and whether the operation completed successfully(see Table 14). It may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or CE#(Either CE_0# or CE_1#), whichever occurs. OE# or CE#(Either CE_0# or CE_1#) must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage. RP# must be V_{IH}.

The extended status register may be read to determine multi word/byte write availability(see Table 14.1). The extended status register may be read at any time by writing the Multi Word/Byte Write command. After writing this command, all subsequent read operations output data from the extended status register, until another valid command is written. Multi Word/Byte Write command must be re-issued to update the extended status register latch.

4.4 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 14). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking multiple blocks or writing several bytes in sequence) may be performed. The status register may be polled to determine if an error occurs during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. It functions independently of the applied V_{PP} Voltage. RP# must be V_{IH}. This command is not functional during block erase, full chip erase, (multi) word/byte write block lock-bit configuration, block erase suspend or (multi) word/byte write suspend modes.

4.5 Query Command

Query database can be read by writing Query command (98H). Following the command write, read cycle from address shown in Table 7~11 retrieve the critical information to write, erase and otherwise control the flash component. A_0 of query offset address is ignored when X8 mode (BYTE#=V_{IL}).

Query data are always presented on the low-byte data output (DQ_0-DQ_7). In x16 mode, high-byte (DQ_8-DQ_{15}) outputs 00H. The bytes not assigned to any information or reserved for future use are set to "0". This command functions independently of the V_{PP} voltage. RP# must be V_{IH}.

Table 6. Example of Query Structure Output

Mode	Offset Address	Output	
		$DQ_{15\sim8}$	$DQ_{7\sim0}$
X8 mode	A_5, A_4, A_3, A_2, A_1, A_0		
	1 , 0 , 0 , 0 , 0 , 0 (20H)	High-Z	"Q"
	1 , 0 , 0 , 0 , 0 , 1 (21H)	High-Z	"Q"
	1, 0 , 0 , 0 , 1 , 0 (22H)	High-Z	"R"
	1 , 0 , 0 , 0 , 1 , 1 (23H)	High-Z	"R"
X16 mode	A_5, A_4, A_3, A_2, A_1		
	1 , 0 , 0 , 0 , 0 (10H)	00H	"Q"
	1 , 0 , 0 , 0 , 1 (11H)	00H	"R"

4.5.1 Block Status Register

This field provides lock configuration and erase status for the specified block. These informations are only available when device is ready (SR.7=1). If block erase or full chip erase operation is finished irregulary, block erase status bit will be set to "1". If bit 1 is "1", this block is invalid.

Table 7. Query Block Status Register

Offset (Word Address)	Length	Description
(BA+2)H	01H	Block Status Register bit0 Block Lock Configuration 0=Block is unlocked 1=Block is Locked bit1 Block Erase Status 0=Last erase operation completed successfully 1=Last erase operation not completed successfully bit2-7 reserved for future use

Note:
1. BA=The beginning of a Block Address.

4.5.2 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. Additionally, it indicates which version of the spec and which Vendor-specified command set(s) is(are) supported.

Table 8. CFI Query Identification String

Offset (Word Address)	Length	Description
10H,11H,12H	03H	Query Unique ASCII string "QRY" 51H,52H,59H
13H,14H	02H	Primary Vendor Command Set and Control Interface ID Code 01H,00H (SCS ID Code)
15H,16H	02H	Address for Primary Algorithm Extended Query Table 31H,00H (SCS Extended Query Table Offset)
17H,18H	02H	Alternate Vendor Command Set and Control Interface ID Code 0000H (0000H means that no alternate exists)
19H,1AH	02H	Address for Alternate Algorithm Extended Query Table 0000H (0000H means that no alternate exists)

4.5.3 System Interface Information

The following device information can be useful in optimizing system interface software.

Table 9. System Information String

Offset (Word Address)	Length	Description
1BH	01H	V_{CC} Logic Supply Minimum Write/Erase voltage 27H (2.7V)
1CH	01H	V_{CC} Logic Supply Maximum Write/Erase voltage 36H (3.6V)
1DH	01H	V_{PP} Programming Supply Minimum Write/Erase voltage 27H (2.7V)
1EH	01H	V_{PP} Programming Supply Maximum Write/Erase voltage 55H (5.5V)
1FH	01H	Typical Timeout per Single Byte/Word Write 04H (2^4=16µs)
20H	01H	Typical Timeout for Maximum Size Buffer Write (32 Bytes) 06H (2^6=64µs)
21H	01H	Typical Timeout per Individual Block Erase 09H (09H=9, 2^9=512ms)
22H	01H	Typical Timeout for Full Chip Erase 0FH (0FH=15, 2^{15}=32768ms)
23H	01H	Maximum Timeout per Single Byte/Word Write, 2^N times of typical. 04H (2^4=16, 16µsx16=256µs)
24H	01H	Maximum Timeout Maximum Size Buffer Write, 2^N times of typical. 04H (2^4=16, 64µsx16=1024µs)
25H	01H	Maximum Timeout per Individual Block Erase, 2^N times of typical. 04H (2^4=16, 1024msx16=16384ms)
26H	01H	Maximum Timeout for Full Chip Erase, 2^N times of typical. 04H (2^4=16, 32768msx16=524288ms)

4.5.4 Device Geometry Definition

This field provides critical details of the flash device geometry.

Table 10. Device Geometry Definition

Offset (Word Address)	Length	Description
27H	01H	Device Size 16H (16H=22, 2^{22}=4194304=4M Bytes)
28H,29H	02H	Flash Device Interface description 02H,00H (x8/x16 supports x8 and x16 via BYTE#)
2AH,2BH	02H	Maximum Number of Bytes in Multi-byte 05H,00H (2^5=32 Bytes)
2CH	01H	Number of Erase Block Regions within device 01H (symmetrically blocked)
2DH,2EH	02H	The Number of Erase Blocks 3FH,00H (3FH=63 ==> 63+1=64 Blocks)
2FH,30H	02H	The Number of "256 Bytes" cluster in a Erase block 00H,01H (0100H=256 ==>256 Bytes x 256= 64K Bytes in a Erase Block)

4.5.5 SCS OEM Specific Extended Query Table

Certain flash features and commands may be optional in a vendor-specific algorithm specification. The optional vendor-specific Query table(s) may be used to specify this and other types of information. These structures are defined solely by the flash vendor(s).

Table 11. SCS OEM Specific Extended Query Table

Offset (Word Address)	Length	Description
31H,32H,33H	03H	PRI 50H,52H,49H
34H	01H	31H (1) Major Version Number , ASCII
35H	01H	30H (0) Minor Version Number, ASCII
36H,37H, 38H,39H	04H	0FH,00H,00H,00H Optional Command Support bit0=1 : Chip Erase Supported bit1=1 : Suspend Erase Supported bit2=1 : Suspend Write Supported bit3=1 : Lock/Unlock Supported bit4=0 : Queued Erase Not Supported bit5-31=0 : reserved for future use
3AH	01H	01H Supported Functions after Suspend bit0=1 : Write Supported after Erase Suspend bit1-7=0 : reserved for future use
3BH,3CH	02H	03H,00H Block Status Register Mask bit0=1 : Block Status Register Lock Bit [BSR.0] active bit1=1 : Block Status Register Valid Bit [BSR.1] active bit2-15=0 : reserved for future use
3DH	01H	V_{CC} Logic Supply Optimum Write/Erase voltage(highest performance) 33H(3.3V)
3EH	01H	V_{PP} Programming Supply Optimum Write/Erase voltage(highest performance) 50H(5.0V)
3FH	reserved	Reserved for future versions of the SCS Specification

4.6 Block Erase Command

Block erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires appropriate sequencing and an address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read (see Figure 5). The CPU can detect block erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable block erasure can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If block erase is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". Successful block erase requires that the corresponding block lock-bit be cleared or if set, that WP#=V_{IH}. If block erase is attempted when the corresponding block lock-bit is set and WP#=V_{IL}, SR.1 and SR.5 will be set to "1".

4.7 Full Chip Erase Command

This command followed by a confirm command (D0H) erases all of the unlocked blocks. A full chip erase setup is first written, followed by a full chip erase confirm. After a confirm command is written, device erases the all unlocked blocks from block 0 to Block 63 block by block. This command sequence requires appropriate sequencing. Block preconditioning, erase and verify are handled internally by the WSM (invisible to the system). After the two-cycle full chip erase sequence is written, the device automatically outputs status register data when read (see Figure 6). The CPU can detect full chip erase completion by analyzing the output data of the STS pin or status register bit SR.7.

When the full chip erase is complete, status register bit SR.5 should be checked. If erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued. If error is detected on a block during full chip erase operation, WSM stops erasing the block and begin to erase the next block. Reading the block valid status by issuing Read ID Codes command or Query command informs which blocks failed to its erase.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in both status register bits SR.4 and SR.5 being set to "1". Also, reliable full chip erasure can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block contents are protected against erasure. If full chip erase is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". When WP#=V_{IH}, all blocks are erased independent of block lock-bits status. When WP#=V_{IL}, only unlocked blocks are erased. Full chip erase can not be suspended.

4.8 Word/Byte Write Command

Word/byte write is executed by a two-cycle command sequence. Word/Byte Write setup (standard 40H or alternate 10H) is written, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word/byte write and write verify algorithms internally. After the word/byte write sequence is written, the device automatically outputs status register data when read (see Figure 7). The CPU can detect the completion of the word/byte write event by analyzing the STS pin or status register bit SR.7.

When word/byte write is complete, status register bit SR.4 should be checked. If word/byte write error is detected, the status register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The CUI remains in read status register mode until it receives another command.

Reliable word/byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against word/byte writes. If word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful word/byte write requires that the corresponding block lock-bit be cleared or, if set, that WP#=V_{IH}. If word/byte write is attempted when the corresponding block lock-bit is set and WP#=V_{IL}, SR.1 and SR.4 will be set to "1". Word/byte write operations with V_{IL}<WP#<V_{IH} produce spurious results and should not be attempted.

4.9 Multi Word/Byte Write Command

Multi word/byte write is executed by at least four-cycle or up to 35-cycle command sequence. Up to 32 bytes in x8 mode (16 words in x16 mode) can be loaded into the buffer and written to the Flash Array. First, multi word/byte write setup (E8H) is written with the write address. At this point, the device automatically outputs extended status register data (XSR) when read (see Figure 8, 9). If extended status register bit XSR.7 is 0, no Multi Word/Byte Write command is available and multi word/byte write setup which just has been written is ignored. To retry, continue monitoring XSR.7 by writing multi word/byte write setup with write address until XSR.7 transitions to 1. When XSR.7 transitions to 1, the device is ready for loading the data to the buffer. A word/byte count (N)-1 is written with write address. After writing a word/byte count(N)-1, the device automatically turns back to output status register data. The word/byte count (N)-1 must be less than or equal to 1FH in x8 mode (0FH in x16 mode). On the next write, device start address is written with buffer data. Subsequent writes provide additional device address and data, depending on the count. All subsequent address must lie within the start address plus the count. After the final buffer data is written, write confirm (D0H) must be written. This initiates WSM to begin copying the buffer data to the Flash Array. An invalid Multi Word/Byte Write command sequence will result in both status register bits SR.4 and SR.5 being set to "1". For additional multi word/byte write, write another multi word/byte write setup and check XSR.7. The Multi Word/Byte Write command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH28F320S3HNS-L11 has two buffers. If an error occurs while writing, the device will stop writing and flush next multi word/byte write command loaded in multi word/byte write command. Status register bit SR.4 will be set to "1". No multi word/byte write command is available if either SR.4 or SR.5 are set to "1". SR.4 and SR.5 should be cleared before issuing multi word/byte write command. If a multi word/byte write command is attempted past an erase block boundary, the device will write the data to Flash Array up to an erase block boundary and then stop writing. Status register bits SR.4 and SR.5 will be set to "1".

Reliable multi byte writes can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, memory contents are protected against multi word/byte writes. If multi word/byte write is attempted while $V_{PP} \leq V_{PPLK}$, status register bits SR.3 and SR.4 will be set to "1". Successful multi word/byte write requires that the corresponding block lock-bit be cleared or, if set, that WP#=V_{IH}. If multi byte write is attempted when the corresponding block lock-bit is set and WP#=V_{IL}, SR.1 and SR.4 will be set to "1".

4.10 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or (multi) word/byte-write data in another block of memory. Once the block-erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bits SR.7 and SR.6 can determine when the block erase operation has been suspended (both will be set to "1"). STS will also transition to High Z. Specification t_{WHRH2} defines the block erase suspend latency.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Multi) Word/Byte Write command sequence can also be issued during erase suspend to program data in other blocks. Using the (Multi) Word/Byte Write Suspend command (see Section 4.11), a (multi) word/byte write operation can also be suspended. During a (multi) word/byte write operation with block erase suspended, status register bit SR.7 will return to "0" and the STS (if set to RY/BY#) output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status.

The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and STS will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read (see Figure 10). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for block erase) while block erase is suspended. RP# must also remain at V_{IH}. Block erase cannot resume until (multi) word/byte write operations initiated during block erase suspend have completed.

4.11 (Multi) Word/Byte Write Suspend Command

The (Multi) Word/Byte Write Suspend command allows (multi) word/byte write interruption to read data in other flash memory locations. Once the (multi) word/byte write process starts, writing the (Multi) Word/Byte Write Suspend command requests that the WSM suspend the (multi) word/byte write sequence at a predetermined point in the algorithm. The device continues to output status register data when read after the (Multi) Word/Byte Write Suspend command is written. Polling status register bits SR.7 and SR.2 can determine when the (multi) word/byte write operation has been suspended (both will be set to "1"). STS will also transition to High Z. Specification t_{WHRH1} defines the (multi) word/byte write suspend latency.

At this point, a Read Array command can be written to read data from locations other than that which is suspended. The only other valid commands while (multi) word/byte write is suspended are Read Status Register and (Multi) Word/Byte Write Resume. After (Multi) Word/Byte Write Resume command is written to the flash memory, the WSM will continue the (multi) word/byte write process. Status register bits SR.2 and SR.7 will automatically clear and STS will return to V_{OL}. After the (Multi) Word/Byte Write command is written, the device automatically outputs status register data when read (see Figure 11). V_{PP} must remain at $V_{PPH1/2/3}$ (the same V_{PP} level used for (multi) word/byte write) while in (multi) word/byte write suspend mode. WP# must also remain at V_{IH} or V_{IL}.

4.12 Set Block Lock-Bit Command

A flexible block locking and unlocking scheme is enabled via block lock-bits. The block lock-bits gate program and erase operations With WP#=V_{IH}, individual block lock-bits can be set using the Set Block Lock-Bit command. See Table 13 for a summary of hardware and software write protection options.

Set block lock-bit is executed by a two-cycle command sequence. The set block lock-bit setup along with appropriate block or device address is written followed by either the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set block lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read (see Figure 12). The CPU can detect the completion of the set block lock-bit event by analyzing the STS pin output or status register bit SR.7.

When the set block lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to "1". Also, reliable operations occur only when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. In the absence of this high voltage, block lock-bit contents are protected against alteration.

A successful set block lock-bit operation requires WP#=V_{IH}. If it is attempted with WP#=V_{IL}, SR.1 and SR.4 will be set to "1" and the operation will fail. Set block lock-bit operations with WP#<V_{IH} produce spurious results and should not be attempted.

4.13 Clear Block Lock-Bits Command

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. With WP#=V_{IH}, block lock-bits can be cleared using only the Clear Block Lock-Bits command. See Table 13 for a summary of hardware and software write protection options.

Clear block lock-bits operation is executed by a two-cycle command sequence. A clear block lock-bits setup is first written. After the command is written, the device automatically outputs status register data when read (see Figure 13). The CPU can detect completion of the clear block lock-bits event by analyzing the STS Pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to "1". Also, a reliable clear block lock-bits operation can only occur when $V_{CC}=V_{CC1/2}$ and $V_{PP}=V_{PPH1/2/3}$. If a clear block lock-bits operation is attempted while $V_{PP}\leq V_{PPLK}$, SR.3 and SR.5 will be set to "1". In the absence of this high voltage, the block lock-bits content are protected against alteration. A successful clear block lock-bits operation requires WP#=V_{IH}. If it is attempted with WP#=V_{IL}, SR.1 and SR.5 will be set to "1" and the operation will fail. Clear block lock-bits operations with V_{IH}<RP# produce spurious results and should not be attempted.

If a clear block lock-bits operation is aborted due to V_{PP} or V_{CC} transitioning out of valid range or RP# active transition, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

4.14 STS Configuration Command

The Status (STS) pin can be configured to different states using the STS Configuration command. Once the STS pin has been configured, it remains in that configuration until another configuration command is issued, the device is powered down or RP# is set to V_{IL}. Upon initial device power-up and after exit from deep power-down mode, the STS pin defaults to RY/BY# operation where STS low indicates that the WSM is busy. STS High Z indicates that the WSM is ready for a new operation.

To reconfigure the STS pin to other modes, the STS Configuration is issued followed by the appropriate configuration code. The three alternate configurations are all pulse mode for use as a system interrupt. The STS Configuration command functions independently of the V_{PP} voltage and RP# must be V_{IH}.

Table 12. STS Configuration Coding Description

Configuration Bits	Effects
00H	Set STS pin to default level mode (RY/BY#). RY/BY# in the default level-mode of operation will indicate WSM status condition.
01H	Set STS pin to pulsed output signal for specific erase operation. In this mode, STS provides low pulse at the completion of BLock Erase, Full Chip Erase and Clear Block Lock-bits operations.
02H	Set STS pin to pulsed output signal for a specific write operation. In this mode, STS provides low pulse at the completion of (Multi) Byte Write and Set Block Lock-bit operation.
03H	Set STS pin to pulsed output signal for specific write and erase operation. STS provides low pulse at the completion of Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-bit Configuration operations.

Table 13. Write Protection Alternatives

Operation	Block Lock-Bit	WP#	Effect
Block Erase, (Multi) Word/Byte Write	0	V_{IL} or V_{IH}	Block Erase and (Multi) Word/Byte Write Enabled
	1	V_{IL}	Block is Locked. Block Erase and (Multi) Word/Byte Write Disabled
		V_{IH}	Block Lock-Bit Override. Block Erase and (Multi) Word/Byte Write Enabled
Full Chip Erase	0,1	V_{IL}	All unlocked blocks are erased, locked blocks are not erased
	X	V_{IH}	All blocks are erased
Set Block Lock-Bit	X	V_{IL}	Set Block Lock-Bit Disabled
		V_{IH}	Set Block Lock-Bit Enabled
Clear Block Lock-Bits	X	V_{IL}	Clear Block Lock-Bits Disabled
		V_{IH}	Clear Block Lock-Bits Enabled

Table 14. Status Register Definition

WSMS	BESS	ECBLBS	WSBLBS	VPPS	WSS	DPS	R
7	6	5	4	3	2	1	0

SR.7 = WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = ERASE AND CLEAR BLOCK LOCK-BITS STATUS
1 = Error in Erase or Clear Blocl Lock-Bits
0 = Successful Erase or Clear Block Lock-Bits

SR.4 = WRITE AND SET BLOCK LOCK-BIT STATUS
1 = Error in Write or Set Block Lock-Bit
0 = Successful Write or Set Block Lock-Bit

SR.3 = V_{PP} STATUS
1 = V_{PP} Low Detect, Operation Abort
0 = V_{PP} OK

SR.2 = WRITE SUSPEND STATUS
1 = Write Suspended
0 = Write in Progress/Completed

SR.1 = DEVICE PROTECT STATUS
1 = Block Lock-Bit and/or WP# Lock Detected, Operation Abort
0 = Unlock

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

Check STS or SR.7 to determine block erase, full chip erase, (multi) word/byte write or block lock-bit configuration completion.
SR.6-0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (multi) word/byte write, block lock-bit configuration or STS configuration attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP} \neq V_{PPH1/2/3}$.

SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates block lock-bit, and WP# only after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set and/or WP# is not V_{IH}. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

Table 14.1. Extended Status Register Definition

SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

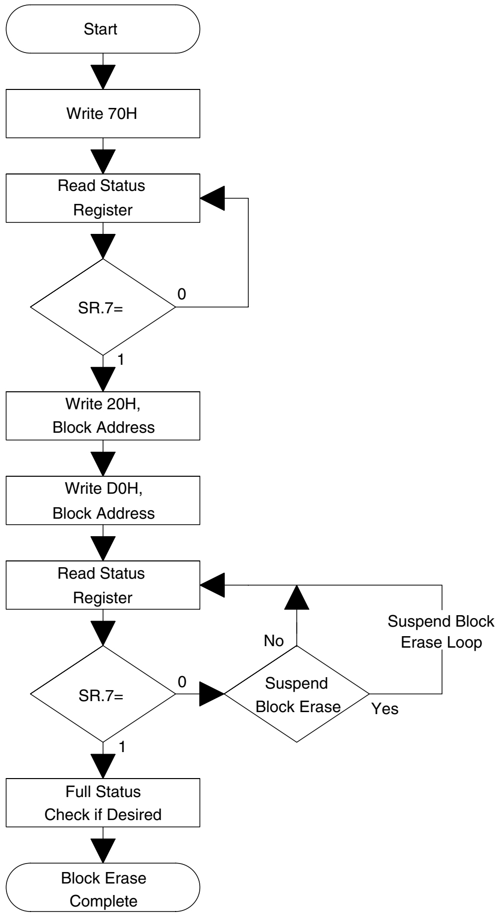
XSR.7 = STATE MACHINE STATUS
1 = Multi Word/Byte Write available
0 = Multi Word/Byte Write not available

XSR.6-0=RESERVED FOR FUTURE ENHANCEMENTS

NOTES:

After issue a Multi Word/Byte Write command: XSR.7 indicates that a next Multi Word/Byte Write command is available.

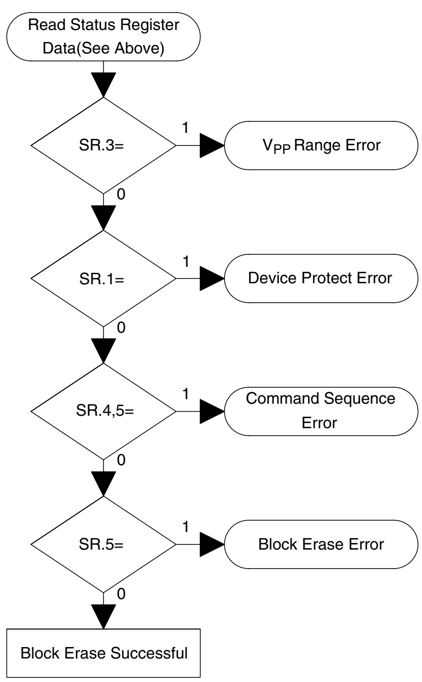
XSR.6-0 is reserved for future use and should be masked out when polling the extended status register.



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Erase Setup	Data=20H Addr=Within Block to be Erased
Write	Erase Confirm	Data=D0H Addr=Within Block to be Erased
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block erasures.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after the last operation to place device in read array mode.

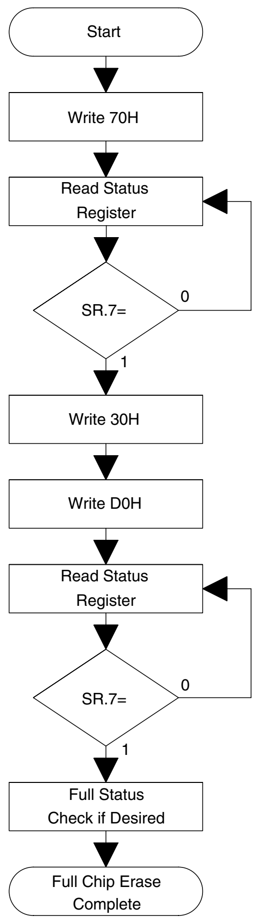
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL},Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

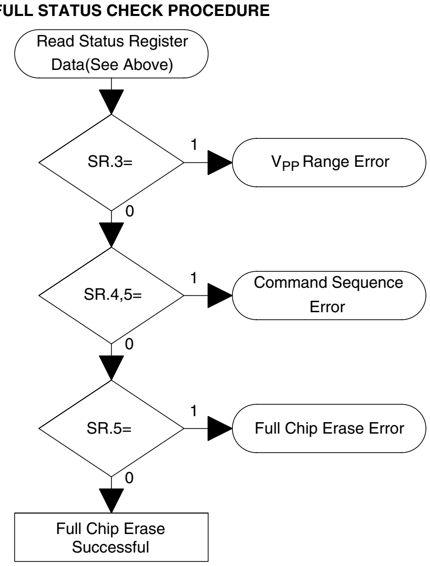
Figure 5. Automated Block Erase Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Full Chip Erase Setup	Data=30H Addr=X
Write	Full Chip Erase Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Full status check can be done after each full chip erase.
Write FFH after the last operation to place device in read array mode.

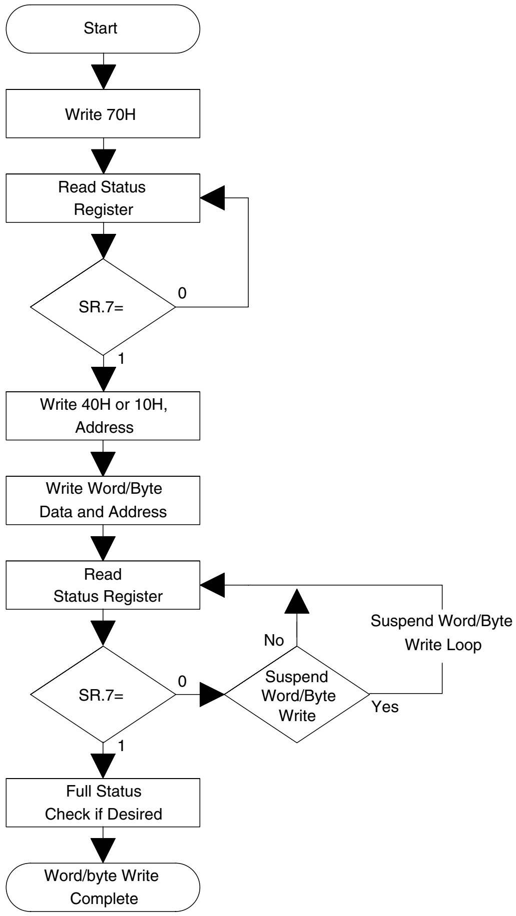
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error

SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

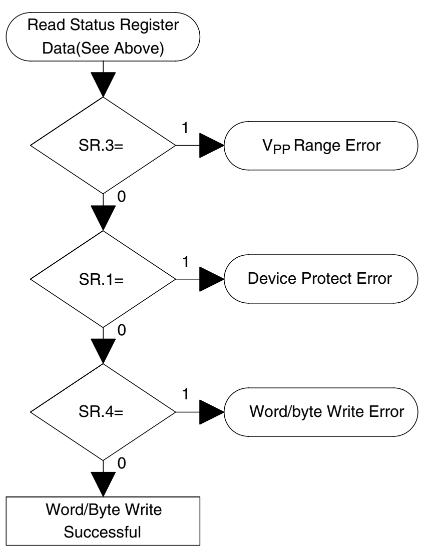
Figure 6. Automated Full Chip Erase Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write	Setup Word/Byte Write	Data=40H or 10H Addr=Location to Be Written
Write	Word/Byte Write	Data=Data to Be Written Addr=Location to Be Written
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent word/byte writes.
SR full status check can be done after each word/byte write, or after a sequence of word/byte writes.
Write FFH after the last word/byte write operation to place device in read array mode.

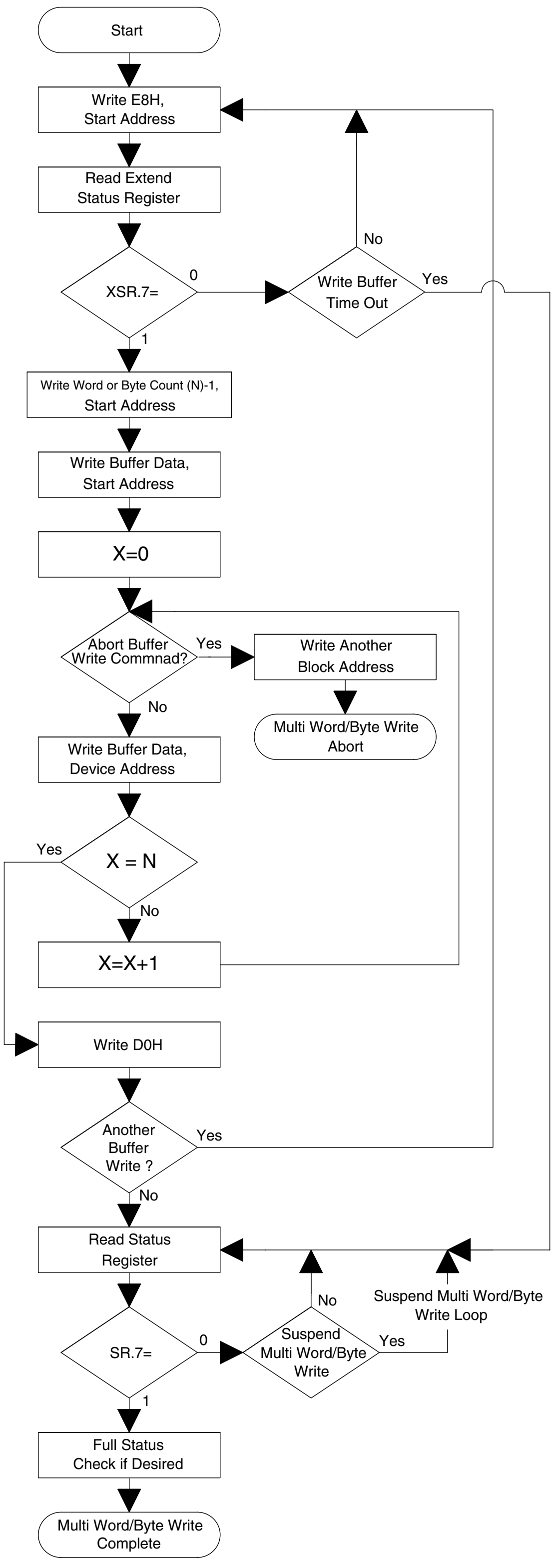
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL},Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4 1=Data Write Error

SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 7. Automated Word/byte Write Flowchart



Bus Operation	Command	Comments
Write	Setup Multi Word/Byte Write	Data=E8H Addr=Start Address
Read		Extended Status Register Data
Standby		Check XSR.7 1=Multi Word/Byte Write Ready 0=Multi Word/Byte Write Busy
Write (Note1)		Data=Word or Byte Count (N)-1 Addr=Start Address
Write (Note2,3)		Data=Buffer Data Addr=Start Address
Write (Note4,5)		Data=Buffer Data Addr=Device Address
Write		Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

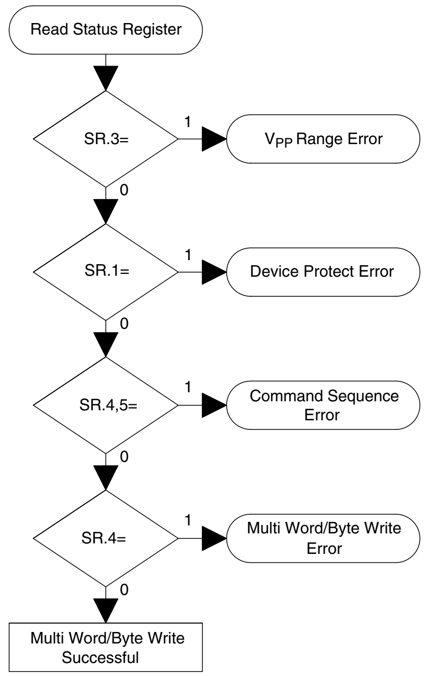
1. Byte or word count values on DQ_{0-7} are loaded into the count register.
2. Write Buffer contents will be programmed at the start address.
3. Align the start address on a Write Buffer boundary for maximum programming performance.
4. The device aborts the Multi Word/Byte Write command if the current address is outside of the original block address.
5. The Status Register indicates an "improper command sequence" if the Multi Word/Byte command is aborted. Follow this with a Clear Status Register command.

SR full status check can be done after each multi word/byte write, or after a sequence of multi word/byte writes.

Write FFH after the last multi word/byte write operation to place device in read array mode.

Figure 8. Automated Multi Word/Byte Write Flowchart

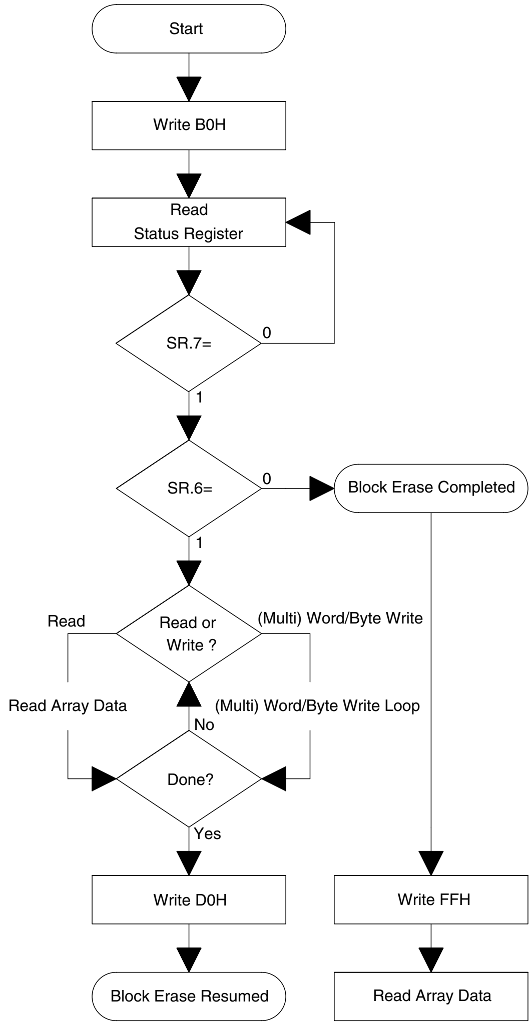
FULL STATUS CHECK PROCEDURE FOR MULTI WORD/BYTE WRITE OPERATION



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL},Block Lock-Bit is Set Only required for systems implementing lock-bit configuration
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Data Write Error

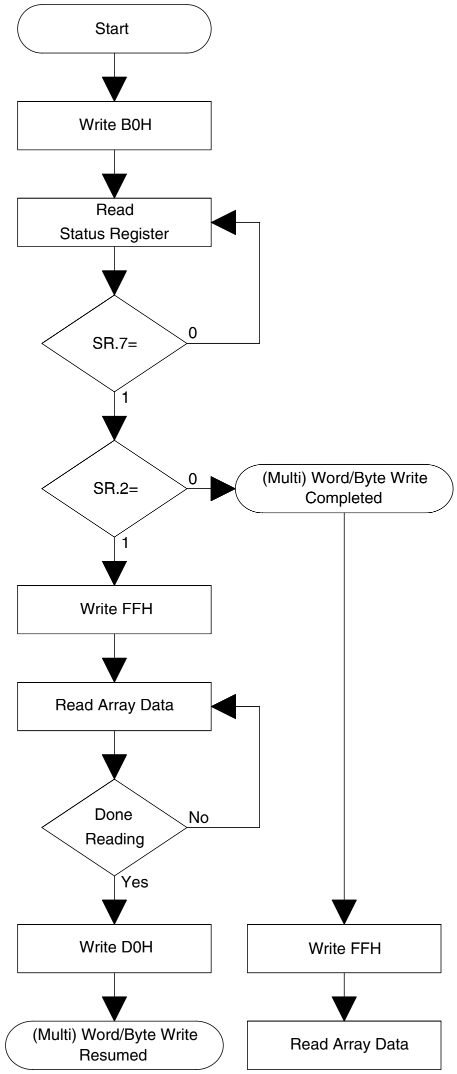
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are written before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 9. Full Status Check Procedure for Automated Multi Word/Byte Write



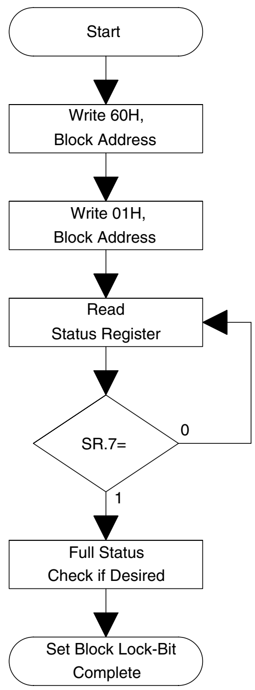
Bus Operation	Command	Comments
Write	Erase Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Erase Resume	Data=D0H Addr=X

Figure 10. Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	(Multi) Word/Byte Write Suspend	Data=B0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=(Multi) Word/Byte Write Suspended 0=(Multi) Word/Byte Write Completed
Write	Read Array	Data=FFH Addr=X
Read		Read Array locations other than that being written.
Write	(Multi) Word/Byte Write Resume	Data=D0H Addr=X

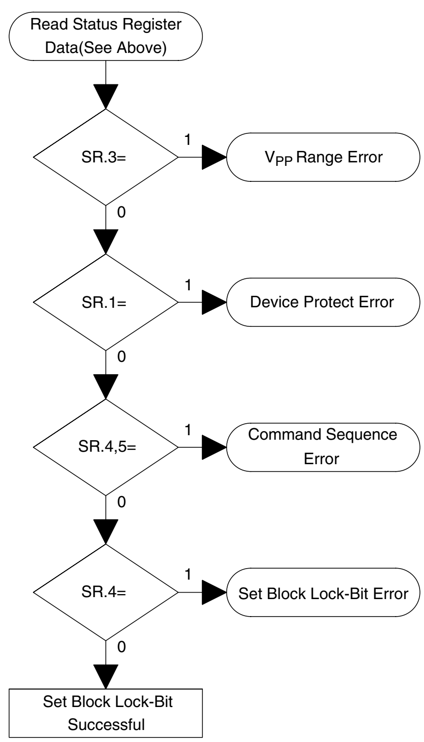
Figure 11. (Multi) Word/Byte Write Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Set Block Lock-Bit Setup	Data=60H Addr=Block Address
Write	Set Block Lock-Bit Confirm	Data=01H, Addr=Block Address
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Repeat for subsequent block lock-bit set operations.
Full status check can be done after each block lock-bit set operation or after a sequence of block lock-bit set operations.
Write FFH after the last block lock-bit set operation to place device in read array mode.

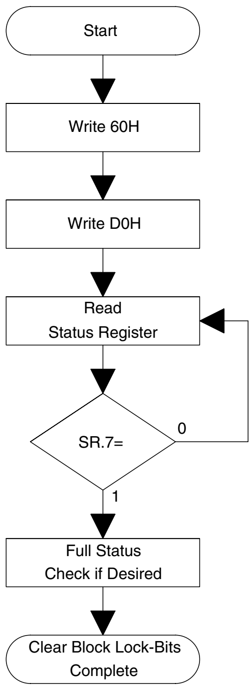
FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL}
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Set Block Lock-Bit Error

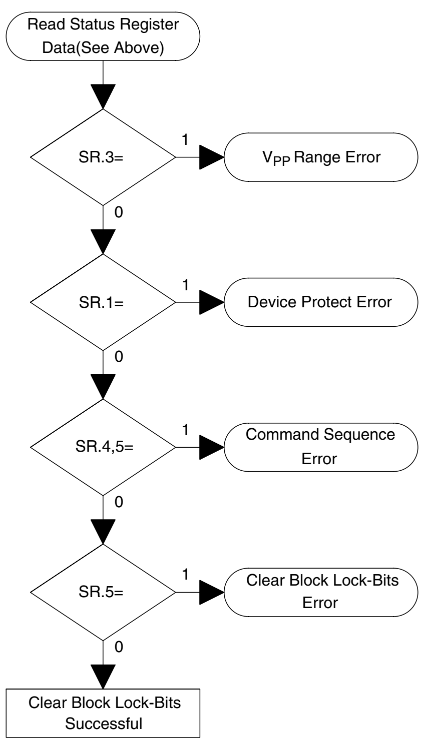
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple block lock-bits are set before full status is checked.
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 12. Set Block Lock-Bit Flowchart



Bus Operation	Command	Comments
Write	Clear Block Lock-Bits Setup	Data=60H Addr=X
Write	Clear Block Lock-Bits Confirm	Data=D0H Addr=X
Read		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Write FFH after the Clear Block Lock-Bits operation to place device in read array mode.		

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect WP#=V_{IL}
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Clear Block Lock-Bits Error
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command. If error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 13. Clear Block Lock-Bits Flowchart

5 DESIGN CONSIDERATIONS

5.1 Three-Line Output Control

The device will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-Line control provides for:

a. Lowest possible memory power dissipation.

b. Complete assurance that data bus contention will not occur.

To use these control inputs efficiently, an address decoder should enable CE# while OE# should be connected to all memory devices and the system's READ# control line. This assures that only selected memory devices have active outputs while deselected memory devices are in standby mode. RP# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should also toggle during system reset.

5.2 STS and Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Polling

STS is an open drain output that should be connected to V_{CC} by a pullup resistor to provide a hardware method of detecting block erase, full chip erase, (multi) word/byte write and block lock-bit configuration completion. In default mode, it transitions low after block erase, full chip erase, (multi) word/byte write or block lock-bit configuration commands and returns to V_{OH} when the WSM has finished executing the internal algorithm. For alternate STS pin configurations, see the Configuration command.

STS can be connected to an interrupt input of the system CPU or controller. It is active at all times. STS, in default mode, is also High-Z when the device is in block erase suspend (with (multi) word/byte write inactive), (multi) word/byte write suspend or deep power-down modes.

5.3 Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in three supply current issues; standby current levels, active current levels and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND and between its V_{PP} and GND. These high-frequency, low inductance capacitors should be placed as close as possible to package leads. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductance.

5.4 V_{PP} Trace on Printed Circuit Boards

Updating flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power supply trace. The V_{PP} pin supplies the memory cell current for block erase, full chip erase, (multi) word/byte write and block lock-bit configuration. Use similar trace widths and layout considerations given to the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

5.5 V_{CC}, V_{PP}, RP# Transitions

Block erase, full chip erase, (multi) word/byte write and block lock-bit configuration are not guaranteed if V_{PP} falls outside of a valid $V_{PPH1/2/3}$ range, V_{CC} falls outside of a valid $V_{CC1/2}$ range, or RP#=V_{IL}. If V_{PP} error is detected, status register bit SR.3 is set to "1" along with SR.4 or SR.5, depending on the attempted operation. If RP# transitions to V_{IL} during block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, STS(if set to RY/BY# mode) will remain low until the reset operation is complete. Then, the operation will abort and the device will enter deep power-down. The aborted operation may leave data partially altered. Therefore, the command sequence must be repeated after normal operation is restored. Device power-off or RP# transitions to V_{IL} clear the status register.

The CUI latches commands issued by system software and is not altered by V_{PP} or CE# transitions or WSM actions. Its state is read array mode upon power-up, after exit from deep power-down or after V_{CC} transitions below V_{LKO}.

After block erase, full chip erase, (multi) word/byte write or block lock-bit configuration, even after V_{PP} transitions down to V_{PPLK}, the CUI must be placed in read array mode via the Read Array command if subsequent access to the memory array is desired.

5.6 Power-Up/Down Protection

The device is designed to offer protection against accidental block and full chip erasure, (multi) word/byte writing or block lock-bit configuration during power transitions. Upon power-up, the device is indifferent as to which power supply (V_{PP} or V_{CC}) powers-up first. Internal circuitry resets the CUI to read array mode at power-up.

A system designer must guard against spurious writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The CUI's two-step command sequence architecture provides added level of protection against data alteration.

In-system block lock and unlock capability prevents inadvertent data alteration. The device is disabled while RP#=V_{IL} regardless of its control inputs state.

5.7 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash memory's nonvolatility increases usable battery life because data is retained when system power is removed.

In addition, deep power-down mode ensures extremely low power consumption even when system power is applied. For example, portable computing products and other power sensitive applications that use an array of devices for solid-state storage can consume negligible power by lowering RP# to V_{IL} standby or sleep modes. If access is again needed, the devices can be read following the t_{PHQV} and t_{PHWL} wake-up cycles required after RP# is first raised to V_{IH}. See AC Characteristics— Read Only and Write Operations and Figures 17, 18, 19, 20 for more information.

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Operating Temperature
During Read, Erase, Write and
Block Lock-Bit Configuration .....-40°C to +85°C(1)
Temperature under Bias............... -40°C to +85°C

Storage Temperature........................ -65°C to +125°C

Voltage On Any Pin
(except V_{CC}, V_{PP})............... -0.5V to V_{CC}+0.5V(2)

V_{CC} Suply Voltage ....-0.2V to +7.0V(2)

V_{PP} Update Voltage during
Erase, Write and
Block Lock-Bit Configuration ......-0.2V to +7.0V(2)

Output Short Circuit Current .... 100mA(3)

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on V_{CC} and V_{PP} pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC}+0.5V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

6.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Test Condition
T_A	Operating Temperature	-40	+85	°C	Ambient Temperature
V_{CC1}	V_{CC} Supply Voltage (2.7V-3.6V)	2.7	3.6	V	
V_{CC2}	V_{CC} Supply Voltage (3.3V±0.3V)	3.0	3.6	V	

6.2.1 CAPACITANCE(1)

T_A=+25°C, f=1MHz

Symbol	Parameter	Typ.	Max.	Unit	Condition
C_{IN}	Input Capacitance	7	10	pF	V_{IN}=0.0V
C_{OUT}	Output Capacitance	9	12	pF	V_{OUT}=0.0V

NOTE:
1. Sampled, not 100% tested.

6.2.2 AC INPUT/OUTPUT TEST CONDITIONS

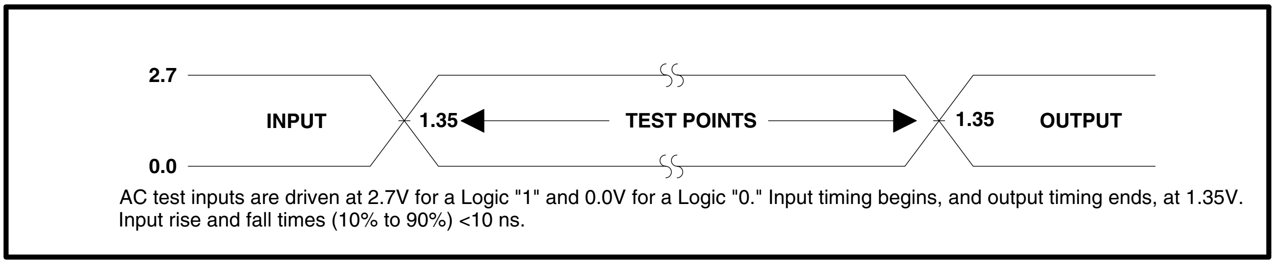


Figure 14. Transient Input/Output Reference Waveform for V_{CC}=2.7V-3.6V

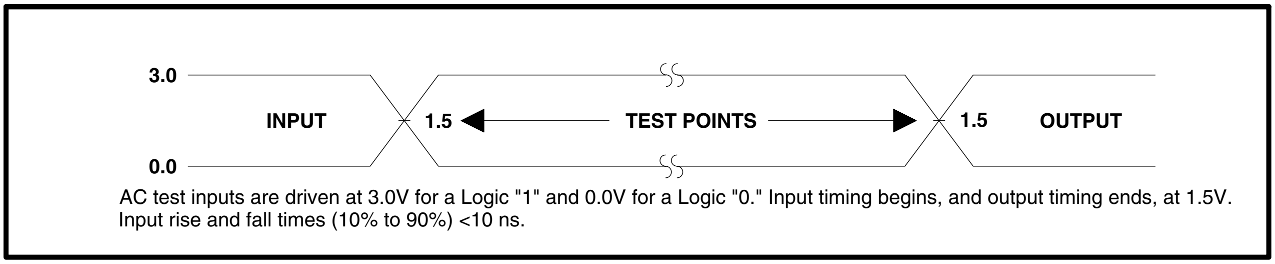


Figure 15. Transient Input/Output Reference Waveform for V_{CC}=3.3V±0.3V

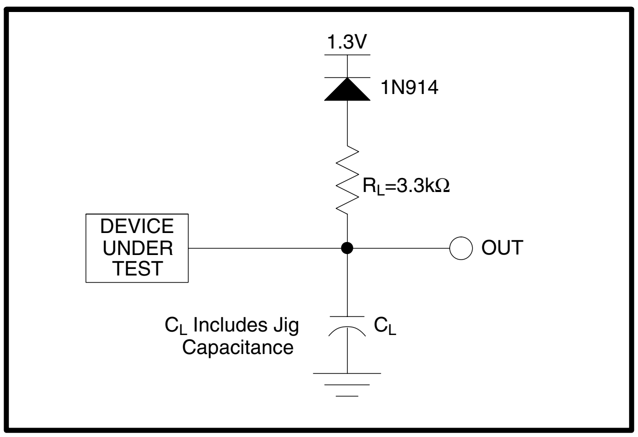


Figure 16. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L(pF)
V_{CC}=3.3V±0.3V, 2.7V-3.6V	50

6.2.3 DC CHARACTERISTICS

DC Characteristics

Sym.	Parameter	Notes	V_{CC}=2.7V Typ.	V_{CC}=2.7V Max.	V_{CC}=3.3V Typ.	V_{CC}=3.3V Max.	Unit	Test Conditions
I_{LI}	Input Load Current	1		±0.5		±0.5	µA	$V_{CC}=V_{CC}$Max. $V_{IN}=V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		±0.5		±0.5	µA	$V_{CC}=V_{CC}$Max. $V_{OUT}=V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1,3,6	20	100	20	100	µA	CMOS Inputs $V_{CC}=V_{CC}$Max. CE#=RP#=V_{CC}±0.2V
			1	4	1	4	mA	TTL Inputs $V_{CC}=V_{CC}$Max. CE#=RP#=V_{IH}
I_{CCD}	V_{CC} Deep Power-Down Current	1		25		25	µA	RP#=GND±0.2V I_{OUT}(STS)=0mA
I_{CCR}	V_{CC} Read Current	1,5,6		30		30	mA	CMOS Inputs $V_{CC}=V_{CC}$Max., CE#=GND f=5MHz, I_{OUT}=0mA
				35		35	mA	TTL Inputs $V_{CC}=V_{CC}$Max., CE#=V_{IL} f=5MHz, I_{OUT}=0mA
I_{CCW}	V_{CC} Write Current ((Multi) W/B Write or Set Block Lock Bit)	1,7		17	—	—	mA	V_{PP}=2.7V-3.6V
				17		17	mA	V_{PP}=3.3V±0.3V
				17		17	mA	V_{PP}=5.0V±0.5V
I_{CCE}	V_{CC} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits)	1,7		17	—	—	mA	V_{PP}=2.7V-3.6V
				17		17	mA	V_{PP}=3.3V±0.3V
				17		17	mA	V_{PP}=5.0V±0.5V
I_{CCWS} I_{CCES}	V_{CC} Write or Block Erase Suspend Current	1,2	1	6	1	6	mA	CE#=V_{IH}
I_{PPS}	V_{PP} Standby Current	1	±2	±15	±2	±15	µA	$V_{PP} \leq V_{CC}$
I_{PPR}	V_{PP} Read Current	1	10	200	10	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current	1	0.1	5	0.1	5	µA	RP#=GND±0.2V
I_{PPW}	V_{PP} Write Current ((Multi) W/B Write or Set Block Lock Bit)	1,7		80	—	—	mA	V_{PP}=2.7V-3.6V
				80		80	mA	V_{PP}=3.3V±0.3V
				80		80	mA	V_{PP}=5.0V±0.5V
I_{PPE}	V_{PP} Erase Current (Block Erase, Full Chip Erase, Clear Block Lock Bits)	1,7		40	—	—	mA	V_{PP}=2.7V-3.6V
				40		40	mA	V_{PP}=3.3V±0.3V
				40		40	mA	V_{PP}=5.0V±0.5V
I_{PPWS} I_{PPES}	V_{PP} Write or Block Erase Suspend Current	1	10	200	10	200	µA	$V_{PP}=V_{PPH1/2/3}$

DC Characteristics (Continued)

Sym.	Parameter	Notes	V_{CC}=2.7V Min.	V_{CC}=2.7V Max.	V_{CC}=3.3V Min.	V_{CC}=3.3V Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	7	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input High Voltage	7	2.0	V_{CC} +0.5	2.0	V_{CC} +0.5	V	
V_{OL}	Output Low Voltage	3,7		0.4		0.4	V	V_{CC}=V_{CC}Min. I_{OL}=2mA
V_{OH1}	Output High Voltage (TTL)	3,7	2.4		2.4		V	V_{CC}=V_{CC}Min. I_{OH}=-2.5mA
V_{OH2}	Output High Voltage (CMOS)	3,7	0.85 V_{CC}		0.85 V_{CC}		V	V_{CC}=V_{CC}Min. I_{OH}=-2.5mA
			V_{CC} -0.4		V_{CC} -0.4		V	V_{CC}=V_{CC}Min. I_{OH}=-100μA
V_{PPLK}	V_{PP} Lockout Voltage during Normal Operations	4,7		1.5		1.5	V	
V_{PPH1}	V_{PP} Voltage during Write or Erase Operations		2.7	3.6	—	—	V	
V_{PPH2}	V_{PP} Voltage during Write or Erase Operations		3.0	3.6	3.0	3.6	V	
V_{PPH3}	V_{PP} Voltage during Write or Erase Operations		4.5	5.5	4.5	5.5	V	
V_{LKO}	V_{CC} Lockout Voltage		2.0		2.0		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C.These currents are valid for all product versions (packages and speeds).
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or byte written while in erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
3. Includes STS.
4. Block erases, full chip erases, (multi) word/byte writes and block lock-bit configurations are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between V_{PPLK}(max.) and V_{PPH1}(min.), between V_{PPH1}(max.) and V_{PPH2}(min.), between V_{PPH2}(max.) and V_{PPH3}(min.) and above V_{PPH3}(max.).
5. Automatic Power Savings (APS) reduces typical I_{CCR} to 3mA at 2.7V and 3.3V V_{CC} in static operation.
6. CMOS inputs are either V_{CC}±0.2V or GND±0.2V. TTL inputs are either V_{IL} or V_{IH}.
7. Sampled, not 100% tested.

6.2.4 AC CHARACTERISTICS - READ-ONLY OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

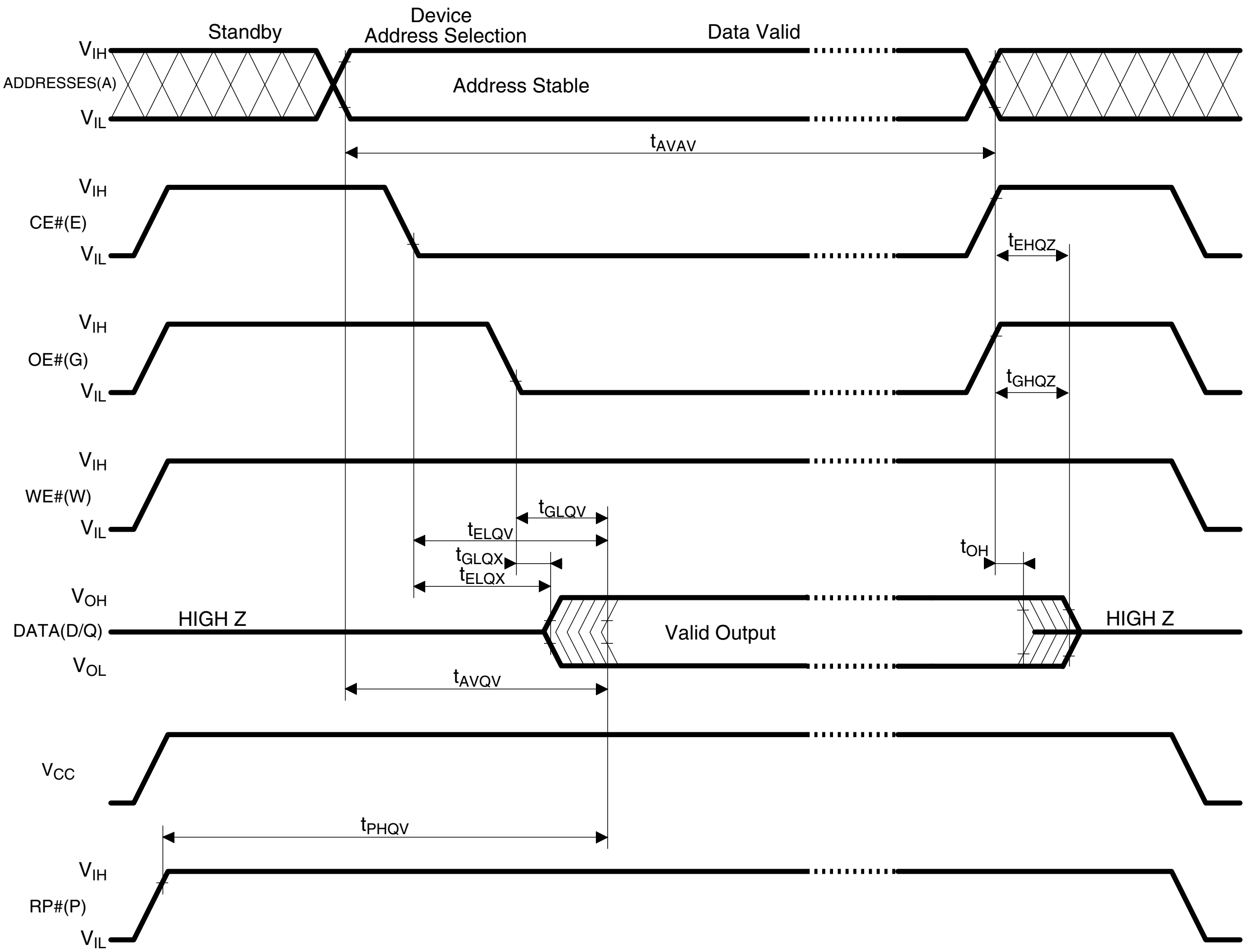
Versions(4)			LH28F320S3H-L140		Unit
Sym.	Parameter	Notes	Min.	Max.	
t_{AVAV}	Read Cycle Time		140		ns
t_{AVQV}	Address to Output Delay			140	ns
t_{ELQV}	CE# to Output Delay	2		140	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		50	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		140	ns
t_{FLQZ}	BYTE# to Output in High Z	3		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5	ns

NOTE:
See 3.3V V_{CC} Read-Only Operations for notes 1 through 4.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

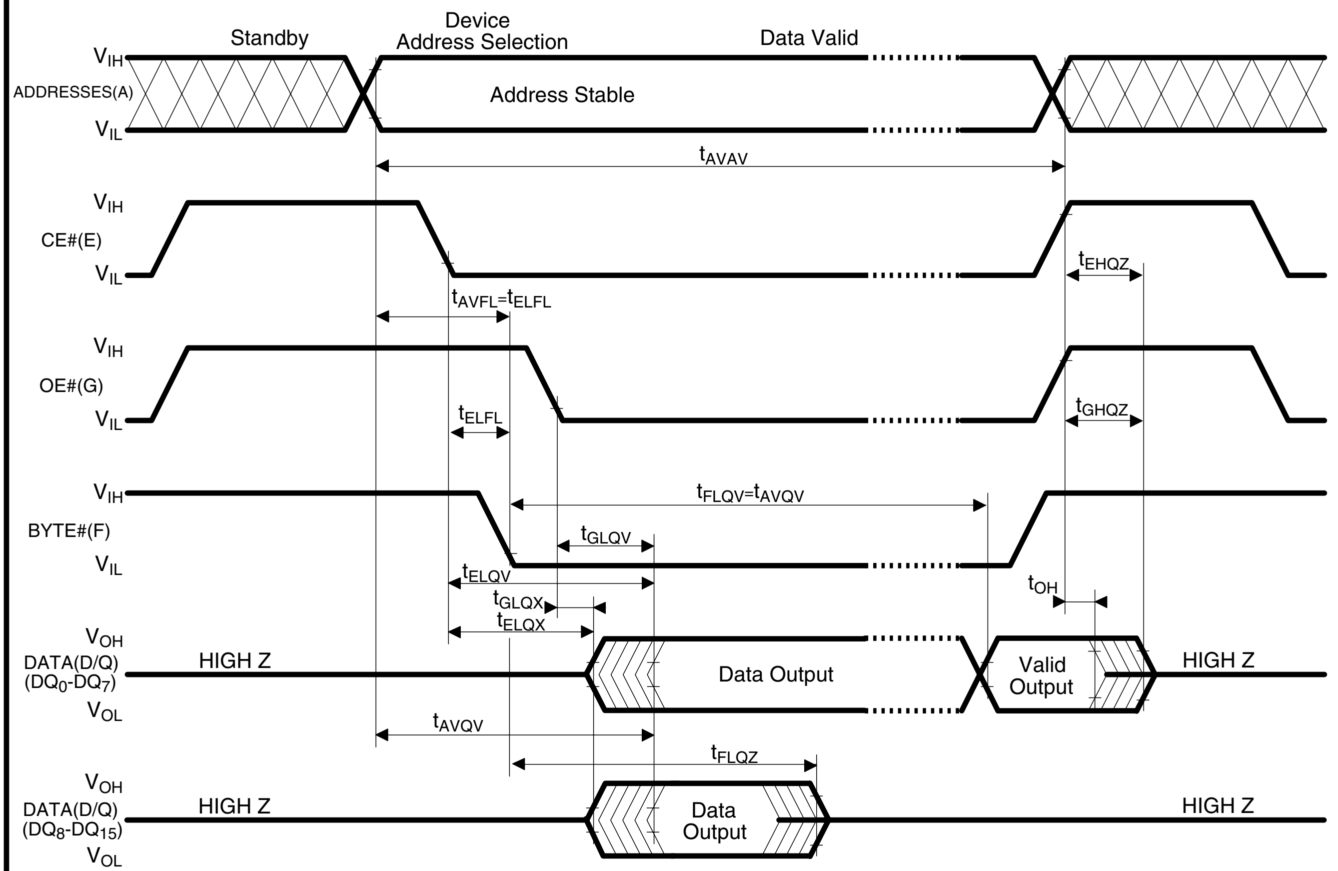
Versions(4)			LH28F320S3H-L110		Unit
Sym.	Parameter	Notes	Min.	Max.	
t_{AVAV}	Read Cycle Time		110		ns
t_{AVQV}	Address to Output Delay			110	ns
t_{ELQV}	CE# to Output Delay	2		110	ns
t_{PHQV}	RP# High to Output Delay			600	ns
t_{GLQV}	OE# to Output Delay	2		45	ns
t_{ELQX}	CE# to Output in Low Z	3	0		ns
t_{EHQZ}	CE# High to Output in High Z	3		50	ns
t_{GLQX}	OE# to Output in Low Z	3	0		ns
t_{GHQZ}	OE# High to Output in High Z	3		20	ns
t_{OH}	Output Hold from Address, CE# or OE# Change, Whichever Occurs First	3	0		ns
t_{FLQV} t_{FHQV}	BYTE# to Output Delay	3		110	ns
t_{FLQZ}	BYTE# to Output in High Z	3		30	ns
t_{ELFL} t_{ELFH}	CE# Low to BYTE# High or Low	3		5	ns

NOTES:
1. See AC Input/Output Reference Waveform for maximum allowable input slew rate.
2. OE# may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. See Ordering Information for device speeds (valid operational combinations).



NOTE: CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 17. AC Waveform for Read Operations



NOTE: CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 18. BYTE# Timing Waveforms

6.2.5 AC CHARACTERISTICS - WRITE OPERATIONS(1)

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

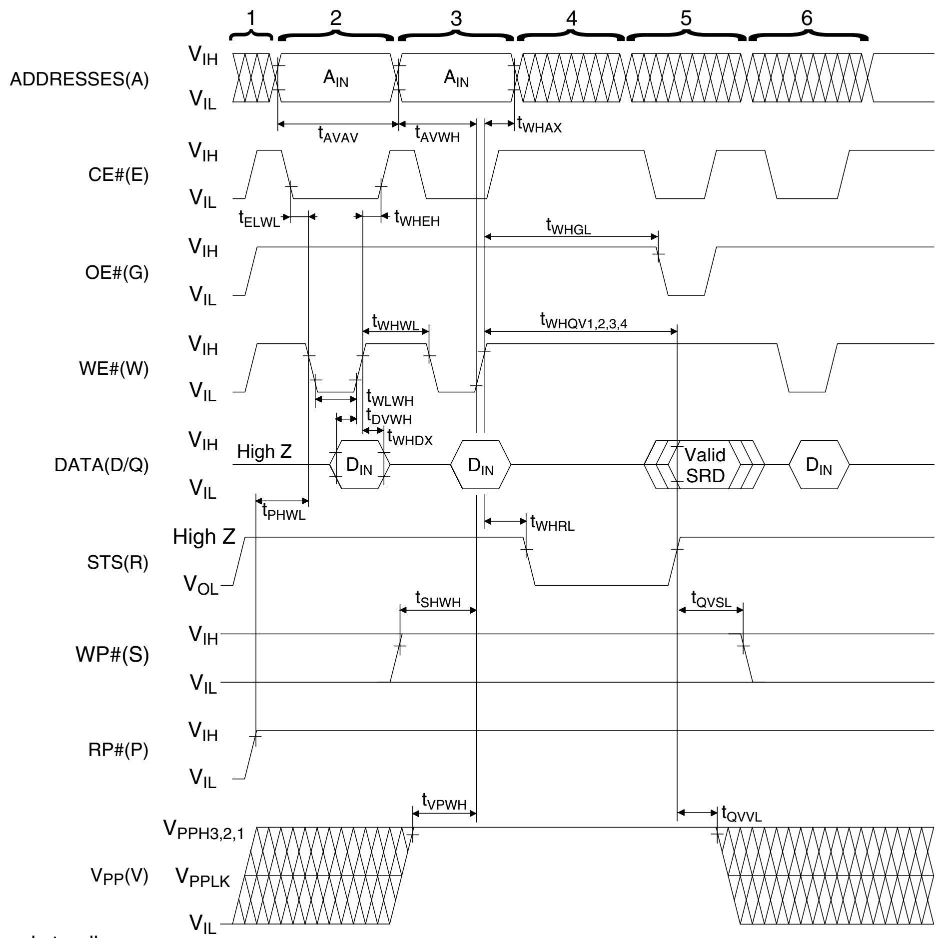
Versions(5)			LH28F320S3H-L140		Unit
Sym.	Parameter	Notes	Min.	Max.	
t_{AVAV}	Write Cycle Time		140		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		55		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		5		ns
t_{WHAX}	Address Hold from WE# High		5		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to STS Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		ns

NOTE:
See 3.3V V_{CC} WE#-Controlled Writes for notes 1 through 5.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Versions(5)			LH28F320S3H-L110		Unit
Sym.	Parameter	Notes	Min.	Max.	
t_{AVAV}	Write Cycle Time		110		ns
t_{PHWL}	RP# High Recovery to WE# Going Low	2	1		µs
t_{ELWL}	CE# Setup to WE# Going Low		10		ns
t_{WLWH}	WE# Pulse Width		55		ns
t_{SHWH}	WP# V_{IH} Setup to WE# Going High	2	100		ns
t_{VPWH}	V_{PP} Setup to WE# Going High	2	100		ns
t_{AVWH}	Address Setup to WE# Going High	3	50		ns
t_{DVWH}	Data Setup to WE# Going High	3	50		ns
t_{WHDX}	Data Hold from WE# High		5		ns
t_{WHAX}	Address Hold from WE# High		5		ns
t_{WHEH}	CE# Hold from WE# High		10		ns
t_{WHWL}	WE# Pulse Width High		30		ns
t_{WHRL}	WE# High to STS Going Low			100	ns
t_{WHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		ns

NOTES:
1. Read timing characteristics during block erase, full chip erase, (multi) wrod/byte write and block lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).



NOTES:
1. V_{CC} power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.
7. CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 19. AC Waveform for WE#-Controlled Write Operations

6.2.6 ALTERNATIVE CE#-CONTROLLED WRITES[1]

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

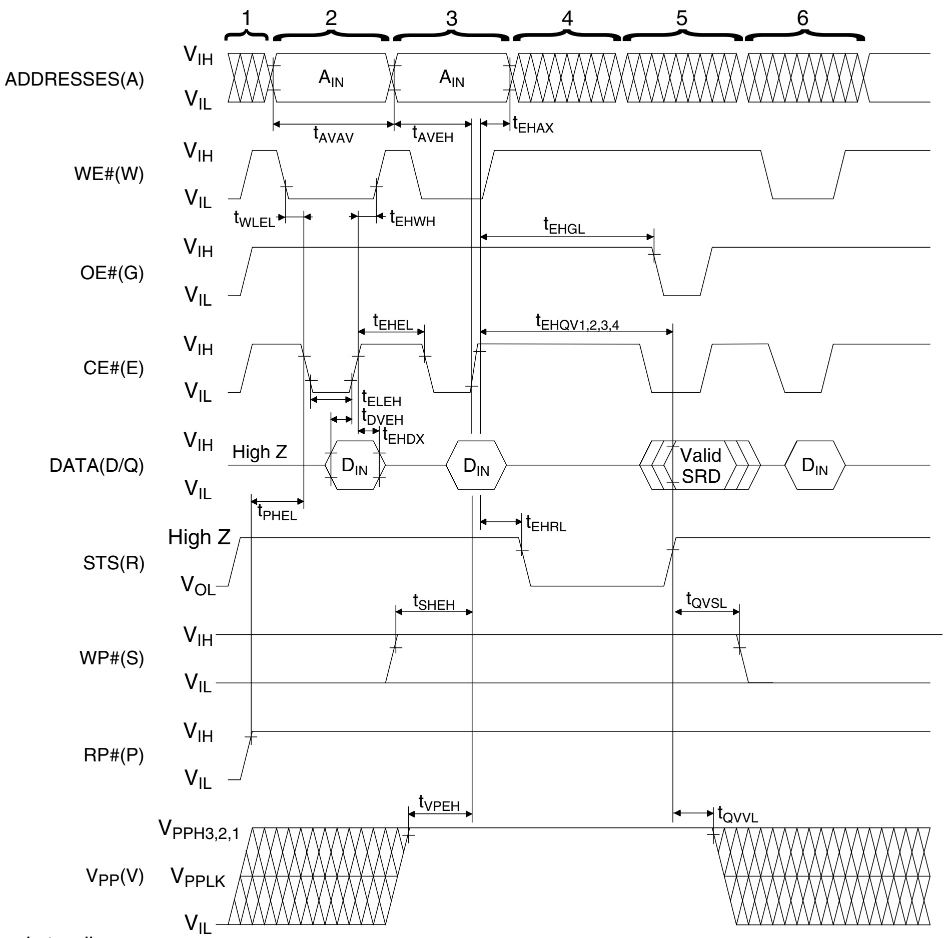
Versions[5]			LH28F320S3H-L140		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		140		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		5		ns
t_{EHAX}	Address Hold from CE# High		5		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to STS Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		ns

NOTE:
See 3.3V V_{CC} Alternative CE#-Controlled Writes for notes 1 through 5.

V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Versions[5]			LH28F320S3H-L110		
Sym.	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		110		ns
t_{PHEL}	RP# High Recovery to CE# Going Low	2	1		µs
t_{WLEL}	WE# Setup to CE# Going Low		0		ns
t_{ELEH}	CE# Pulse Width		70		ns
t_{SHEH}	WP# V_{IH} Setup to CE# Going High	2	100		ns
t_{VPEH}	V_{PP} Setup to CE# Going High	2	100		ns
t_{AVEH}	Address Setup to CE# Going High	3	50		ns
t_{DVEH}	Data Setup to CE# Going High	3	50		ns
t_{EHDX}	Data Hold from CE# High		5		ns
t_{EHAX}	Address Hold from CE# High		5		ns
t_{EHWH}	WE# Hold from CE# High		0		ns
t_{EHEL}	CE# Pulse Width High		25		ns
t_{EHRL}	CE# High to STS Going Low			100	ns
t_{EHGL}	Write Recovery before Read		0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, STS High Z	2,4	0		ns
t_{QVSL}	WP# V_{IH} Hold from Valid SRD, STS High Z	2,4	0		ns

NOTES:
1. In systems where CE# defines the write pulse width (within a longer WE# timing waveform), all setup, hold and inactive WE# times should be measured relative to the CE# waveform.
2. Sampled, not 100% tested.
3. Refer to Table 4 for valid A_{IN} and D_{IN} for block erase, full chip erase, (multi) word/byte write or block lock-bit configuration.
4. V_{PP} should be held at $V_{PPH1/2/3}$ until determination of block erase, full chip erase, (multi) word/byte write or block lock-bit configuration success (SR.1/3/4/5=0).
5. See Ordering Information for device speeds (valid operational combinations).



NOTES:
1. V_{CC} power-up and standby.
2. Write erase or write setup.
3. Write erase confirm or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. Write Read Array command.
7. CE# is defined as the latter of CE_0# and CE_1# going Low or the first of CE_0# or CE_1# going High.

Figure 20. AC Waveform for CE#-Controlled Write Operations

6.2.7 RESET OPERATIONS

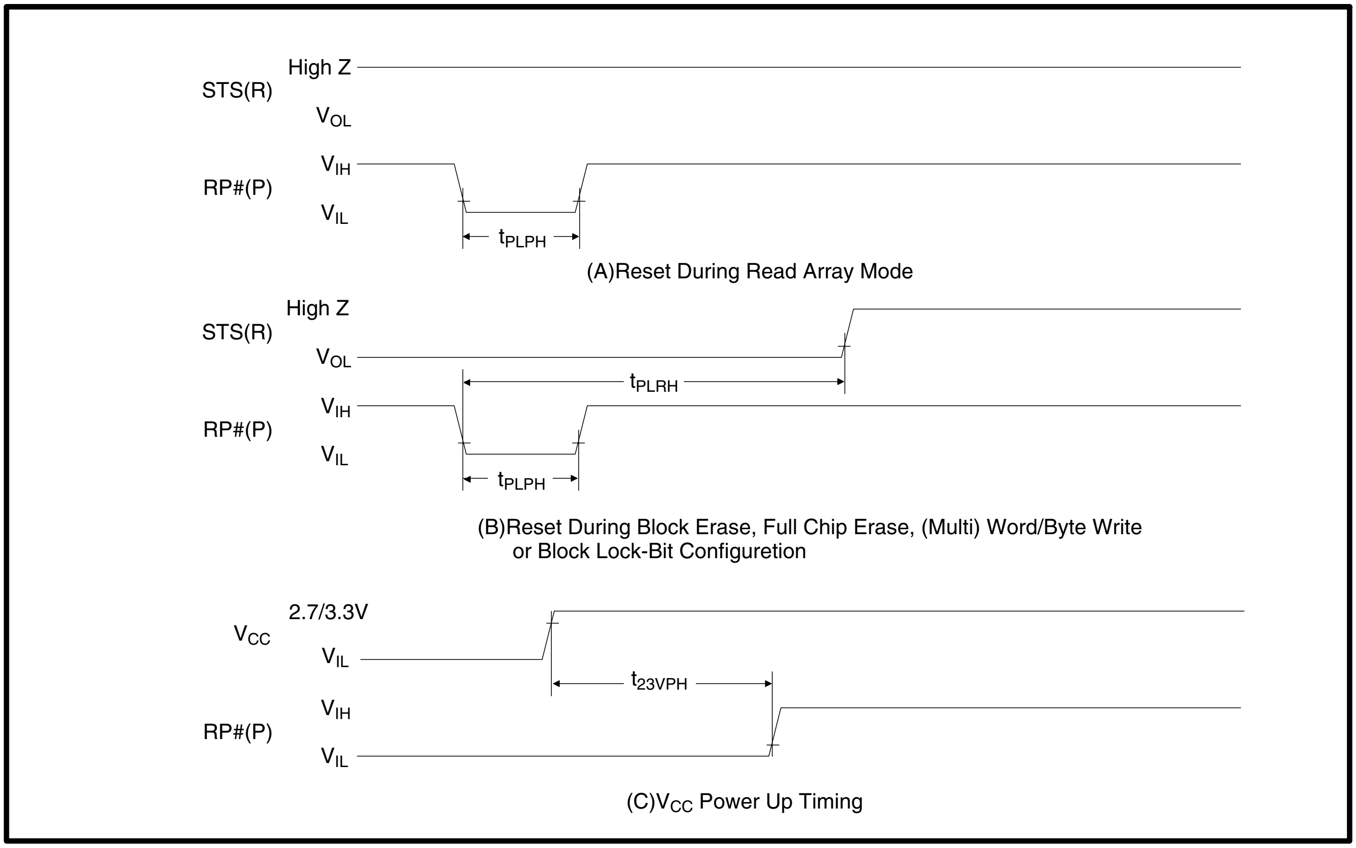


Figure 21. AC Waveform for Reset Operation

Reset AC Specifications(1)

Symbol	Parameter	Notes	V_{CC}=2.7V		V_{CC}=3.3V		Unit
			Min.	Max.	Min.	Max.	
t_{PLPH}	RP# Pulse Low Time (If RP# is tied to V_{CC}, this specification is not applicable)		100		100		ns
t_{PLRH}	RP# Low to Reset during Block Erase, Full Chip Erase, (Multi) Word/Byte Write or Block Lock-Bit Configuration	2,3		21.5		21.1	µs
t_{23VPH}	V_{CC} at 2.7V to RP# High V_{CC} at 3.0V to RP# High	4	100		100		ns

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase, full chip erase, (multi) word/byte write or block lock-bit configuration operation is not executing, the reset will complete within 100ns.
3. A reset time, t_{PHQV}, is required from the latter of STS going High Z or RP# going high until outputs are valid.
4. When the device power-up, holding RP# low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

6.2.8 BLOCK ERASE, FULL CHIP ERASE, (MULTI) WORD/BYTE WRITE AND BLOCK LOCK-BIT CONFIGURATION PERFORMANCE[3,4]

V_{CC}=2.7V-3.6V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	V_{PP}=2.7V-3.6V Typ.[1]	V_{PP}=2.7V-3.6V Max.	V_{PP}=3.0V-3.6V Typ.[1]	V_{PP}=3.0V-3.6V Max.	V_{PP}=4.5V-5.5V Typ.[1]	V_{PP}=4.5V-5.5V Max.	Unit
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in word mode)	2	22.19	250	22.19	250	13.2	180	µs
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in byte mode)	2	19.9	250	19.9	250	13.2	180	µs
	Word/Byte Write Time (using multi word/byte write)	2	5.76	250	5.76	250	2.76	180	µs
	Block Write Time (using W/B write, in word mode)	2	0.73	8.2	0.73	8.2	0.44	4.8	s
	Block Write Time (using W/B write, in byte mode)	2	1.31	16.5	1.31	16.5	0.87	10.9	s
	Block Write Time (using multi word/byte write)	2	0.37	4.1	0.37	4.1	0.18	2	s
t_{WHQV2} t_{EHQV2}	Block Erase Time	2	0.56	10	0.56	10	0.42	10	s
	Full Chip Erase Time		35.9	640	35.9	640	26.9	640	s
t_{WHQV3} t_{EHQV3}	Set Block Lock-Bit Time	2	22.17	250	22.17	250	13.2	180	µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2	0.56	10	0.56	10	0.42	10	s
t_{WHRH1} t_{EHRH1}	Write Suspend Latency Time to Read		7.24	10.2	7.24	10.2	6.73	9.48	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read		15.5	21.5	15.5	21.5	12.54	17.54	µs

NOTE:

See 3.3V V_{CC} Block Erase, Full Chip Erase, (Multi) Word/Byte Write and Block Lock-Bit Configuration Performance for notes 1 through 4.

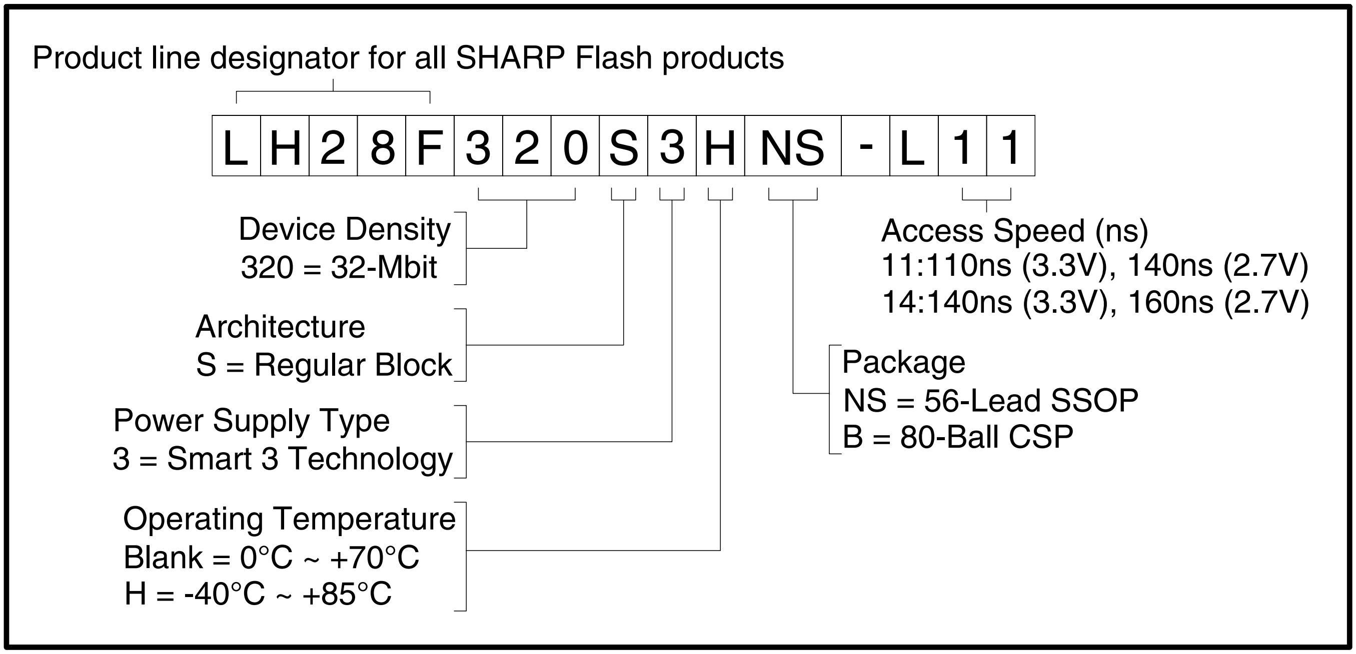
V_{CC}=3.3V±0.3V, T_A=-40°C to +85°C

Sym.	Parameter	Notes	V_{PP}=3.0V-3.6V		V_{PP}=4.5V-5.5V		Unit
			Typ.(1)	Max.	Typ.(1)	Max.	
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in word mode)	2	21.75	250	12.95	180	µs
t_{WHQV1} t_{EHQV1}	Word/Byte Write Time (using W/B write, in byte mode)	2	19.51	250	12.95	180	µs
	Word/Byte Write Time (using multi word/byte write)	2	5.66	250	2.7	180	µs
	Block Write Time (using W/B write, in word mode)	2	0.72	8.2	0.43	4.8	s
	Block Write Time (using W/B write, in byte mode)	2	1.28	16.5	0.85	10.9	s
	Block Write Time (using multi word/byte write)	2	0.36	4.1	0.18	2	s
t_{WHQV2} t_{EHQV2}	Block Erase Time	2	0.55	10	0.41	10	s
	Full Chip Erase Time		35.2	640	26.3	640	s
t_{WHQV3} t_{EHQV3}	Set Block Lock-Bit Time	2	21.75	250	12.95	180	µs
t_{WHQV4} t_{EHQV4}	Clear Block Lock-Bits Time	2	0.55	10	0.41	10	s
t_{WHRH1} t_{EHRH1}	Write Suspend Latency Time to Read		7.1	10	6.6	9.3	µs
t_{WHRH2} t_{EHRH2}	Erase Suspend Latency Time to Read		15.2	21.1	12.3	17.2	µs

NOTES:
1. Typical values measured at T_A=+25°C and nominal voltages. Assumes corresponding block lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.

7 ADDITIONAL INFORMATION

7.1 Ordering Information



Option	Order Code	Valid Operational Combinations	
		V_{CC}=2.7V-3.6V 50pF load, 1.35V I/O Levels	V_{CC}=3.3V±0.3V 50pF load, 1.5V I/O Levels
1	LH28F320S3HNS-L11	LH28F320S3H-L140	LH28F320S3H-L110

8 Package and packing specification

1. Package Outline Specification
   Refer to drawing No.AA2021

2. Markings
   2−1. Marking contents
   (1) Product name : LH28F320S3HNS−L11
   (2) Company name : SHARP
   (3) Date code
   (Example) YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.
   ××× → Denotes the production ref.code (1∼3)
   WW → Denotes the production week. (01,02,03, · · · · · 52,53)
   YY → Denotes the production year. (Lower two digits of the year.)
   (4) The marking of "JAPAN" indicates the country of origin.
   2−2. Marking layout
   Refer to drawing No.AA2021
   (This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)
   Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).
   When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package.
   This dry packing is designed to prevent the above problem from occurring in surface mount packages.
   3−1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (50devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (500devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

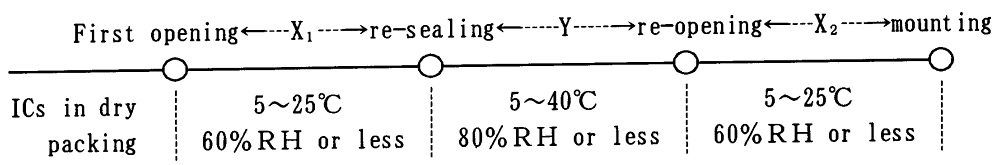
3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 3 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 3 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 3 days, and store the ICs in the same environment as section 4-3.(1).



X_1+X_2	: within 3 days
Y	: within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃.
Heat resistance tray is used for shipping tray.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

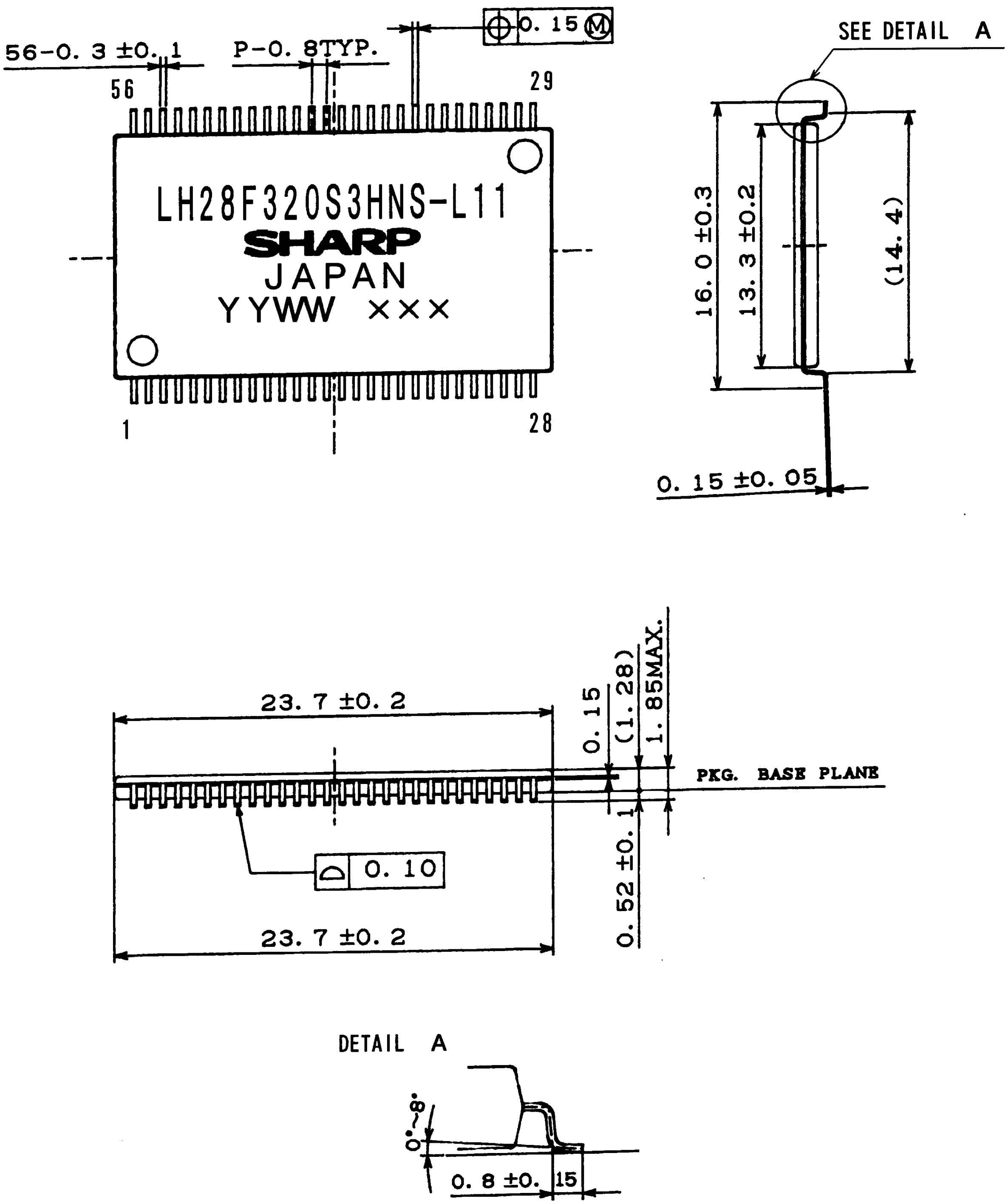
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

5−1. Soldering conditions (The following conditions are valid only for one time soldering.)

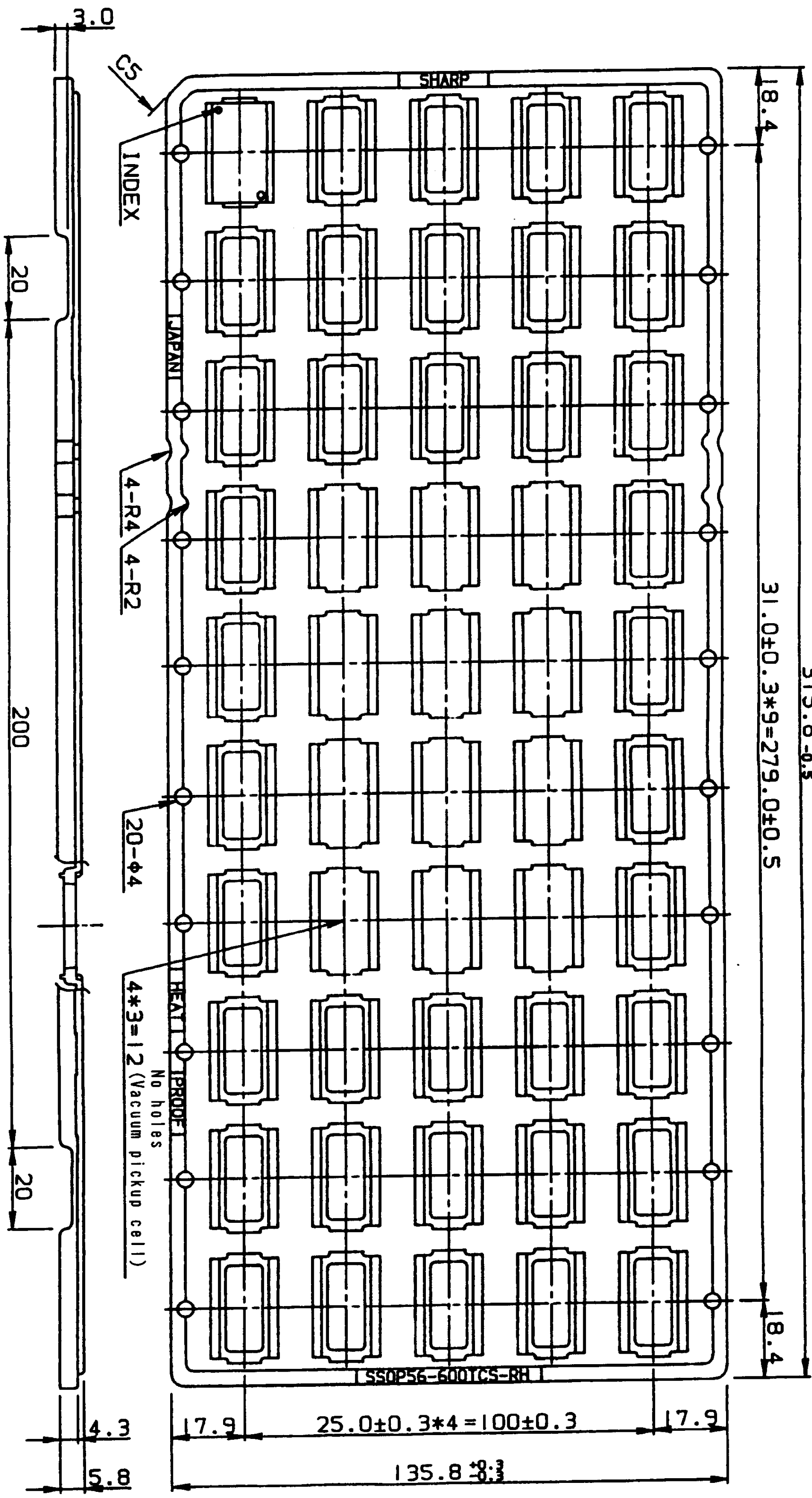
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃ or less, duration of less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC package surface
Manual soldering (soldering iron)	260℃ or less, duration of less than 10 seconds	IC outer lead surface

5−2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃



名称 NAME	SSOP56-P-600	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE	プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA2021	単位 UNIT	mm		

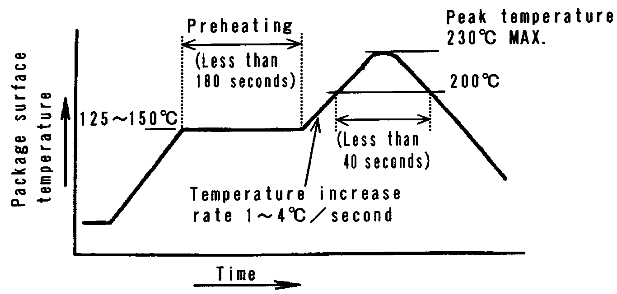


名称 NAME	SSOP56−600TCS−RH			備考 NOTE
DRAWING NO.	CV795	単位 UNIT	mm	

《Supplementary data》

LHF32K03 Recommended mounting conditions for two time reflow soldering .	
Product name(Package)	LH28F320S3HNS-L11 (SSOP56-P-600)
Packing specification	Tray (Dry packing)
Mounting method	Reflow soldering (Air)
Reflow soldering conditions	Peak temperature of 230℃ or less. 200℃ or over, duration of less than 40 seconds. Preheat temperature of 125~150℃, duration of less than 180 seconds. Temperature increase rate of 1~4℃/second.
Measurement point	IC package surface
Storage conditions	After opening the dry packing, store the ICs in an environment with a temperature of 5~25℃ and a relative humidity of 60% or less. If doing reflow soldering twice, do the first reflow soldering within 72 hours after opening dry packing and do the second reflow soldering within 72 hours after the first reflow soldering.
Note	If the above storage conditions are not applicable, bake it before reflow soldering. The recommended conditions are 16~24 hours at 120℃. (Heat resistance tray is used for shipping tray.)

Recommended Reflow Soldering(Air) Temperature Profile



Flash memory LHFXXKXX family Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems.
Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands, causing undesired memory updating.
To protect the data stored in the flash memory against unwanted overwriting, systems operating with the flash memory should have the following write protect designs, as appropriate:

1) Protecting data in specific block
Setting the lock bit of the desired block and pulling WP# low disables the writing operation on that block. By using this feature, the flash memory space can be divided into, for example, the program section(locked section) and data section(unlocked section).
By controlling WP#, desired blocks can be locked/unlocked through the software.
For further information on setting/resetting block bit, refer to the specification. (See chapter 4.12 and 4.13.)

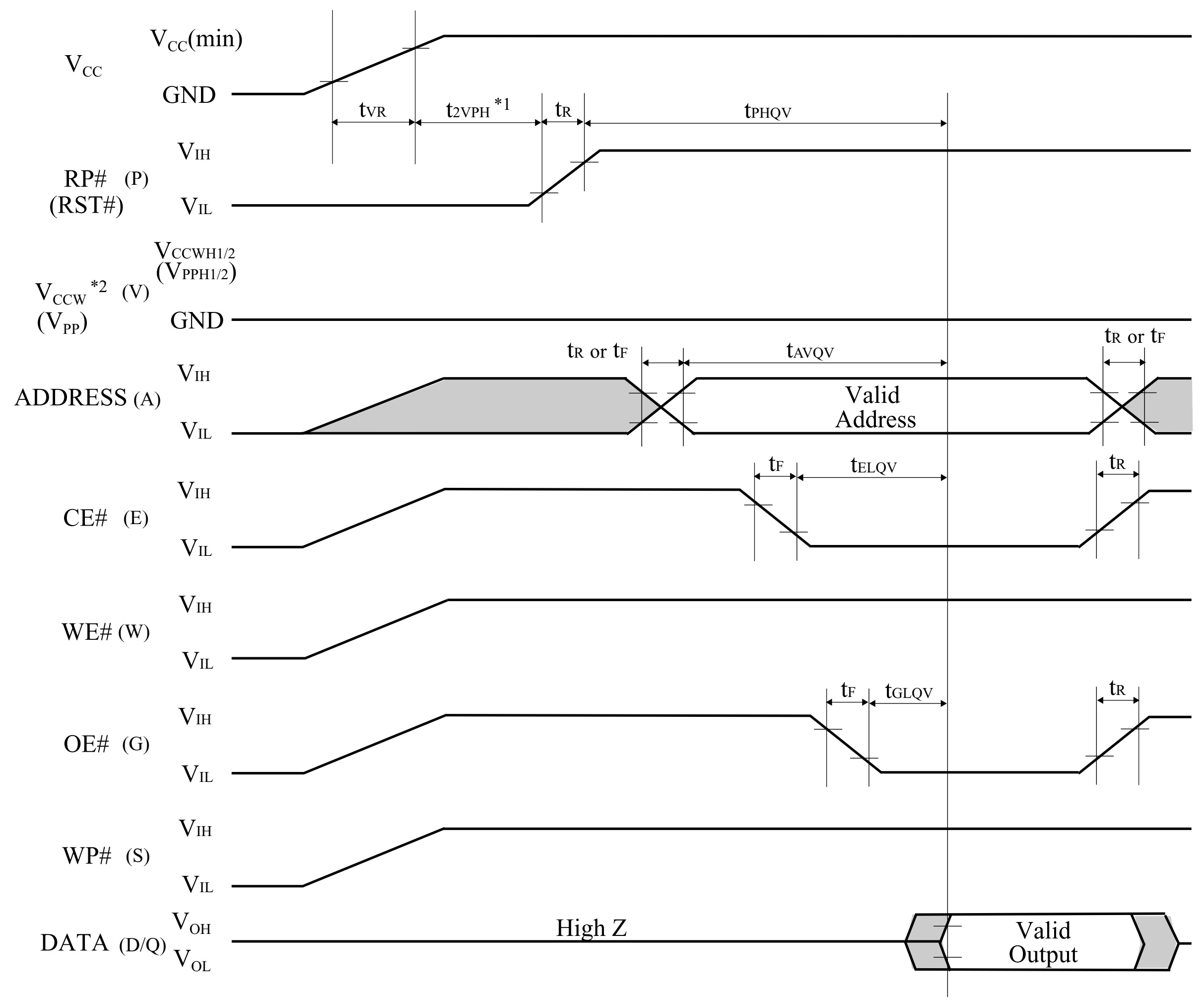
2) Data protection through Vpp
When the level of Vpp is lower than VPPLK (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
For the lockout voltage, refer to the specification. (See chapter 6.2.3.)

3) Data protection through RP#
When the RP# is kept low during power up and power down sequence such as voltage transition, write operation on the flash memory is disabled, write protecting all blocks.
For the details of RP# control, refer to the specification. (See chapter 5.6 and 6.2.7.)

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 t_{5VPH} for the device in 5V operations.

*2 To prevent the unwanted writes, system designers should consider the V_{CCW} (V_{PP}) switch, which connects V_{CCW} (V_{PP}) to GND during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations.
See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “ELECTRICAL SPECIFICATIONS“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.
   t_R(Max.) and t_F(Max.) for RP# (RST#) are 100µs/V.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

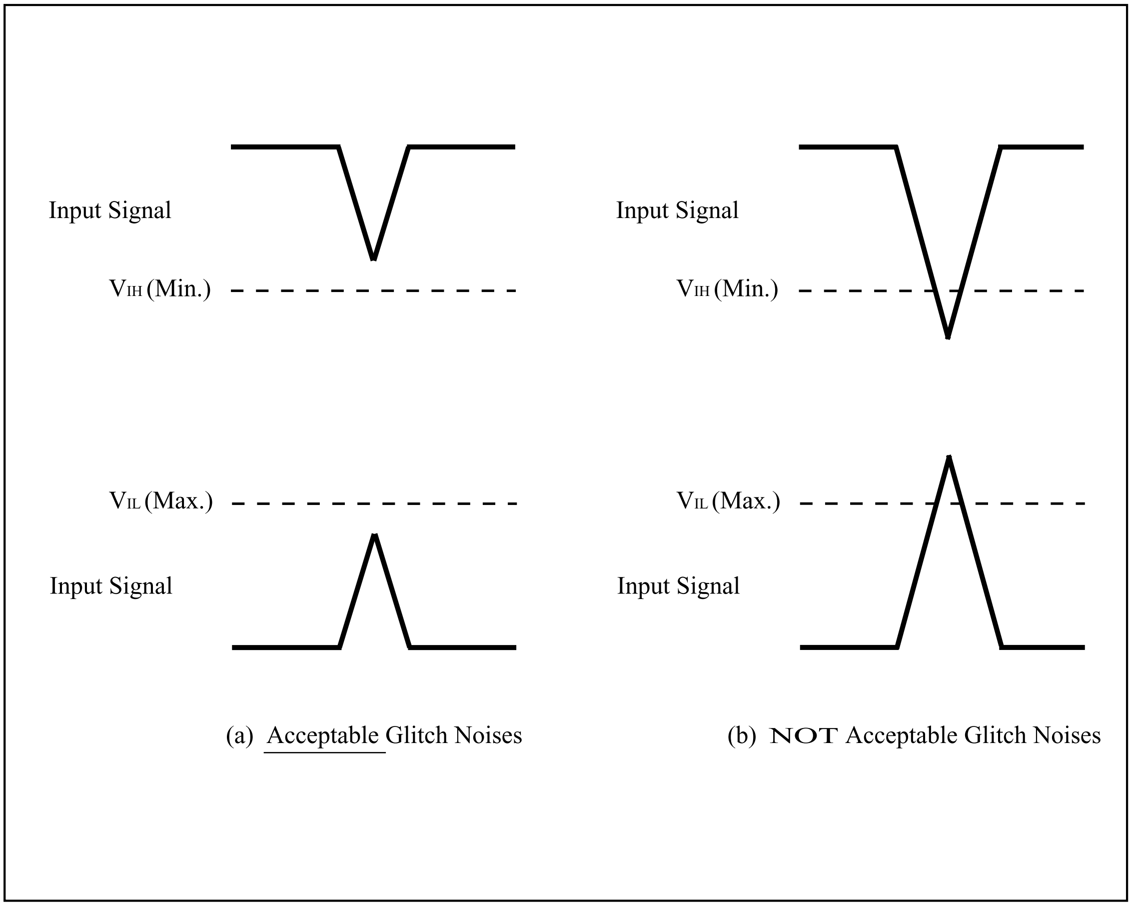


Figure A-2. Waveform for Glitch Noises

See the “DC CHARACTERISTICS“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

SHARP

NORTH AMERICA

SHARP Microelectronics of the Americas
5700 NW Pacific Rim Blvd.
Camas, WA 98607, U.S.A.
Phone: (1) 360-834-2500
Fax: (1) 360-834-8903
Fast Info: (1) 800-833-9437
www.sharpsma.com

EUROPE

SHARP Microelectronics Europe
Division of Sharp Electronics (Europe) GmbH
Sonninstrasse 3
20097 Hamburg, Germany
Phone: (49) 40-2376-2286
Fax: (49) 40-2376-2232
www.sharpsme.com

JAPAN

SHARP Corporation
Electronic Components & Devices
22-22 Nagaike-cho, Abeno-Ku
Osaka 545-8522, Japan
Phone: (81) 6-6621-1221
Fax: (81) 6117-725300/6117-725301
www.sharp-world.com

TAIWAN

SHARP Electronic Components
(Taiwan) Corporation
8F-A, No. 16, Sec. 4, Nanking E. Rd.
Taipei, Taiwan, Republic of China
Phone: (886) 2-2577-7341
Fax: (886) 2-2577-7326/2-2577-7328

SINGAPORE

SHARP Electronics (Singapore) PTE., Ltd.
438A, Alexandra Road, #05-01/02
Alexandra Technopark,
Singapore 119967
Phone: (65) 271-3566
Fax: (65) 271-3855

KOREA

SHARP Electronic Components
(Korea) Corporation
RM 501 Geosung B/D, 541
Dohwa-dong, Mapo-ku
Seoul 121-701, Korea
Phone: (82) 2-711-5813 ~ 8
Fax: (82) 2-711-5819

CHINA

SHARP Microelectronics of China
(Shanghai) Co., Ltd.
28 Xin Jin Qiao Road King Tower 16F
Pudong Shanghai, 201206 P.R. China
Phone: (86) 21-5854-7710/21-5834-6056
Fax: (86) 21-5854-4340/21-5834-6057
Head Office:
No. 360, Bashen Road,
Xin Development Bldg. 22
Waigaoqiao Free Trade Zone Shanghai
200131 P.R. China
Email: smc@china.global.sharp.co.jp

HONG KONG

SHARP-ROXY (Hong Kong) Ltd.
3rd Business Division,
17/F, Admiralty Centre, Tower 1
18 Harcourt Road, Hong Kong
Phone: (852) 28229311
Fax: (852) 28660779
www.sharp.com.hk
Shenzhen Representative Office:
Room 13B1, Tower C,
Electronics Science & Technology Building
Shen Nan Zhong Road
Shenzhen, P.R. China
Phone: (86) 755-3273731
Fax: (86) 755-3273735