

N-channel 40 V, 1.7 mΩ typ., 160 A, STripFET™ VI DeepGATE™ Power MOSFET in a I²PAK package

Datasheet — production data

Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STI300N4F6	40 V	2.2 mΩ	160 A ⁽¹⁾

1. Limited by wire bonding
- Standard level V_{GS(th)}
- 100% avalanche rated

Applications

- Automotive switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R_{DS(on)} in all packages.

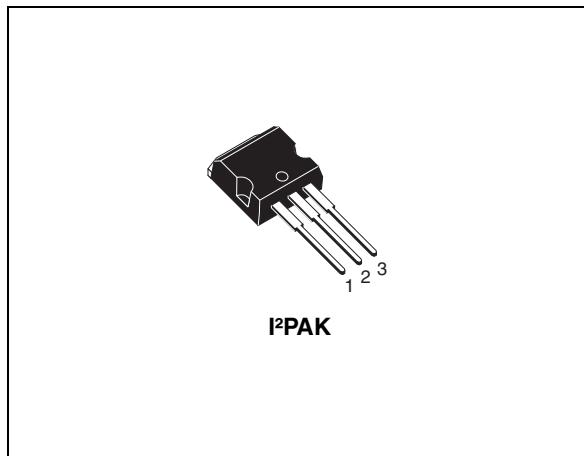


Figure 1. Internal schematic diagram

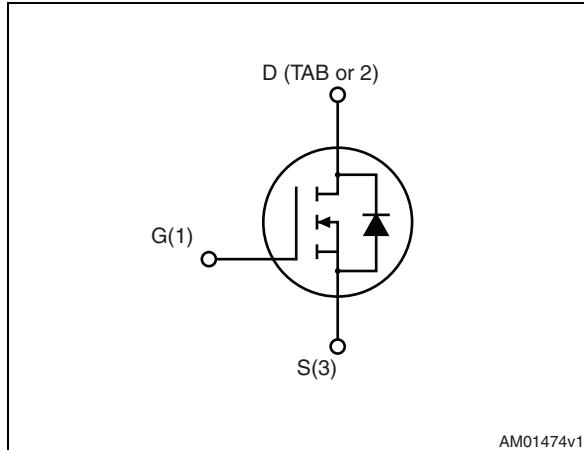


Table 1. Device summary

Order code	Marking	Package	Packaging
STI300N4F6	300N4F6	I ² PAK	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
2.1	Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	12

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	160	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	640	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
I_{AV}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	160	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_D=I_{AV}$, $V_{DD}=35\text{ V}$)	1100	mJ
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Limited by wire bonding
2. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	

2 Electrical characteristics

($T_J = 25^\circ\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage ($V_{GS}=0$)	$I_D = 250 \mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 40 \text{ V}$, $V_{GS} = 40 \text{ V}$, $T_C = 125^\circ\text{C}$			1 100	μA μA
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$			100	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2		4	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$		1.7	2.2	$\text{m}\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			13800		nF
C_{oss}	Output capacitance	$V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$,	-	1870	-	nF
C_{rss}	Reverse transfer capacitance	$V_{GS} = 0$		1095		nF
Q_g	Total gate charge	$V_{DD} = 20 \text{ V}$, $I_D = 160 \text{ A}$	-	240		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10 \text{ V}$	-	59	-	nC
Q_{gd}	Gate-drain charge	(see <i>Figure 14</i>)		75.2		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(\text{on})}$	Turn-on delay time			28		ns
t_r	Rise time			98		ns
$t_{d(\text{off})}$	Turn-off delay time	$V_{DD} = 20 \text{ V}$, $I_D = 80 \text{ A}$,	-	190	-	ns
t_f	Fall time	$R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see <i>Figure 13</i>)		95		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-	-	160	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	640	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 160 \text{ A}, V_{GS} = 0$	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 160 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 32 \text{ V}, T_J = 25^\circ\text{C}$ (see Figure 15)	-	58.7 99.2 3.38		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

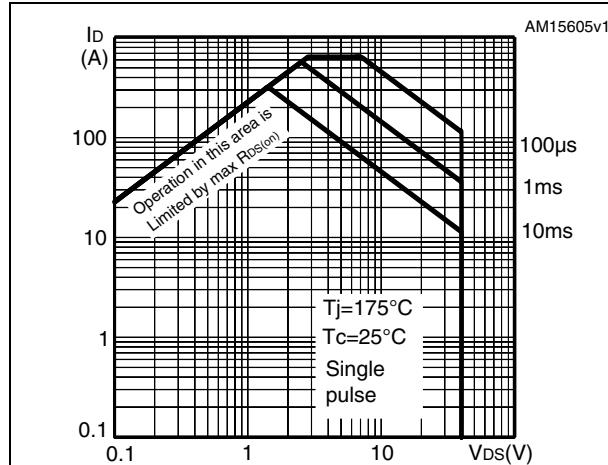


Figure 3. Thermal impedance

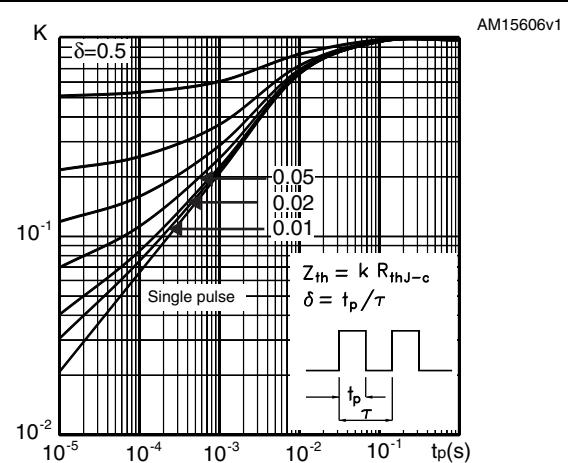


Figure 4. Output characteristics

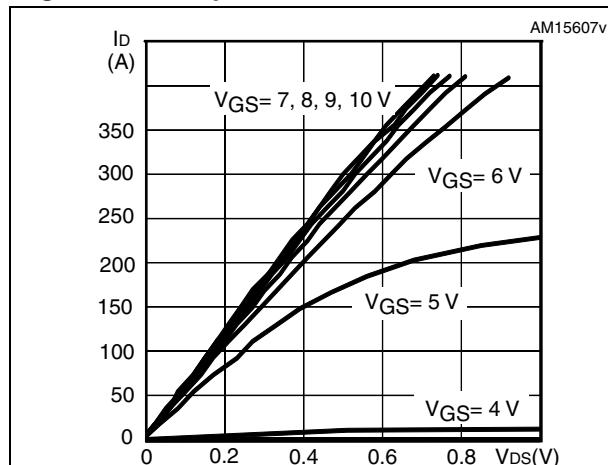


Figure 5. Transfer characteristics

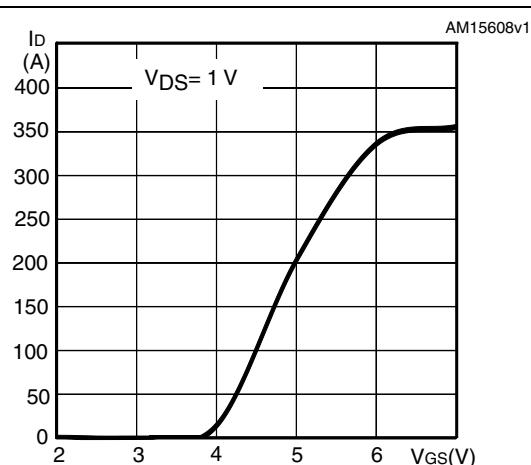


Figure 6. Gate charge vs gate-source voltage

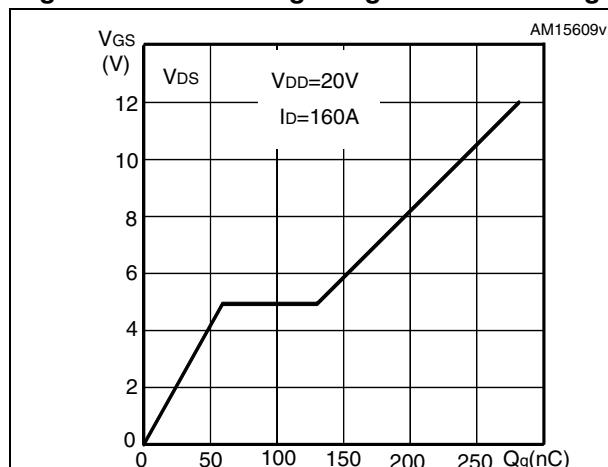


Figure 7. Static drain-source on-resistance

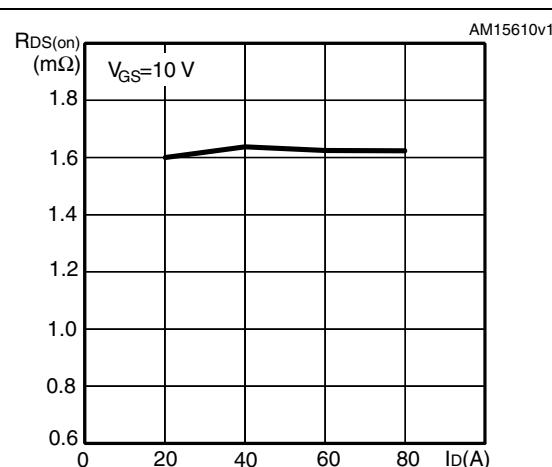
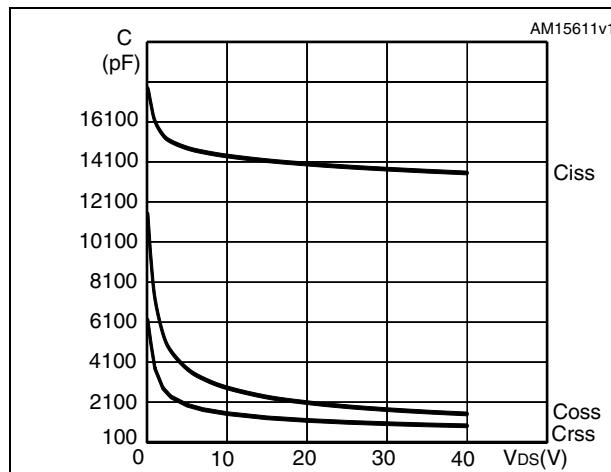
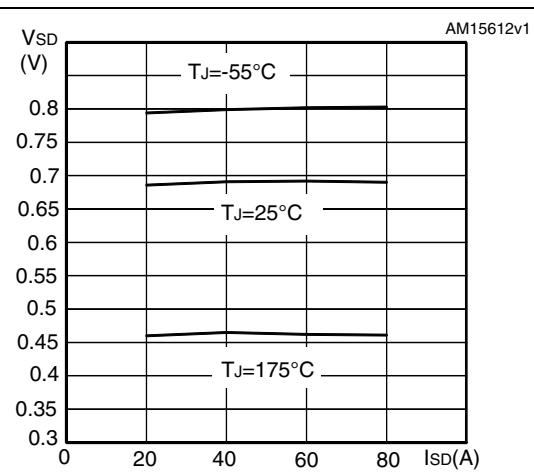
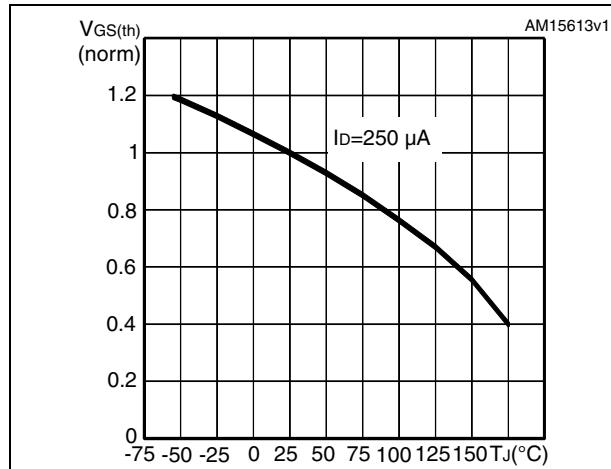
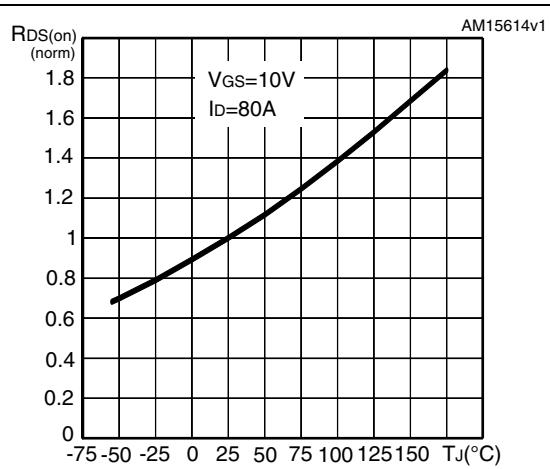
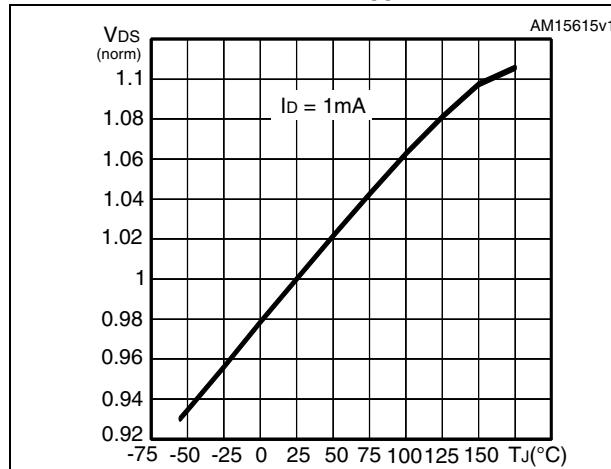


Figure 8. Capacitance variations**Figure 9. Drain-source diode forward characteristics****Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on-resistance vs temperature****Figure 12. Normalized BVDSS vs temperature**

3 Test circuits

Figure 13. Switching times test circuit for resistive load

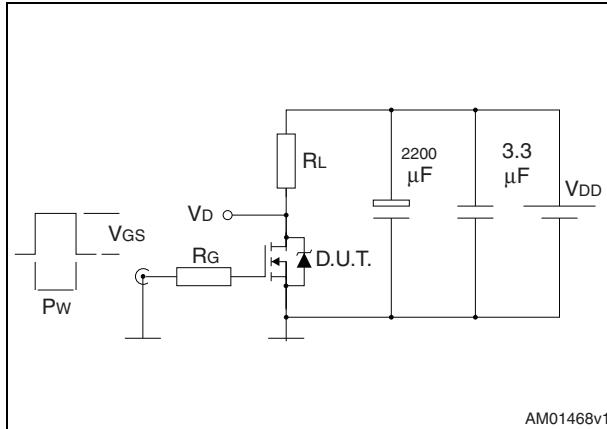


Figure 14. Gate charge test circuit

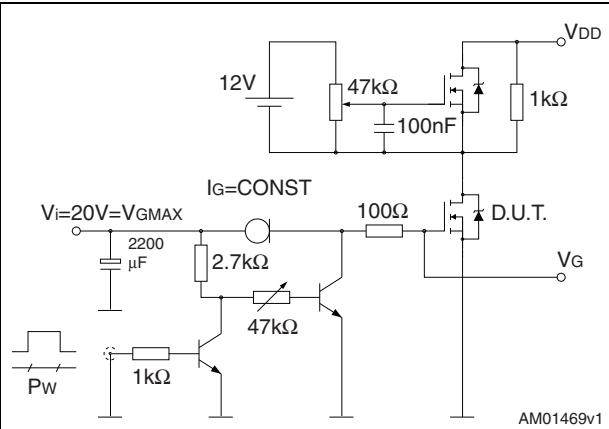


Figure 15. Test circuit for inductive load switching and diode recovery times

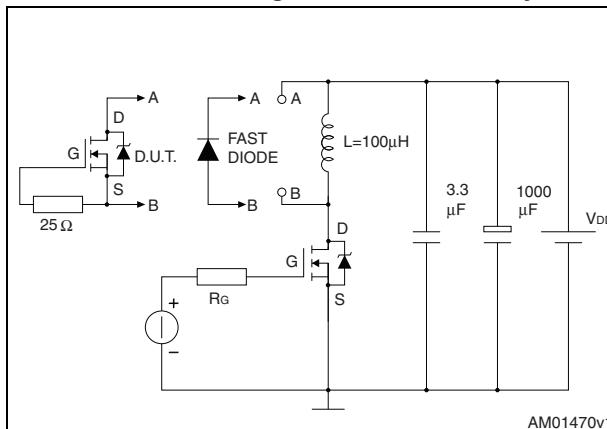


Figure 16. Unclamped inductive load test circuit

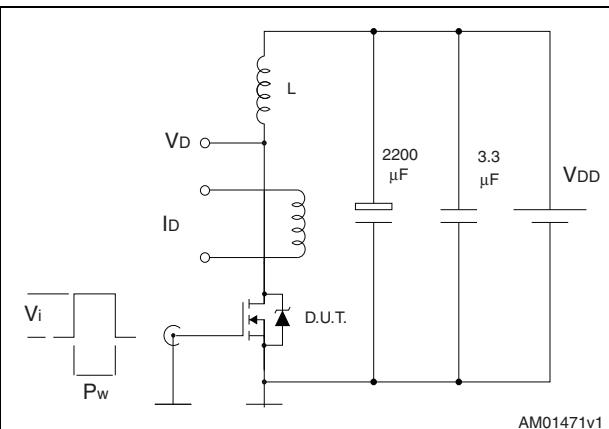


Figure 17. Unclamped inductive waveform

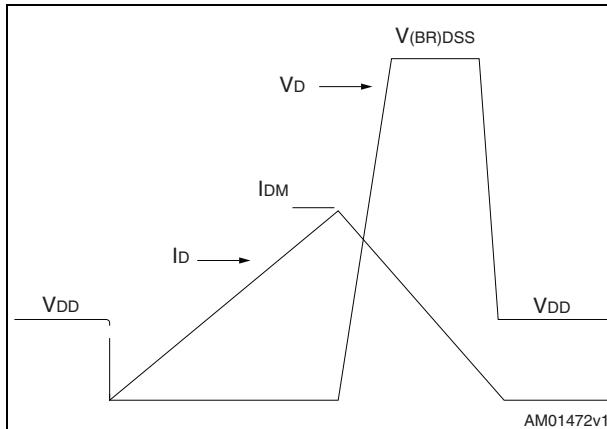
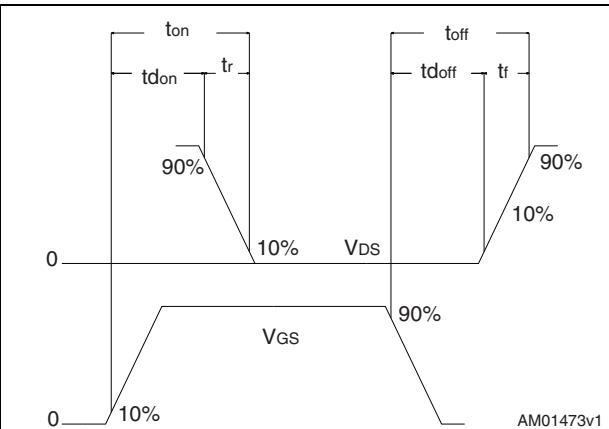


Figure 18. Switching time waveform

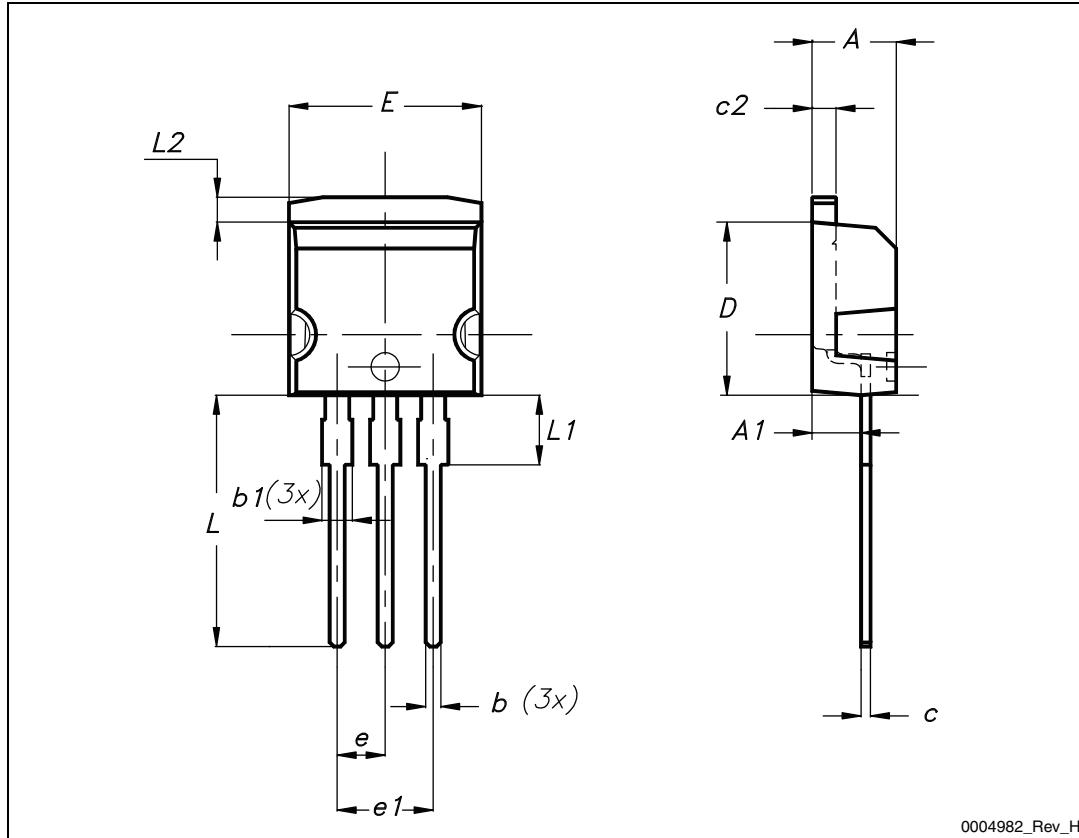


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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Table 8. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 19. I²PAK (TO-262) drawing

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
05-Oct-2010	1	First release
01-Feb-2013	2	<ul style="list-style-type: none">– Added: <i>Section 2.1: Electrical characteristics (curves)</i>– Minor text changes– Updated: <i>Section 4: Package mechanical data</i>

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