

### **CP771-CXDM4060P**

## P-Channel MOSFET Die Enhancement-Mode

The CP771-CXDM4060P medium power P-Channel MOSFET is optimized for power management and drive circuit applications where energy efficiency is a critical design element. The 7.5 mil thick die provides an ultra low profile device that is readily attached via wire bond techniques. Parametrically, low on-resistance and gate charge characteristics maximize efficient operation.

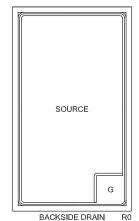
#### **FEATURES:**

- Low on-resistance, r<sub>DS(ON)</sub>
- Low gate charge, Q<sub>gs</sub>
- High drain current density
- · Low profile geometry
- Metalization suitable for standard die attach technologies
- Top metalization optimized for wire bonding

#### **APPLICATIONS:**

- Power management
- Motor drives

- · Load switching
- DC-DC conversion



#### **MECHANICAL SPECIFICATIONS:**

55 x 32 MILS
7.5 MILS
7.3 x 7.3 MILS
50 x 25 MILS
AI – 40,000Å
Ti/Ni/Ag - 1,000Å/3,000Å/10,000Å
3.15 MILS
8 INCHES
25,200

MAXIMUM RATINGS: (TA=25°C)	SYMBOL		UNITS
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	25	V
Continuous Drain Current (Steady State)	I <sub>D</sub>	6.0	Α
Maximum Pulsed Drain Current, tp=10µs	I <sub>DM</sub>	20	Α
Operating and Storage Junction Temperature	T <sub>I</sub> , T <sub>eta</sub>	-55 to +150	°C

#### **ELECTRICAL CHARACTERISTICS**: (T<sub>A</sub>=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
IGSSF, IGSSR	$V_{GS}$ =25V, $V_{DS}$ =0			100	nA
IDSS	$V_{DS}$ =40V, $V_{GS}$ =0			1.0	μΑ
BVDSS	$V_{GS}$ =0, $I_D$ =250 $\mu$ A	40			V
V <sub>GS(th)</sub>	$V_{GS}=V_{DS}$ , $I_{D}=250\mu A$	1.0	2.0	3.0	V
V <sub>SD</sub>	$V_{GS}=0, I_{S}=2.0A$			1.2	V
rDS(ON)	$V_{GS}$ =10V, $I_D$ =6.0A		48	65	$m\Omega$
rDS(ON)	$V_{GS}$ =4.5V, $I_{D}$ =4.0A		80	95	mΩ
` '				R1 (28	-March 2019)

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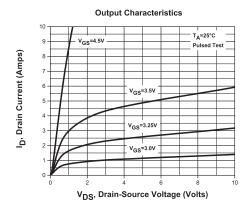
ELECTRICA	L CHARACTERISTICS - Continued: (	T <sub>A</sub> =25°C unle	ess otherwise	noted)	
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
C <sub>rss</sub>	$V_{DS}$ =25V, $V_{GS}$ =0, f=1.0MHz		61		pF
C <sub>iss</sub>	$V_{DS}$ =25V, $V_{GS}$ =0, f=1.0MHz		750		pF
C <sub>oss</sub>	$V_{DS}$ =25V, $V_{GS}$ =0, f=1.0MHz		56		pF
$Q_{g(tot)}$	$V_{DS}$ =32V, $V_{GS}$ =4.5V, $I_{D}$ =6.0A		6.5		nC
Q <sub>gs</sub>	$V_{DS}$ =32V, $V_{GS}$ =4.5V, $I_{D}$ =6.0A		3.2		nC
Q <sub>gd</sub>	$V_{DS}$ =32V, $V_{GS}$ =4.5V, $I_{D}$ =6.0A		2.7		nC
ton	$V_{DS}$ =20V, $V_{GS}$ =10V, $V_{D}$ =1.0A		18		ns
toff	$R_{G}$ =3.0 $\Omega$ , $R_{L}$ =20 $\Omega$		64		ns

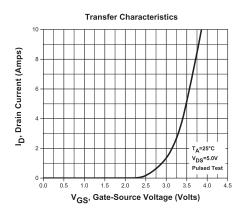
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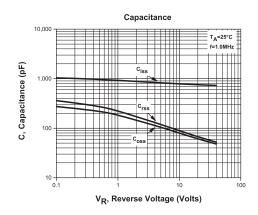
## **Typical Electrical Characteristics**

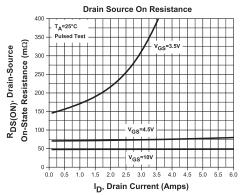


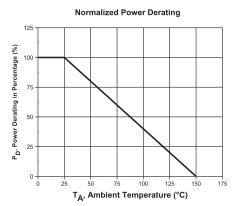
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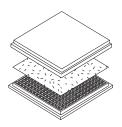






#### BARE DIE PACKING OPTIONS

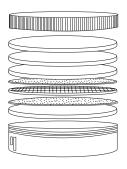




#### BARE DIE IN TRAY (WAFFLE) PACK

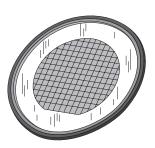
CT: Singulated die in tray (waffle) pack. (example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes). (example: CP211-PART NUMBER-CM)



#### **UNSAWN WAFER**

WN: Full wafer, unsawn, 100% tested with reject die inked. (example: CP211-PART NUMBER-WN)



#### SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,

100% tested with reject die inked. (example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications: www.centralsemi.com/bdspecs

R2 (3-April 2017)

#### **OUTSTANDING SUPPORT AND SUPERIOR SERVICES**



#### PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- · Inventory bonding
- · Consolidated shipping options

- · Custom bar coding for shipments
- · Custom product packing

#### **DESIGNER SUPPORT/SERVICES**

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- · Custom electrical curves
- · Environmental regulation compliance
- · Customer specific screening
- Up-screening capabilities

- · Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- · Application and design sample kits
- Custom product and package development

#### REQUESTING PRODUCT PLATING

- 1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
- 2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

#### **CONTACT US**

#### Corporate Headquarters & Customer Support Team

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# Product End of Life Notification

PDN ID:	PDN01159
Notification Date:	10/08/20
	4/08/21
Last Shipment Date	10/08/21

Summary: The CP771 wafer process is being discontinued and is now classified as End of Life (EOL). Replacement wafer process CP805 was previously referenced in PCN191, June 19, 2020.

Although Central Semiconductor Corp. makes every effort to continue to produce devices that have been proclaimed EOL (End of Life) by other manufacturers, it is an accepted industry practice to discontinue certain devices when customer demand falls below a minimum level of sustainability. Accordingly, the following product(s) have been transitioned to End of Life status as part of Central's ongoing Product Management Process. Any replacement products are noted below. The effective date for placing last purchase orders will be six (6) months from the date of this notice and twelve (12) months from the notice date for final shipments, and minimum order quantities may apply. The last purchase and shipment dates may be extended if inventory is available.

\* All Plating types (PBFREE,TIN/LEAD) for each item listed are included in this notice.

Central Part Number	Replacement
CP771-CXDM4060P-CT	CP805-CXDM4060P-CT
CP771-CXDM4060P-WN	CP805-CXDM4060P-WN

Central would be happy to assist you by providing additional information or technical data to help locate an alternate source if we have no replacement available. Please email your requests to engineering@centralsemi.com.

DISCLAIMER: This End of Life (EOL) notification is in accordance with JEDEC standard JESD48 - Product Discontinuance. Central Semiconductor Corp. will make every effort to offer life-time buy (LTB) opportunities and/or offer replacement devices to existing customers for discontinued devices, however, one or both may not be possible for all devices. Please contact your local Central Semiconductor sales representative for LTB opportunities/additional information.

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