

Description

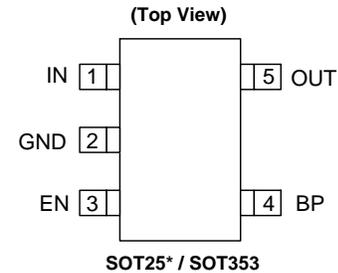
The AP7115 is a 150mA, fixed output voltage, low dropout linear regulator. The device includes pass element, error amplifier, band gap reference, current-limit and thermal shutdown circuit. The characteristics of low dropout voltage and low quiescent current make it suitable for use in battery powered devices. The typical quiescent current is approximately 50 μ A. Several fixed output voltages are available from 1.0V to 3.5V. Additional protection is provided with built-in current-limit and thermal-shutdown functions.

Features

- Wide Input Voltage Range from 2.5V to 5.5V
- 200mV Low Dropout Voltage at 150mA Output Current
- Guaranteed 150mA Output Current
- Low Quiescent Current 50 μ A
- Output Voltage from 1.0V to 3.5V
- $\pm 2\%$ Output Voltage Accuracy
- Low Temperature Drift at Output Voltage
- High PSRR
- Fast Transient Response
- Current Limit Protection
- Short Circuit Protection
- Thermal Shutdown Protection
- SOT25 and SOT353: Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments

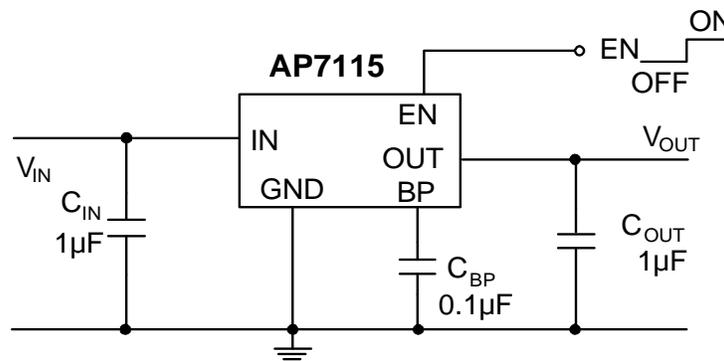


* SOT25 is not recommended for new design.

Applications

- Wireless Communication
- GSM/GPRS Cellular Phones
- Handheld Mobile Devices
- Battery Powered Devices
- CD-ROM, DVD, and LAN Cards
- PC and Notebook Peripherals

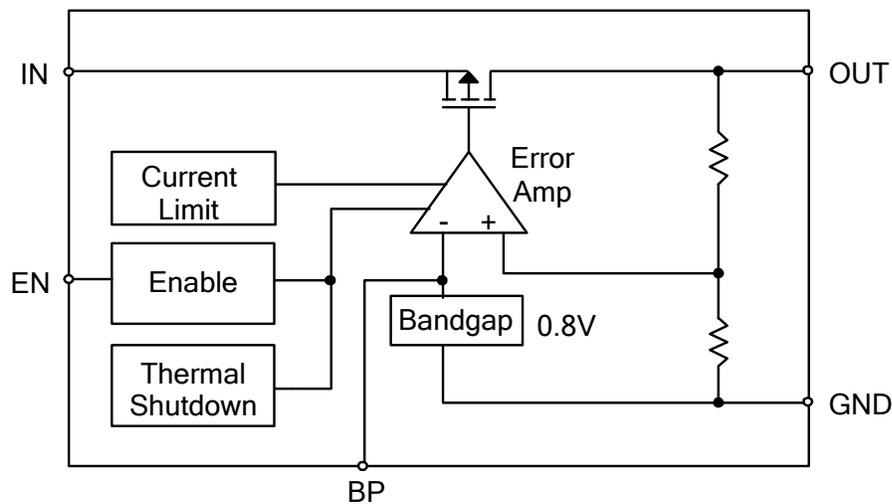
Typical Applications Circuit



Pin Descriptions

| Pin Number | Pin Name | Description |
|------------|----------|---------------------|
| 1 | IN | Voltage Input |
| 2 | GND | Ground |
| 3 | EN | Chip Enable Control |
| 4 | BP | Band-Gap Bypass |
| 5 | OUT | Voltage Output |

Functional Block Diagram



Absolute Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

| Symbol | Parameter | Rating | Unit |
|-----------|--------------------------------------|----------------------|------------------|
| ESD HBM | Human Body Model ESD Protection | 3.5 | kV |
| ESD MM | Machine Model ESD Protection | 400 | V |
| V_{IN} | Input Voltage | -0.3 to 5.5 | V |
| V_{EN} | EN Pin Voltage | -0.3 to 5.5 | V |
| V_{OUT} | Output Voltage | -0.3 to $V_{IN}+0.3$ | V |
| V_{BP} | Band Gap Bypass Pin Voltage | -0.3 to 5.5 | V |
| P_D | Power Dissipation | 500 | mW |
| T_J | Operating Junction Temperature Range | -40 to +125 | $^\circ\text{C}$ |
| T_{ST} | Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |

Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

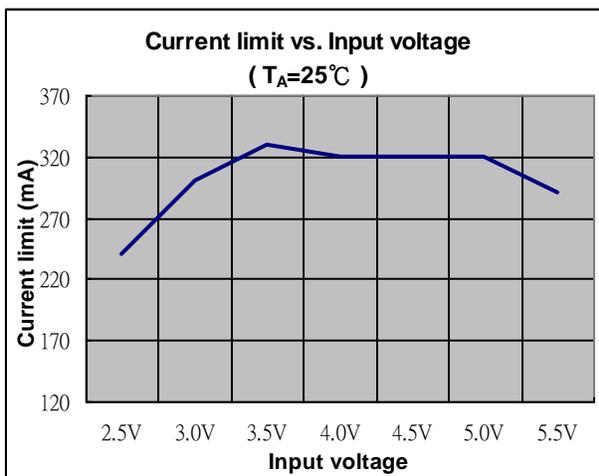
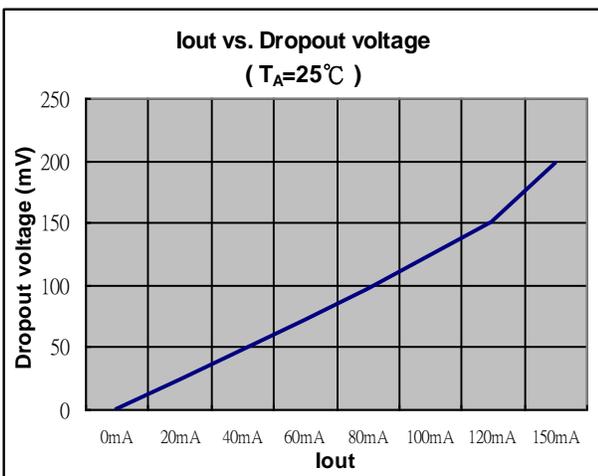
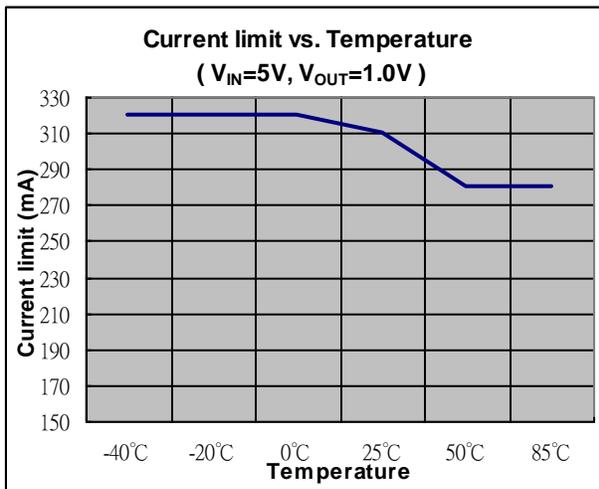
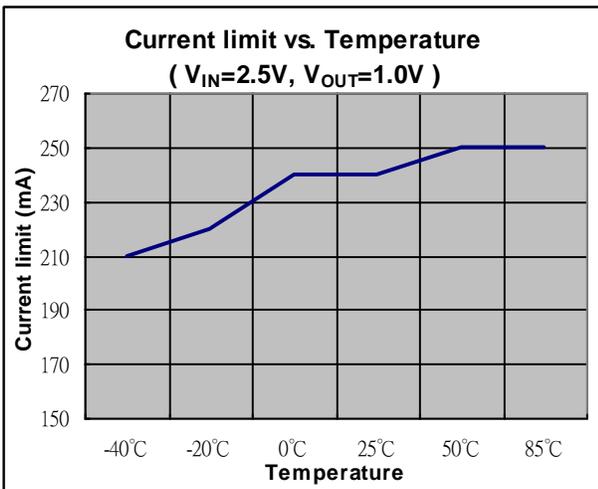
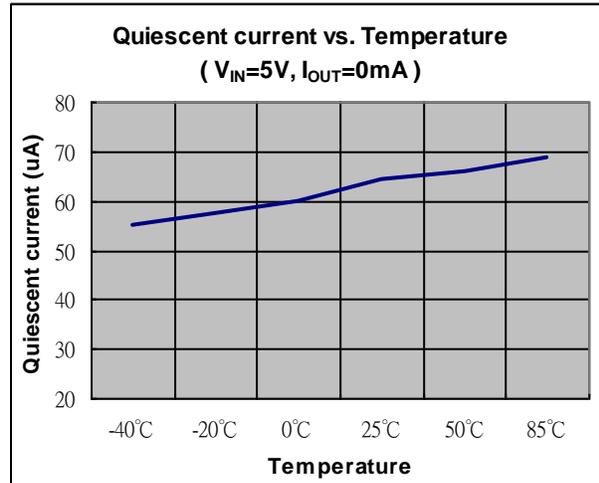
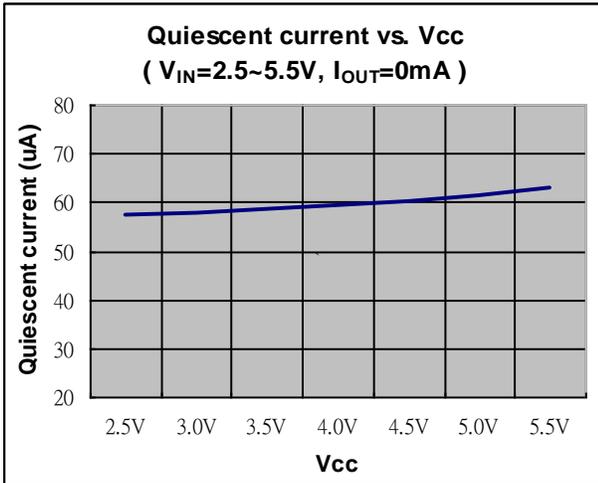
| Symbol | Parameter | Min | Max | Unit |
|-----------|-------------------------------|-----|-----|------------------|
| V_{IN} | Input Voltage | 2.5 | 5.5 | V |
| I_{OUT} | Output Current | — | 150 | mA |
| T_A | Operating Ambient Temperature | -40 | +85 | $^\circ\text{C}$ |

Electrical Characteristics (@ $V_{CC} = 3.3\text{V}$, $I_L = 30\text{mA}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT} = 1\mu\text{F}$, $T_A = +25^\circ\text{C}$)

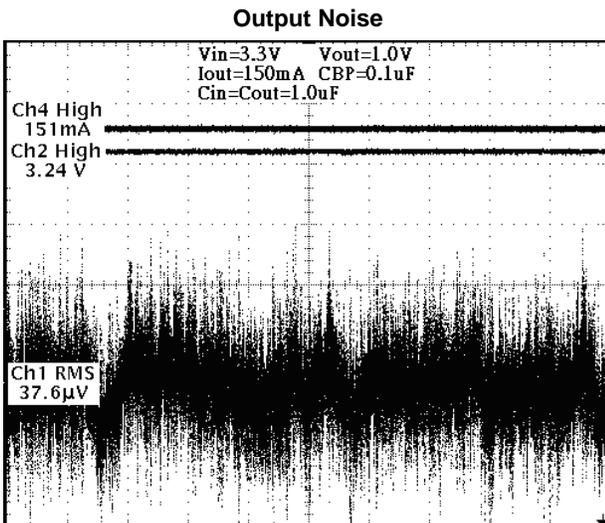
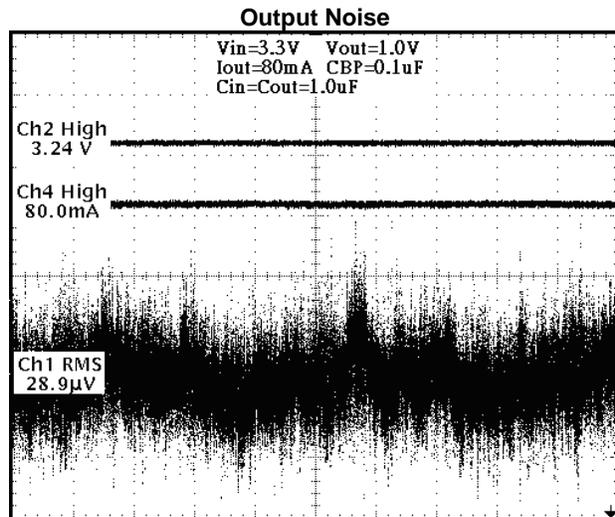
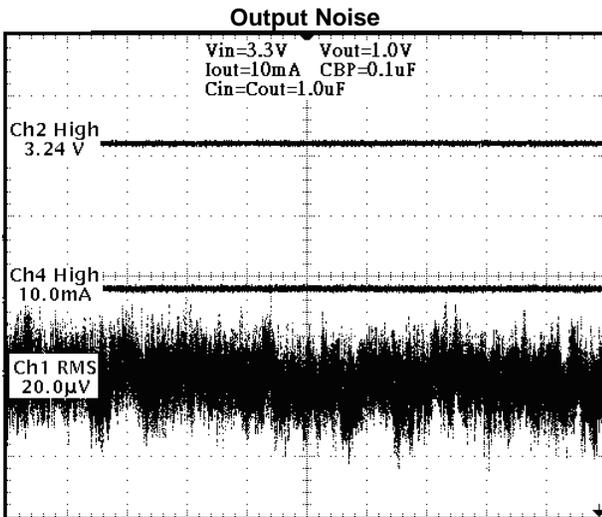
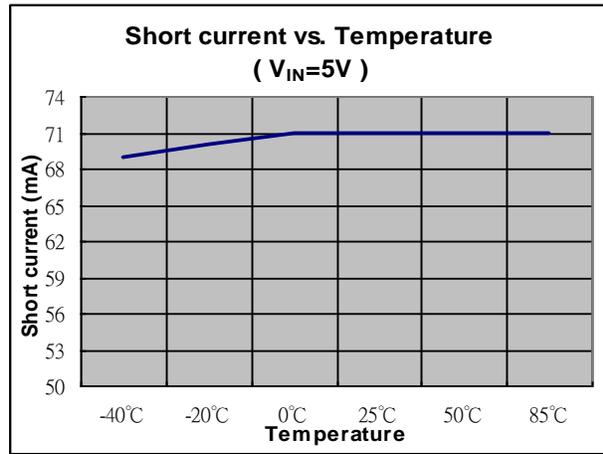
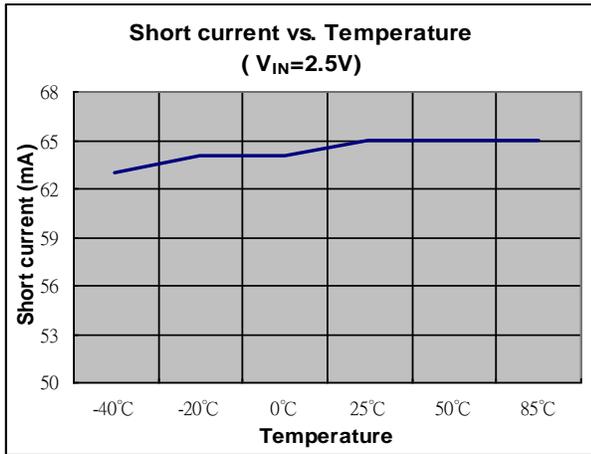
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--|---|-----|-------|-------|---------------------------|
| System Supply Input | | | | | | |
| V_{IN} | Operating Input Voltage | $I_L = 0$ to 150mA | 2.5 | — | 5.5 | V |
| $\Delta V_{OUT}/V_{OUT}$ | Output Voltage Accuracy | $V_{IN} = V_{OUT} + 1\text{V}$ where $1\text{mA} \leq I_{OUT} \leq 50\text{mA}$ | -2 | — | 2 | % |
| V_{DO} | Dropout Voltage | $I_L = 150\text{mA}$ | — | 200 | 300 | mV |
| I_{OUT} | Output Current | $V_{IN} - V_{OUT} = 1\text{V}$ | 150 | — | — | mA |
| I_Q | Quiescent Current | $V_{IN} = V_{OUT} + 1\text{V}$ where $I_{OUT} = 0$ and $V_{EN} = V_{IN}$ | — | 50 | 80 | μA |
| $I_{SHUTDOWN}$ | Shutdown Current | $V_{IN} = V_{OUT} + 1\text{V}$ where $I_{OUT} = 0$ and $V_{EN} = 0$ | — | 0.1 | 1 | μA |
| PSRR | Power Supply Rejection Ratio | $I_{OUT} = 30\text{mA}$, $f = 1\text{kHz}$ | — | 70 | — | dB |
| I_{LIMIT} | Current Limit | — | 200 | 250 | — | mA |
| Thermal Management | | | | | | |
| $T_{SHUTDOWN}$ | Thermal Shutdown | — | — | +150 | — | $^\circ\text{C}$ |
| Reference Voltage | | | | | | |
| $\Delta V_{REF}/\Delta T$ | Tempco of Bandgap Reference | — | — | 30 | 50 | ppm/ $^\circ\text{C}$ |
| $\Delta V_{OUT}/\Delta T$ | Tempco of Output Voltage | $I_{OUT} = 30\text{mA}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | — | 50 | 100 | ppm/ $^\circ\text{C}$ |
| Control and Protection | | | | | | |
| $V_{IH,EN}$ | — | — | 2.0 | — | — | V |
| $V_{IL,EN}$ | — | — | — | — | 0.7 | V |
| I_{EN} | EN Pin Leakage Current | $V_{EN} = V_{IN}$ @ $V_{IN} = 5.0\text{V}$ and $V_{SS} = 0\text{V}$ | — | 0.01 | 0.1 | μA |
| | | $V_{EN} = V_{SS}$ @ $V_{IN} = 5.0\text{V}$ and $V_{SS} = 0\text{V}$ | — | 0.01 | 0.1 | μA |
| Regulation | | | | | | |
| $\Delta V_O/\Delta V_{IN}$ | Line Regulation | $V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$ where $V_{OUT} > 2.0\text{V}$, $I_{OUT} = 30\text{mA}$ | — | 0.02 | 0.1 | %/V |
| ΔV_{LOAD} | Load Regulation | $1\text{mA} \leq I_L \leq 150\text{mA}$ where $V_{IN} = V_{OUT} + 1\text{V}$ | — | 0.003 | 0.006 | %/mA |
| Noise | | | | | | |
| e_n | Output Noise | BW = 10Hz to 100kHz | — | 50 | — | μV_{rms} |
| Thermal Resistance | | | | | | |
| θ_{JA} | Thermal Resistance Junction-to-Ambient | SOT25 (Note 4) | — | 200 | — | $^\circ\text{C}/\text{W}$ |
| | | SOT353 (Note 4) | — | 337 | — | $^\circ\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance Junction-to-Case | SOT25 (Note 4) | — | 52 | — | $^\circ\text{C}/\text{W}$ |
| | | SOT353 (Note 4) | — | 121 | — | $^\circ\text{C}/\text{W}$ |

Note: 4. Test condition for SOT25 and SOT353: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Typical Operating Characteristics

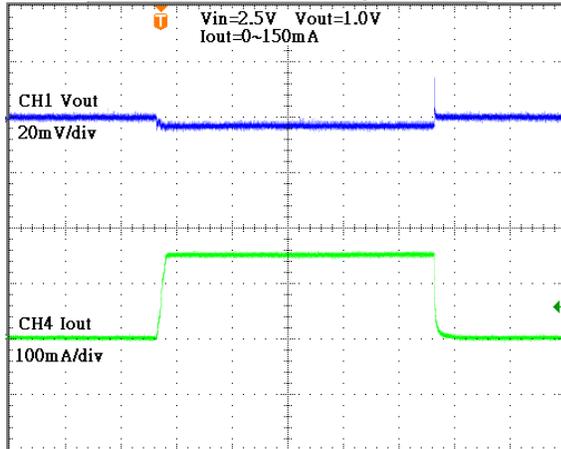


Typical Operating Characteristics (Cont.)

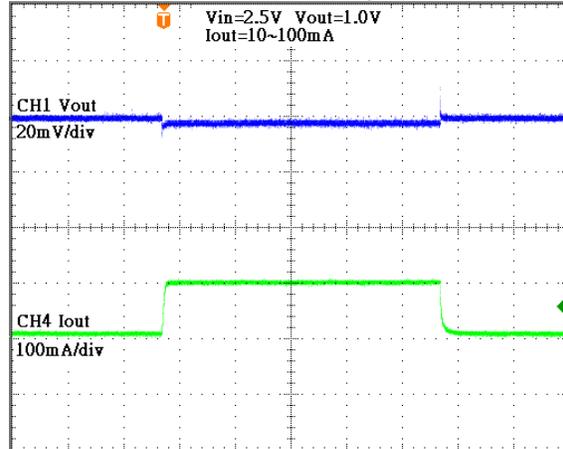


Typical Operating Characteristics (Cont.)

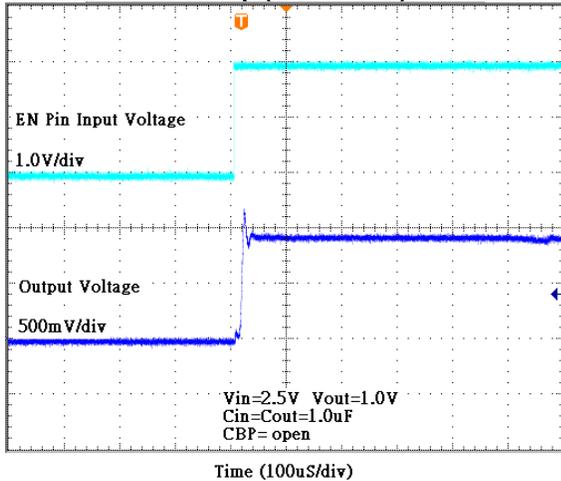
Load Transient Response



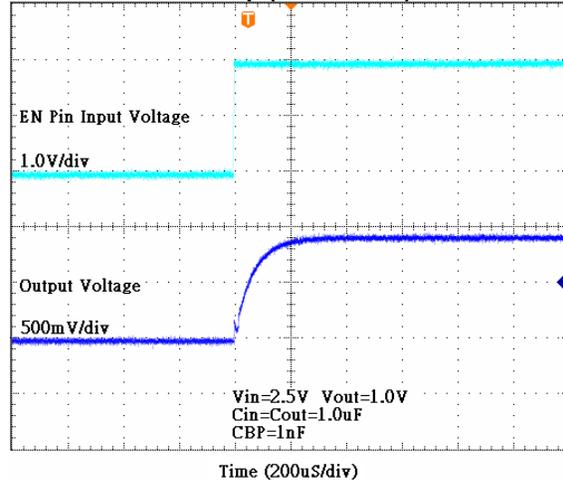
Load Transient Response



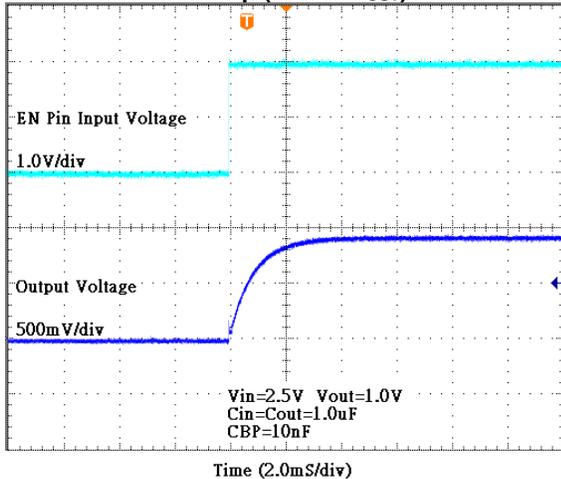
Start Up (EN vs. V_{OUT})



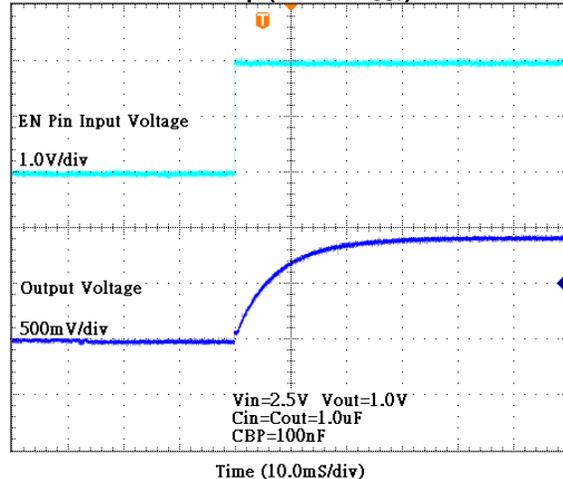
Start Up (EN vs. V_{OUT})



Start Up (EN vs. V_{OUT})



Start Up (EN vs. V_{OUT})



Application Note

Input Capacitor

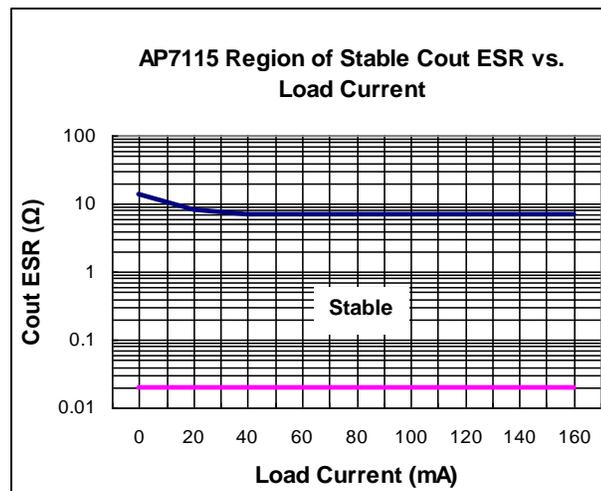
A 1 μ F input capacitor is required between the AP7115 input pin and GND.

There are no requirements for the ESR on input capacitor, but tolerance and temperature coefficient must be considered.

Output Capacitor

The AP7115 can work with very small ceramic output capacitors (1 μ F or greater). Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it from a zero to provide phase lead which is required for loop stability.

Figure below is Cout ESR vs. Load Current.



Band-Gap Bypass Capacitor

0.1 μ F bypass capacitor Between BP pin and GND can reduce output voltage noise.

Shutdown Input Operation

The AP7115 is shutdown by pulling the EN pin low, and turned on by driving the input high. If the shutdown feature is not required, the EN pin should be tied to VIN to keep the regulator on at all time.

Dropout Voltage

$$V_{\text{DROPOUT}} = V_{\text{IN}} - V_{\text{OUT}} = R_{\text{DS(ON)}} \times I_{\text{OUT}}$$

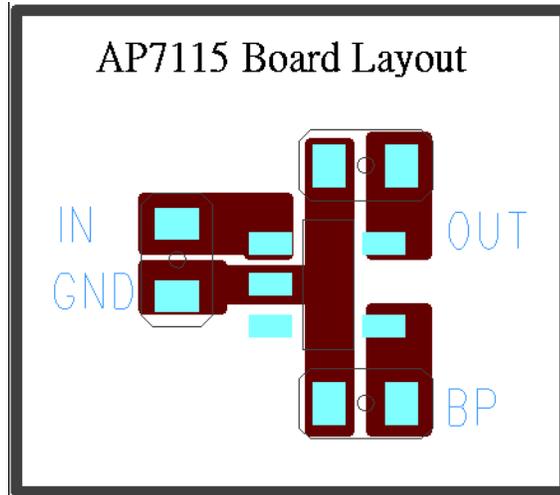
Current Limit

The AP7115 monitors and controls the PMOS' gate voltage, limiting the output current to 250mA (typ.). The output can be shorted to ground for an indefinite period of time without damaging the part.

Application Note (Cont.)

PCB Layout

Optimum performance can only be achieved when the device is mounted on a PC board according to the diagram below:



Thermal Considerations

Thermal Shutdown Protection limits power dissipation in AP7115. When the operation junction temperature exceeds +155°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by +30°C. For continuous operation, do not exceed absolute maximum operation junction temperature +125°C. The power dissipation definition in device is:

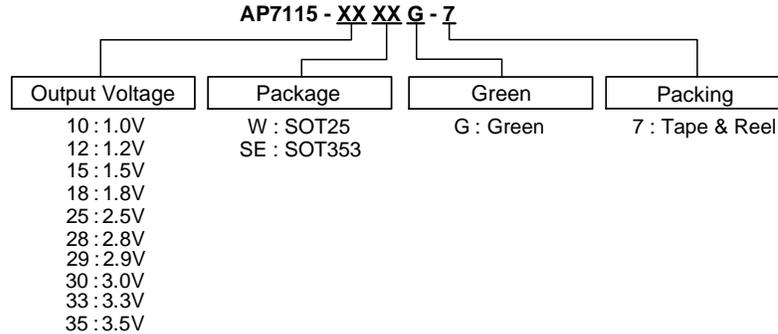
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature +125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Ordering Information



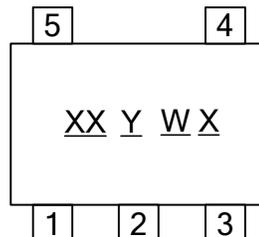
| Part Number | Package Code | Packaging (Note 5) | 7" Tape and Reel | |
|------------------------|--------------|--------------------|------------------|--------------------|
| | | | Quantity | Part Number Suffix |
| AP7115-XXWG-7 (Note 6) | W | SOT25 | 3000/Tape & Reel | -7 |
| AP7115-XXSEG-7 | SE | SOT353 | 3000/Tape & Reel | -7 |

Notes: 5. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at <http://www.diodes.com/package-outlines.html>.
6. SOT25 is not recommended for new design.

Marking Information

SOT25/SOT353

(Top View)



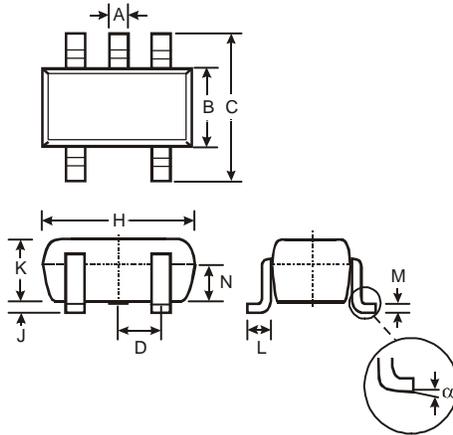
XX : Identification code
 Y : Year 0~9
 W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
 X : A~Z : Green

| Part Number | Identification Code | Part Number | Identification Code |
|----------------|---------------------|----------------|---------------------|
| SOT25 (Note 6) | | SOT353 | |
| AP7115-10WG-7 | FO | AP7115-10SEG-7 | GO |
| AP7115-12WG-7 | FP | AP7115-12SEG-7 | GP |
| AP7115-15WG-7 | FQ | AP7115-15SEG-7 | GQ |
| AP7115-18WG-7 | FR | AP7115-18SEG-7 | GR |
| AP7115-25WG-7 | FS | AP7115-25SEG-7 | GS |
| AP7115-28WG-7 | FT | AP7115-28SEG-7 | GT |
| AP7115-29WG-7 | FU | AP7115-29SEG-7 | GU |
| AP7115-30WG-7 | FV | AP7115-30SEG-7 | GV |
| AP7115-33WG-7 | FW | AP7115-33SEG-7 | GW |
| AP7115-35WG-7 | FX | AP7115-35SEG-7 | GX |

Package Outline Dimensions

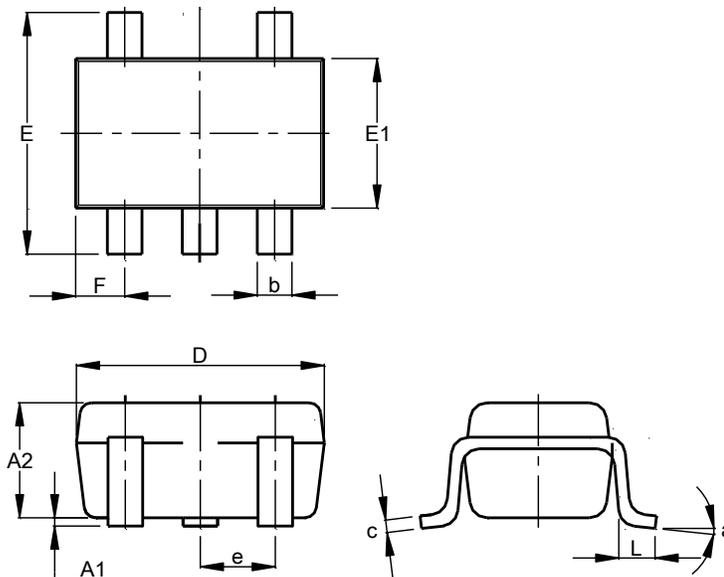
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: SOT25 (Note 6)



| SOT25 | | | |
|----------------------|-------|------|------|
| Dim | Min | Max | Typ |
| A | 0.35 | 0.50 | 0.38 |
| B | 1.50 | 1.70 | 1.60 |
| C | 2.70 | 3.00 | 2.80 |
| D | - | - | 0.95 |
| H | 2.90 | 3.10 | 3.00 |
| J | 0.013 | 0.10 | 0.05 |
| K | 1.00 | 1.30 | 1.10 |
| L | 0.35 | 0.55 | 0.40 |
| M | 0.10 | 0.20 | 0.15 |
| N | 0.70 | 0.80 | 0.75 |
| α | 0° | 8° | - |
| All Dimensions in mm | | | |

(2) Package Type: SOT353

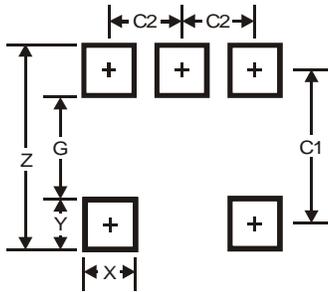


| SOT353 | | | |
|----------------------|-----------|------|-------|
| Dim | Min | Max | Typ |
| A1 | 0.00 | 0.10 | 0.05 |
| A2 | 0.90 | 1.00 | 1.00 |
| b | 0.10 | 0.30 | 0.25 |
| c | 0.10 | 0.22 | 0.11 |
| D | 1.80 | 2.20 | 2.15 |
| E | 2.00 | 2.20 | 2.10 |
| E1 | 1.15 | 1.35 | 1.30 |
| e | 0.650 BSC | | |
| F | 0.40 | 0.45 | 0.425 |
| L | 0.25 | 0.40 | 0.30 |
| a | 0° | 8° | -- |
| All Dimensions in mm | | | |

Suggested Pad Layout

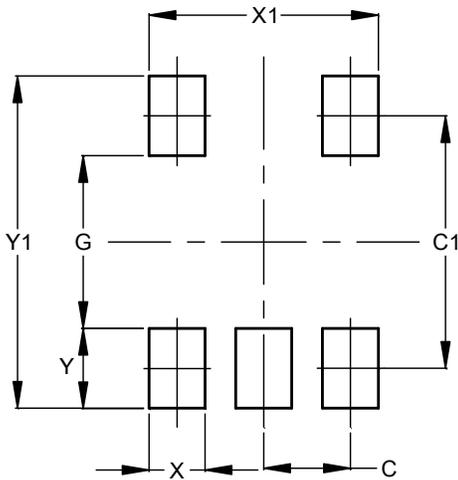
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

(1) Package Type: SOT25 (Note 6)



| Dimensions | Value |
|------------|-------|
| Z | 3.20 |
| G | 1.60 |
| X | 0.55 |
| Y | 0.80 |
| C1 | 2.40 |
| C2 | 0.95 |

(2) Package Type: SOT353



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.650 |
| C1 | 1.900 |
| G | 1.300 |
| X | 0.420 |
| X1 | 1.720 |
| Y | 0.600 |
| Y1 | 2.500 |

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