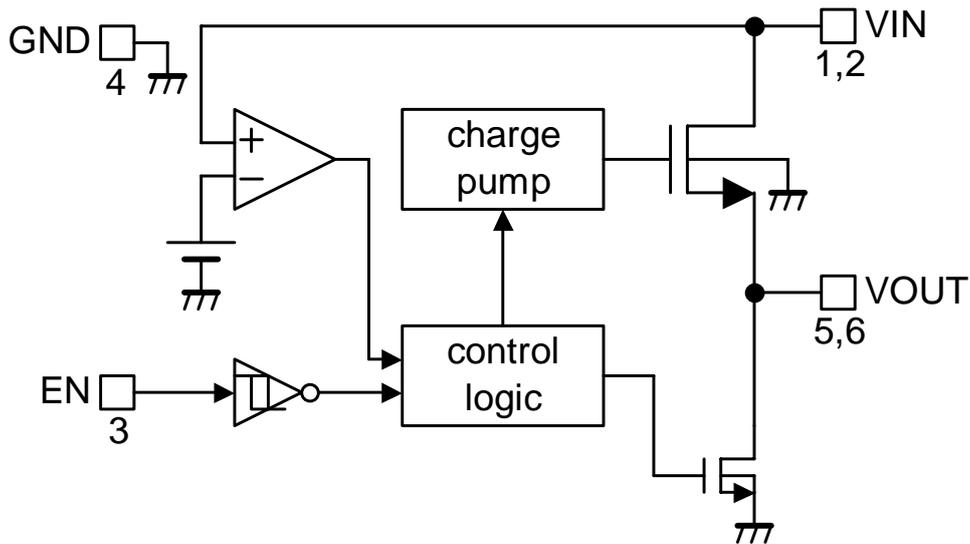
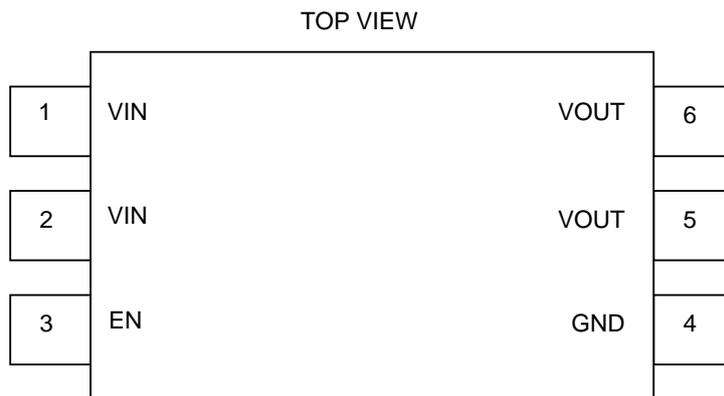


●Block Diagram



●Pin Configuration



●Pin Description

Pin No.	Symbol	Pin Function
1	VIN	Switch input pin. At use, connect each pin outside.
2		
3	EN	Switch control input pin (hysteresis input) Switch ON at High.
4	GND	Ground
5	VOUT	Switch output pin At use, connect each pin outside.
6		

● Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{IN}	-0.3 to 6.0	V
Control input voltage	V_{EN}	-0.3 to $V_{IN} + 0.3$	V
Switch output voltage	V_{OUT}	-0.3 to 6.0	V
Storage temperature	T_{STG}	-55 to 150	°C
Power dissipation	P_d	510 ^{*1}	mW

*1 Derating : 4.08mW/°C for operation above $T_a = 25^{\circ}C$.

● Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{IN}	3.0 to 5.5	V
Operating Temperature	T_{OPR}	-25 to 75	°C
Switch current	I_{OUT}	500	mA

● Electrical Characteristics Unless otherwise specified, $T_a = 25^{\circ}C$, $V_{IN} = 5V$,

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Operating current	I_{DD}	-	50	75	μA	$V_{EN} = 5V, V_{OUT} = \text{Open}$
Standby current	I_{STB}	-	0.1	1	μA	$V_{EN} = 0V, V_{OUT} = \text{Open}$
EN input voltage	V_{ENH}	-	-	2.5	V	High level input voltage
	V_{ENL}	0.7	-	-	V	Low level input voltage
EN input leak current	I_{EN}	-1	0.01	1	μA	
Switch on resistance	R_{ON}	-	200	255	$m\Omega$	$V_{IN} = 5V$
		-	250	335	$m\Omega$	$V_{IN} = 3.3V$
Switch leak current	I_{LEAK}	-	-	10	μA	At switch OFF
Switch rise time	T_{ON1}	-	0.4	0.8	ms	$R_L=10\Omega$. Refer to the timing diagram in Figure 2.
Switch rise delay time	T_{ON2}	-	0.5	1.0	ms	$R_L=10\Omega$. Refer to the timing diagram in Figure 2.
Switch fall time	T_{OFF1}	-	1	2	us	$R_L=10\Omega$. Refer to the timing diagram in Figure 2.
Switch fall delay time	T_{OFF2}	-	2	4	us	$R_L=10\Omega$. Refer to the timing diagram in Figure 2.
UVLO threshold voltage	V_{UVLO}	1.9	2.2	2.5	V	V_{IN} increasing
		1.8	2.1	2.4	V	V_{IN} decreasing
Discharge resistance	R_{DISC}	-	200	350	Ω	$V_{EN} = 0V, I_L = 1mA$
Discharge current	I_{DISC}	0.8	1.8	-	mA	$V_{EN} = 0V, V_{IN} = V_{OUT} = 1.8V$

● Measurement Circuit

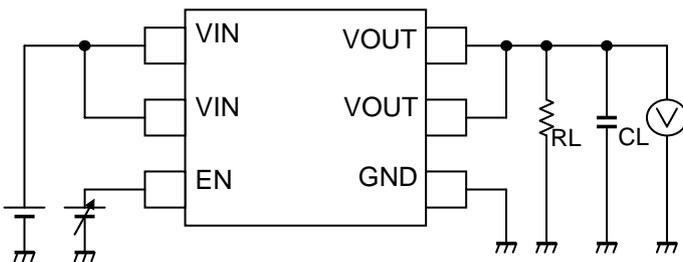


Figure 1. Measurement circuit

● Timing Diagram

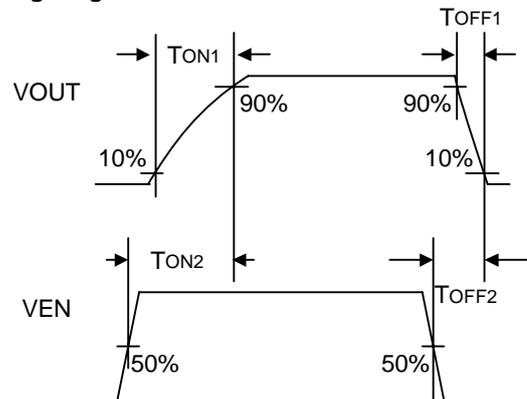


Figure 2. Timing diagram

● Typical Performance Curves

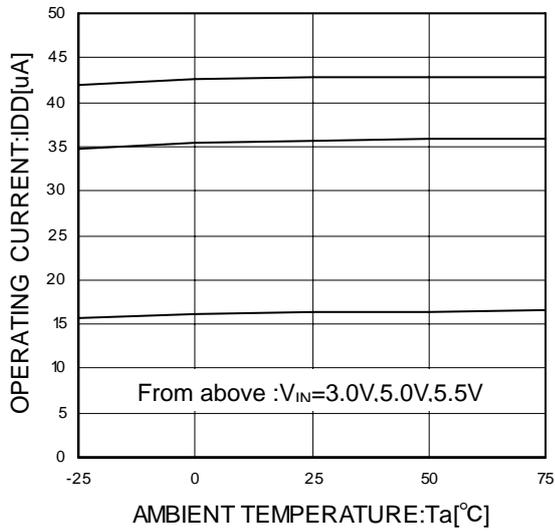


Figure 3. Operating current

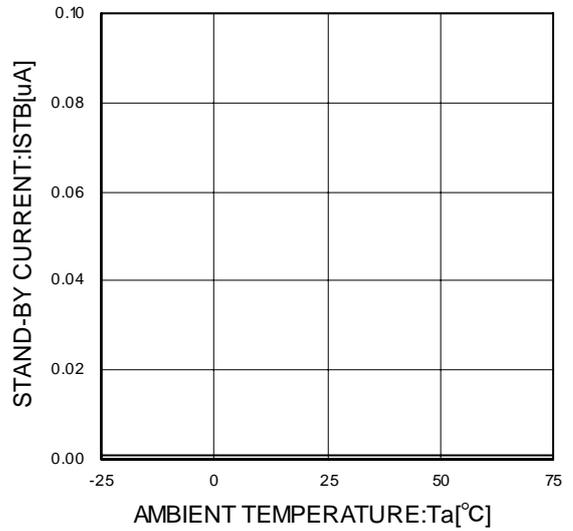


Figure 4. Standby current

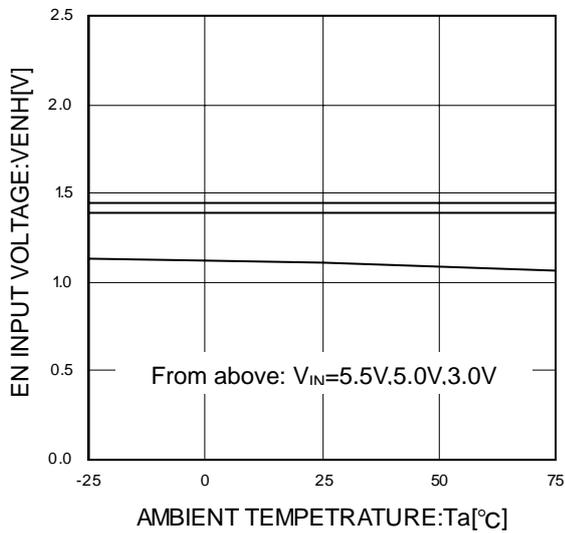


Figure 5. EN threshold voltage
(High level input voltage)

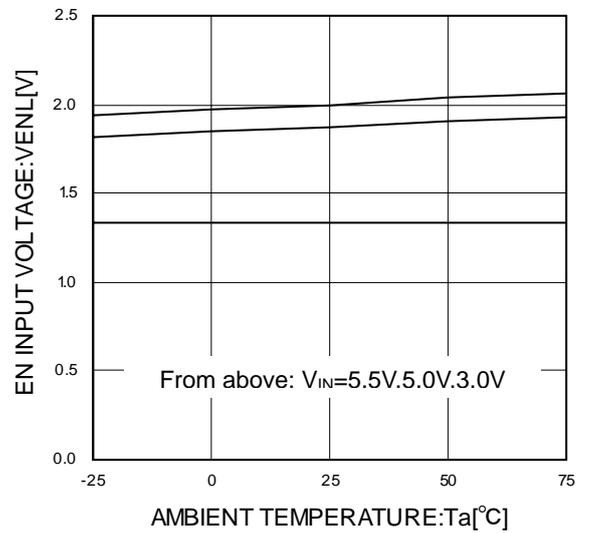


Figure 6. EN threshold voltage
(Low level input voltage)

● Typical Performance Curves - continued

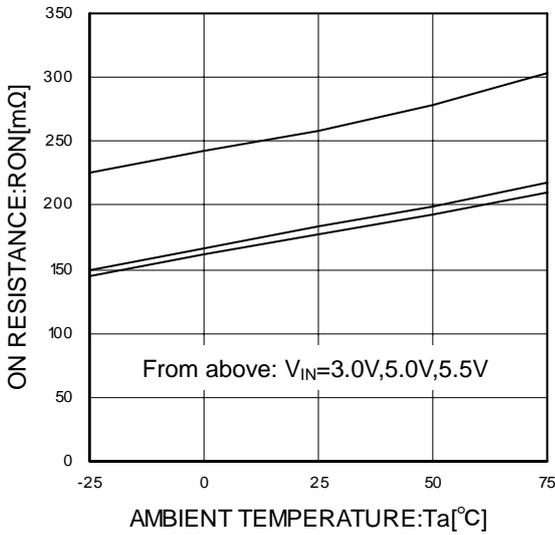


Figure 7. Switch on resistance

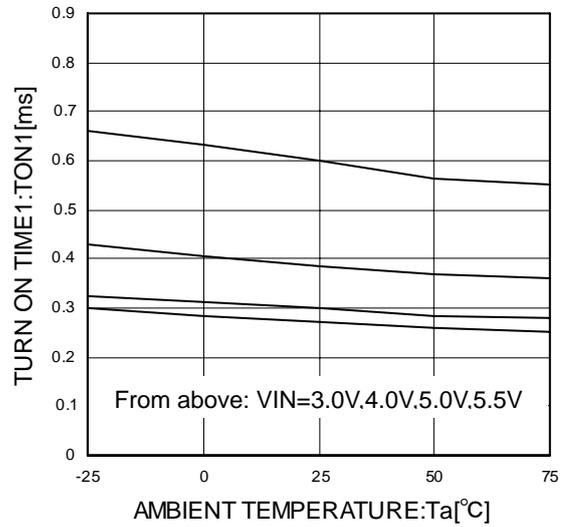


Figure 8. Switch rise time

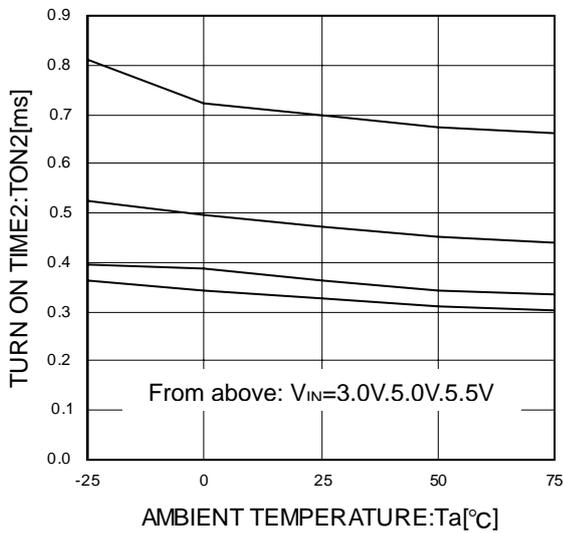


Figure 9. Switch rise delay time

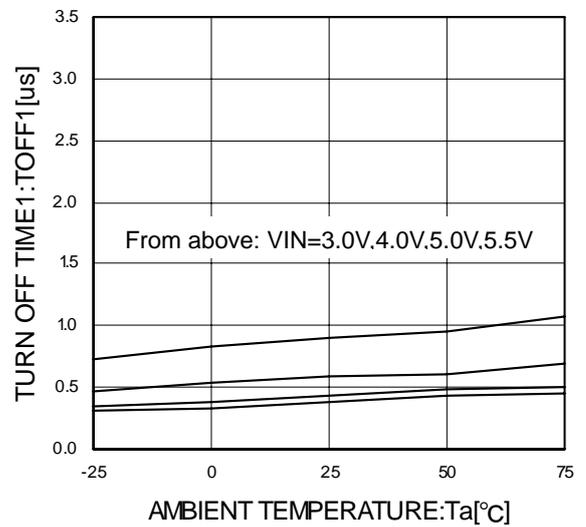


Figure 10. Switch fall time

● Typical Performance Curves - continued

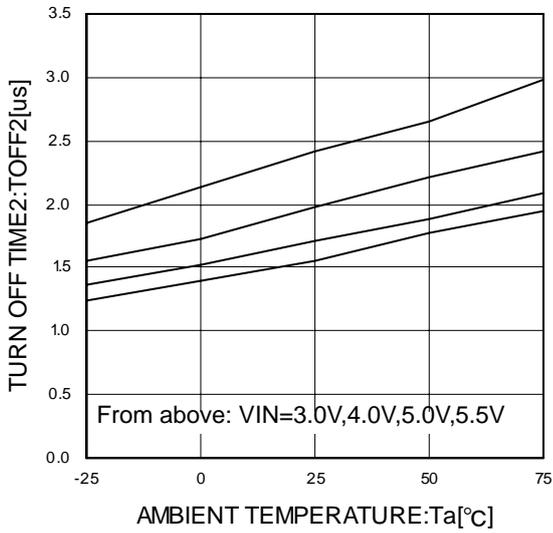


Figure 11. Switch fall delay time

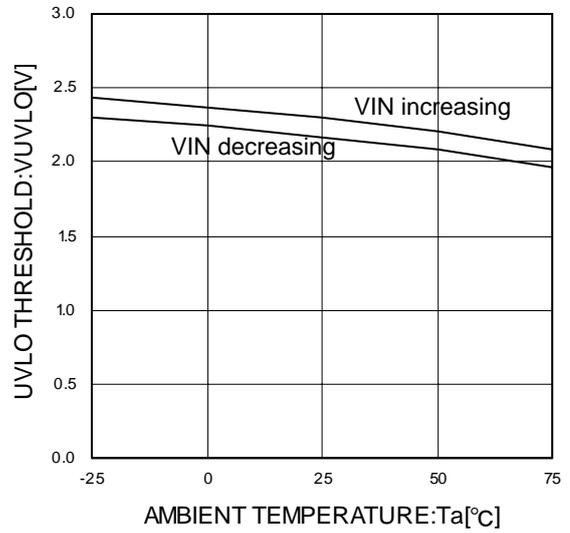


Figure 12. UVLO threshold voltage

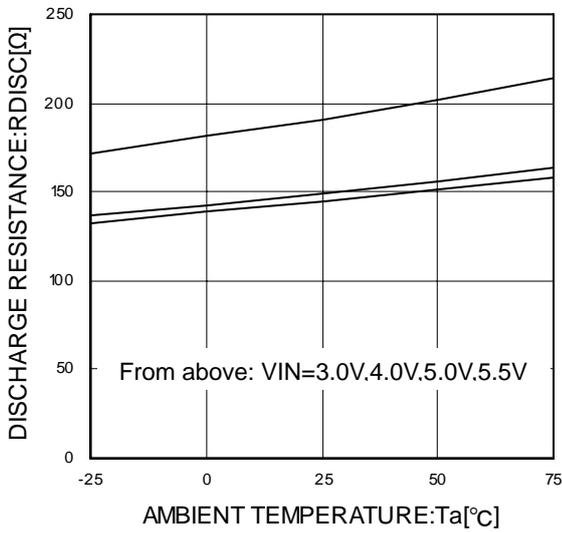


Figure 13. Discharge resistance

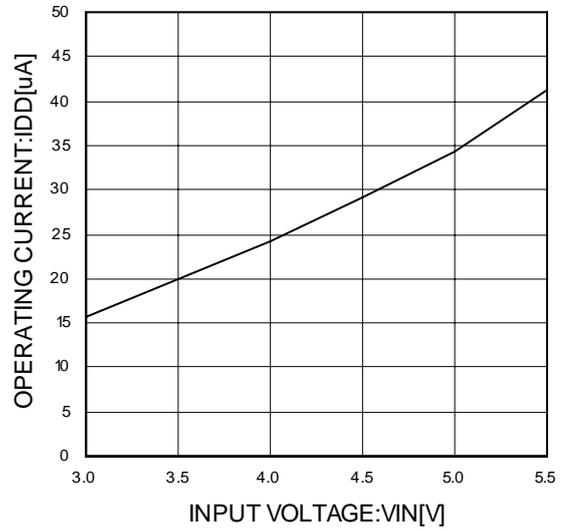


Figure 14. Operating current

● Typical Performance Curves - continued

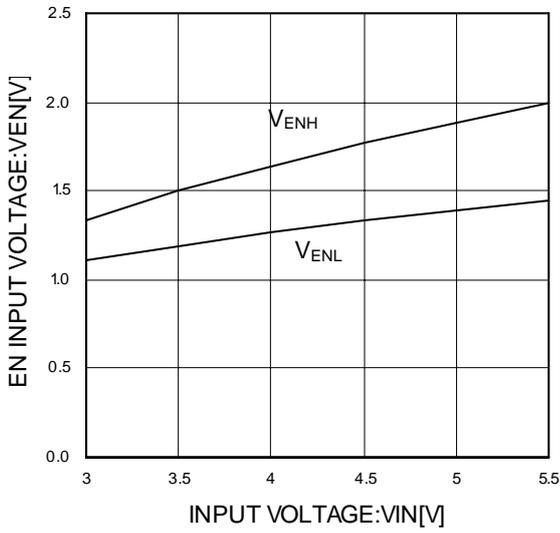


Figure 15. EN threshold voltage

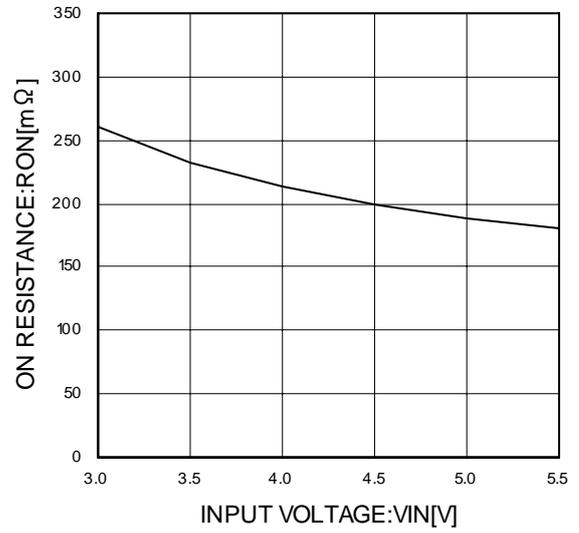


Figure 16. Switch on resistance

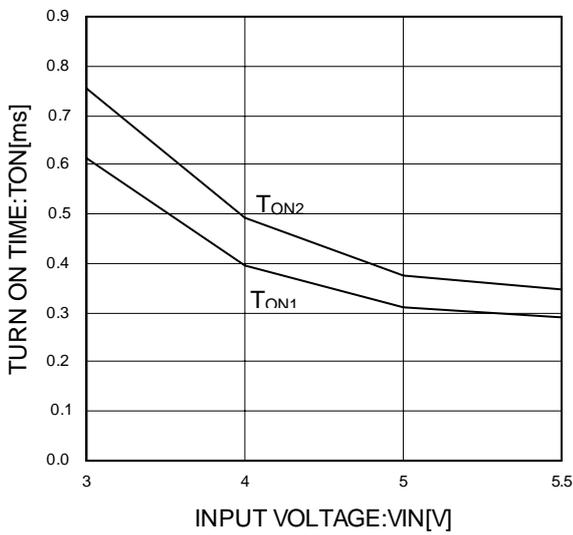


Figure 17. Switch rise time

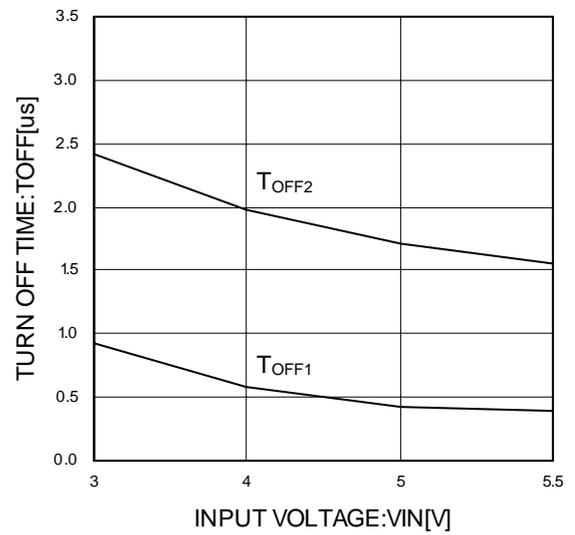


Figure 18. Switch fall time

● Typical Performance Curves - continued

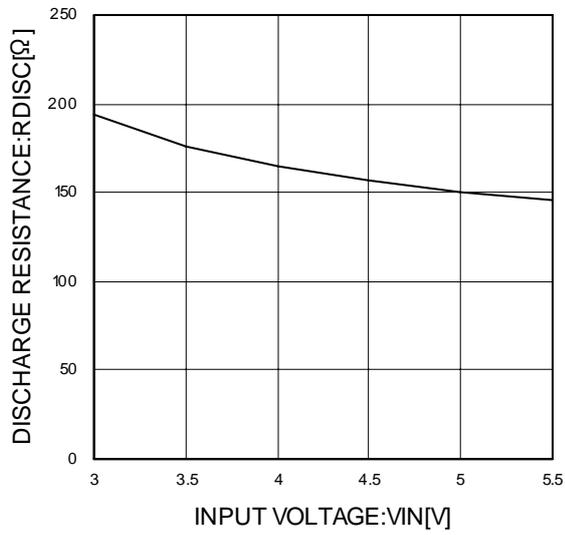


Figure 19. Discharge resistance

● Typical Wave Forms

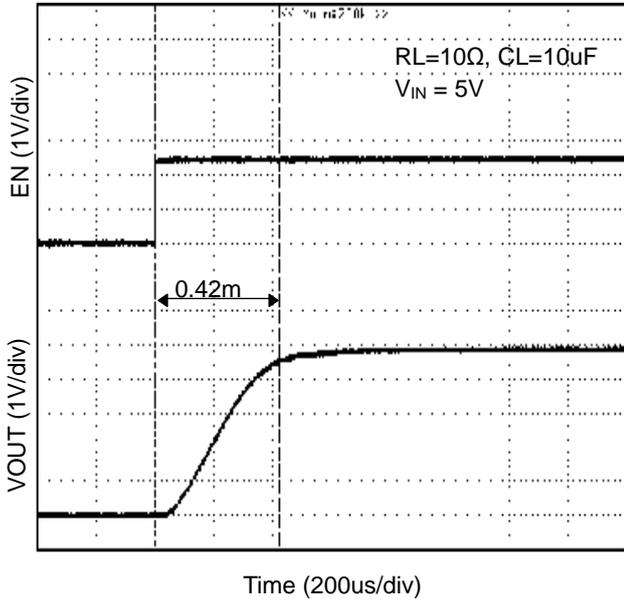


Figure 20. Switch rise time

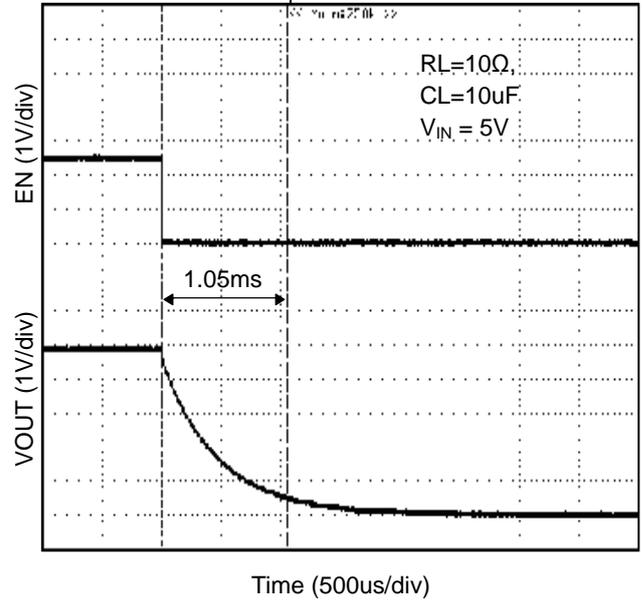


Figure 21. Switch fall time

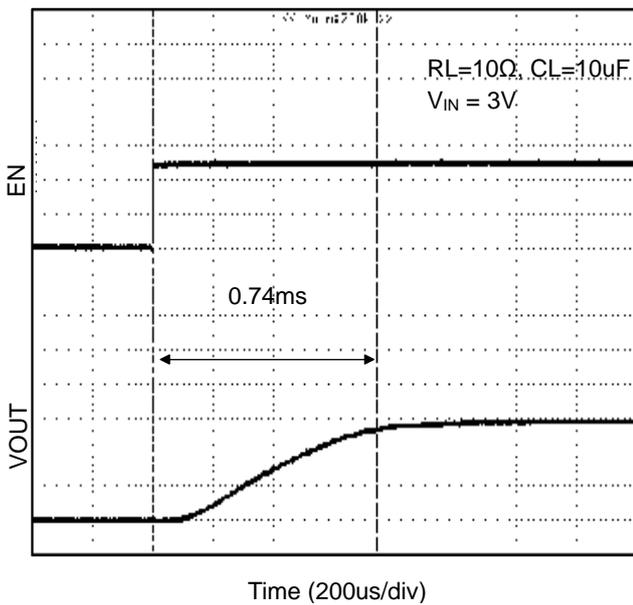


Figure 22. Switch rise time

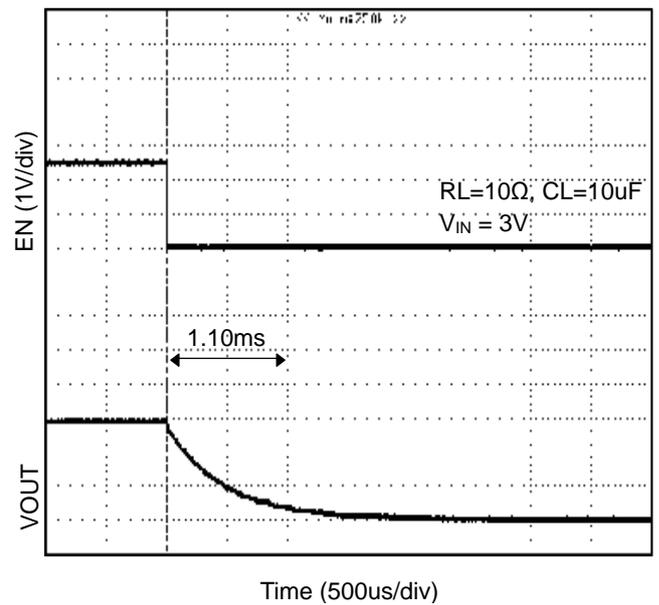


Figure 23. Switch fall time

● Typical Wave Forms – continued

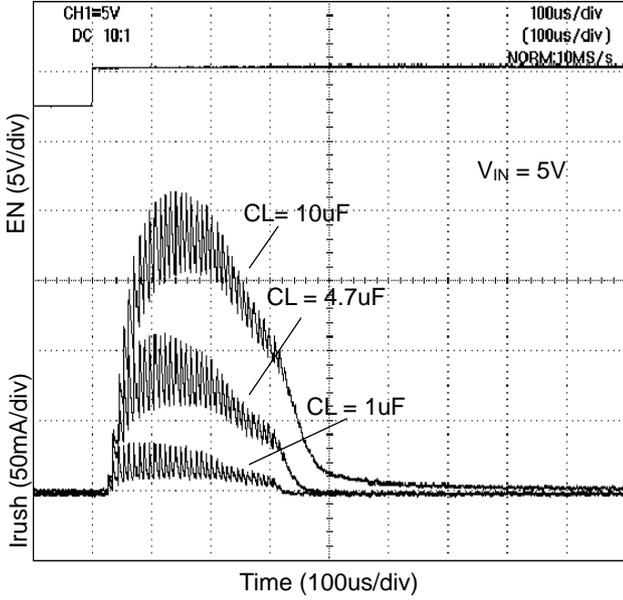


Figure 24. Inrush current

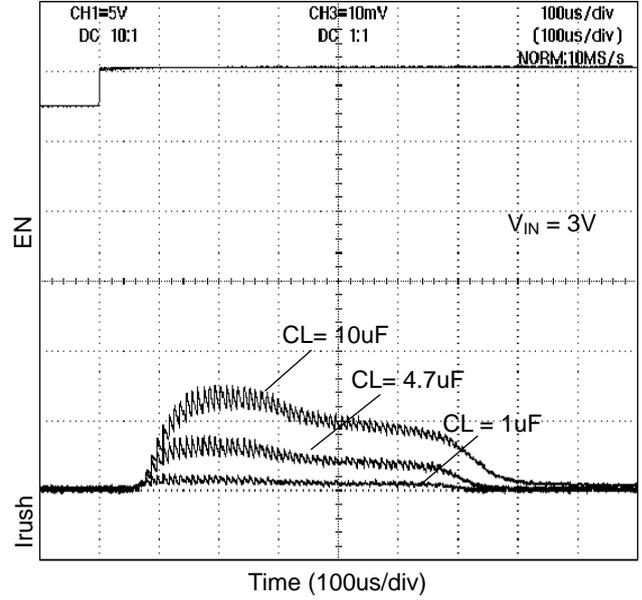


Figure 25. Inrush current

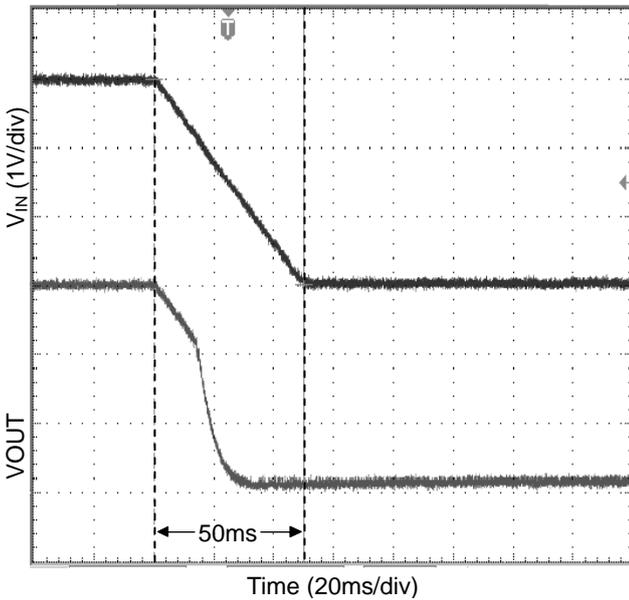


Figure 26. UVLO
CL = 10uF

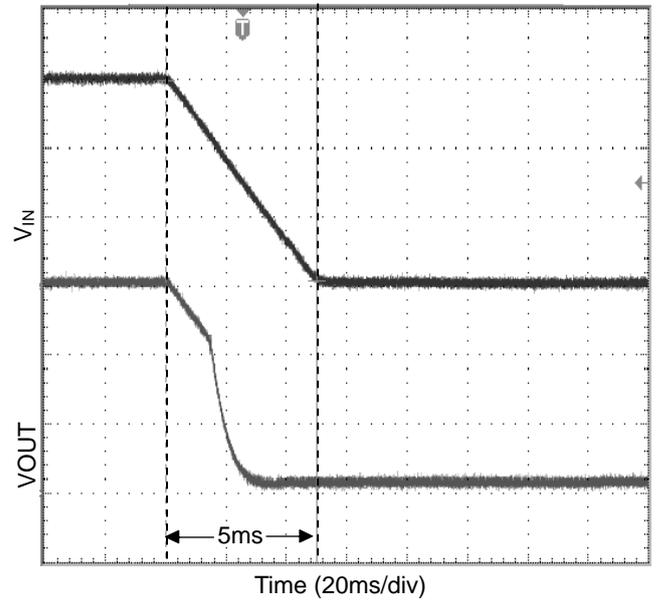
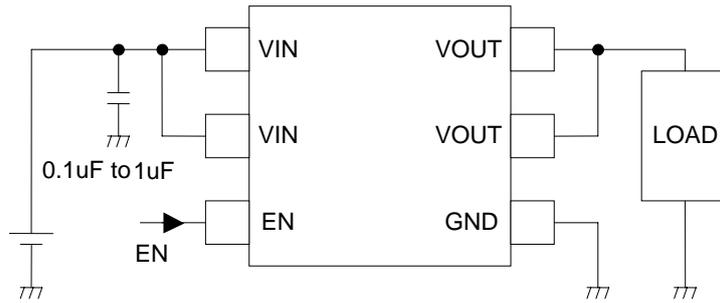


Figure 27. UVLO
CL = 1uF

●Typical Application Circuit



●Functional Description

1. Input / output

VIN pin and VOUT pin are connected to the drain and the source of N-MOS switch respectively. VIN pin is also used as power source input to internal control circuit.

When EN input is set to High level and the switch is turned on, VIN pin and VOUT pin are connected by a 200mΩ switch. In a normal condition, current flows from VIN to VOUT. If voltage of VOUT is higher than VIN, current flows from VOUT to VIN, since the switch is bidirectional. There is no parasitic diode between the drain and the source, so it is possible to prevent current from flowing reversely from VOUT pin to VIN pin when the switch is disabled.

2. Discharge circuit

When the switch between the VIN and the VOUT is OFF, the 200Ω(Typ.) discharge switch between VOUT and GND turns on. By turning on this switch, electric charge at capacitive load is discharged.

3. Under voltage lockout (UVLO)

The UVLO circuit monitors the voltage of the VIN pin, when the EN input is active. UVLO circuit prevents the switch from turning on until the VIN exceeds 2.2V(Typ.). If the VIN drops below 2.1V(Typ.) while the switch turns on, then UVLO shuts off the switch.

While the switch between the VIN pin and VOUT pin is OFF due to UVLO operations, the switch of the discharge circuit turns on. However, when the voltage of VIN declines extremely, then the VOUT pin becomes Hi-Z.

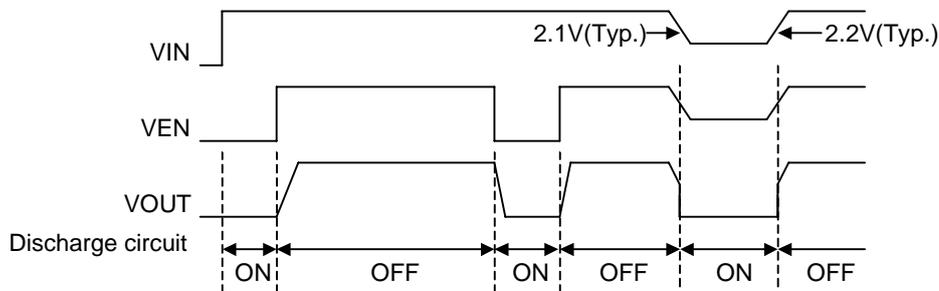


Figure 28. Operation timing

● Power Dissipation

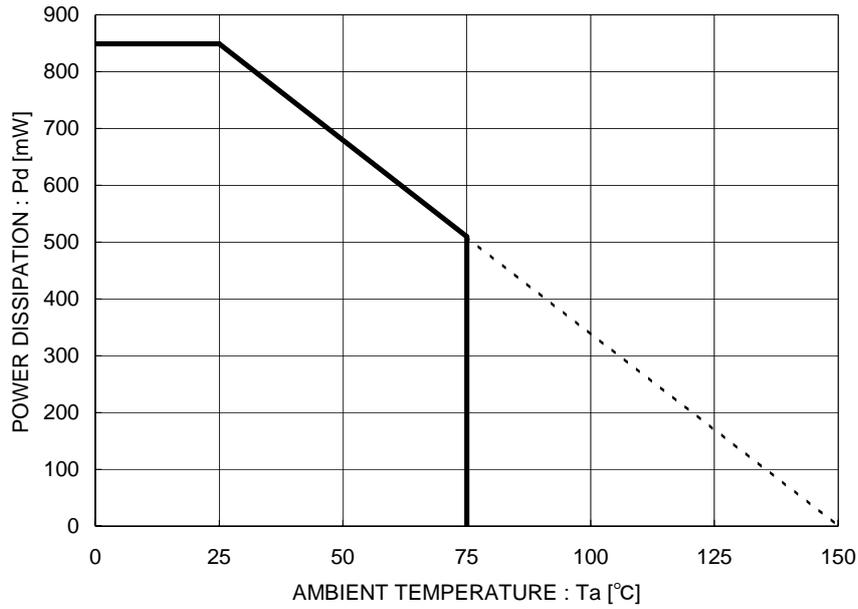
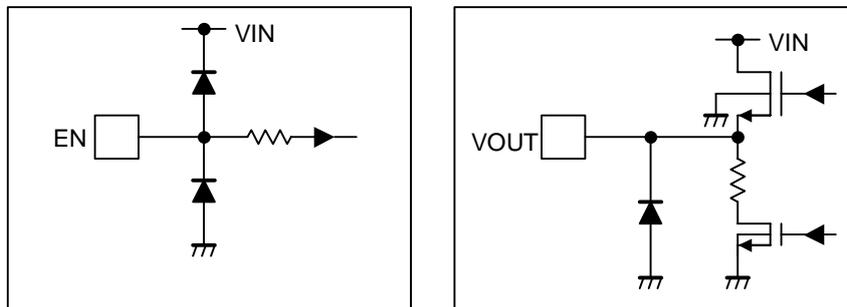


Figure 29. Power dissipation curve (Pd-Ta Curve)
(HVSO6 package)

● I/O Equivalent Circuit



●Operational Notes

(1) Absolute Maximum Ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings

(2) Recommended operating conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power supply line

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between pins and mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7) Operation under strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8) Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

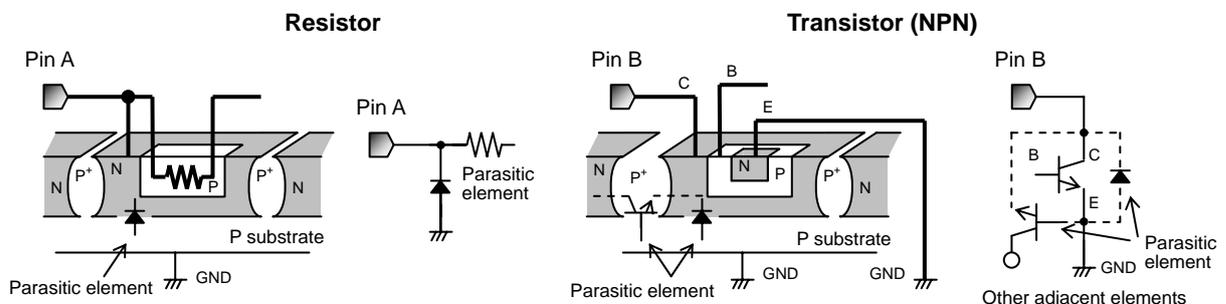
(9) Regarding input pins of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

(10) GND wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) External Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

(13) Thermal consideration

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions ($P_c \geq P_d$).

Package Power dissipation : $P_d (W) = (T_{jmax} - T_a) / \theta_{ja}$

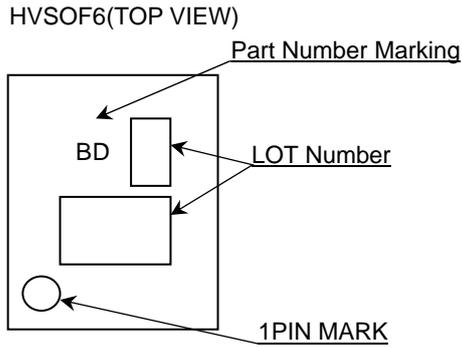
Power dissipation : $P_c (W) = (V_{cc} - V_o) \times I_o + V_{cc} \times I_b$

(T_{jmax} : Maximum junction temperature=150°C, T_a : Peripheral temperature[°C],
 θ_{ja} : Thermal resistance of package-ambience[°C/W], P_d : Package Power dissipation [W],
 P_c : Power dissipation [W], V_{cc} : Input Voltage, V_o : Output Voltage, I_o : Load, I_b : Bias Current)

● Ordering Information



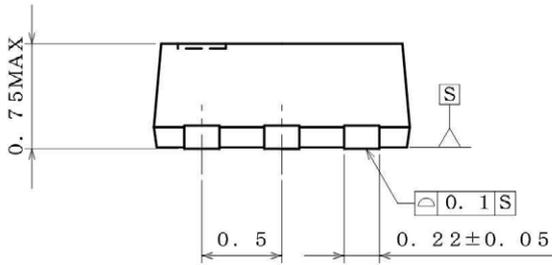
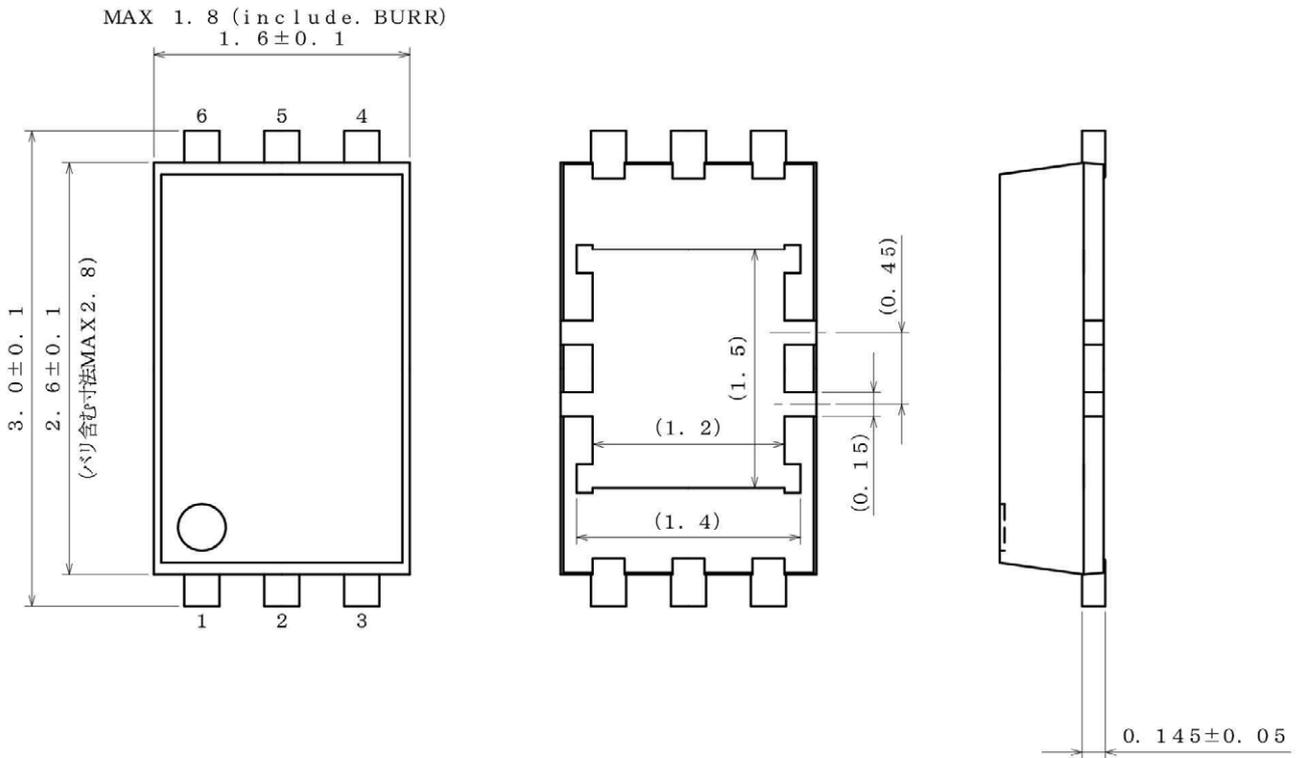
● Marking Diagram



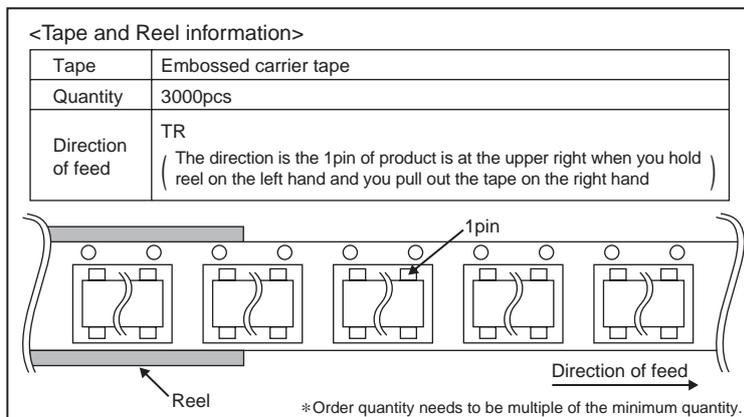
Part Number	Part Number Marking
BD6524HFV	BD

●Physical Dimension, Tape and Reel Information

Package Name	HVSOF6
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(UNIT : mm)
PKG : HVSO6
Drawing No. EX162-5002



●Revision History

Date	Revision	Changes
11.Mar.2013	001	New Release

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
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 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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- 8) Confirm that operation temperature is within the specified range described in the product specification.
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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
- 2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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- 4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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