

October 1987 Revised May 2002

# MM74C90 • MM74C93 4-Bit Decade Counter • 4-Bit Binary Counter

## **General Description**

The MM74C90 decade counter and the MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the  $R_{01},\,R_{02},\,R_{91}$  and  $R_{92}$  inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs  $R_{01}$  and  $R_{02},\,$  and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

All inputs are protected against static discharge damage.

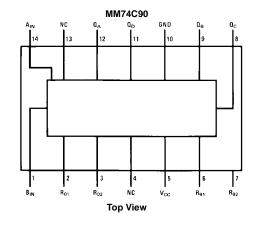
#### **Features**

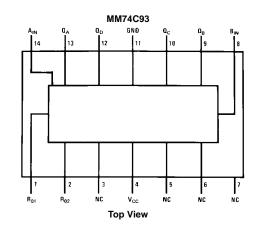
- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V<sub>CC</sub> (typ.)
- Low power compatibility: Fan out of 2 TTL driving 74L
- The MM74C93 follows the MM74L93 Pinout

## **Ordering Code:**

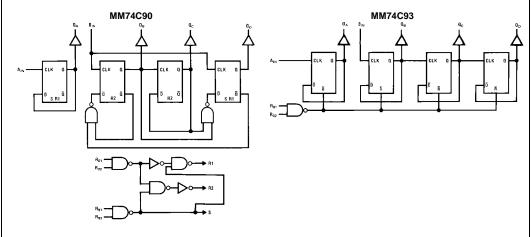
Order Number	Package Number	Package Description
MM74C90N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C93N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

## **Connection Diagrams**





# **Logic Diagrams**



# **Truth Tables**

MM74C90 4-Bit Decade Counter BCD Count Sequence

Count	Output				
	$Q_D$	QC	$Q_B$	$Q_A$	
0	L	L	L	L	
1	L	L	L	Н	
2	L	L	Н	L	
3	L	L	Н	Н	
4	L	Н	L	L	
5	L	Н	L	Н	
6	L	Н	Н	L	
7	L	Н	Н	Н	
8	Н	L	L	L	
9	Н	L	L	Н	

Output  $\mathbf{Q}_{A}$  is connected to Input B for BCD count. H = HIGH Level L = LOW Level X = Irrelevant

MM74C93 4-Bit Binary Counter Binary Count Sequence

Count	Output				
	$Q_D$	QC	$Q_B$	$Q_A$	
0	L	L	L	L	
1	L	L	L	Н	
2	L	L	Н	L	
3	L	L	Н	Н	
4	L	Н	L	L	
5	L	Н	L	Н	
6	L	Н	Н	L	
7	L	Н	Н	Н	
8	Н	L	L	L	
9	Н	L	L	Н	
10	Н	L	Н	L	
11	Н	L	Н	Н	
12	Н	Н	L	L	
13	Н	Н	L	Н	
14	Н	Н	Н	L	
15	Н	Н	Н	Н	

Output  $\mathbf{Q}_A$  is connected to input B for binary count sequence.  $\mathbf{H} = \mathbf{H} (\mathbf{G} \mathbf{H} \ \mathbf{L} \mathbf{e} \mathbf{v} \mathbf{e})$   $\mathbf{L} = \mathbf{L} \mathbf{O} \mathbf{W} \ \mathbf{L} \mathbf{e} \mathbf{v} \mathbf{e}$   $\mathbf{X} = \mathbf{I} \mathbf{r} \mathbf{r} \mathbf{e} \mathbf{e} \mathbf{v} \mathbf{a} \mathbf{t}$ 

# **Function Tables**

## Reset/Count Function Table

Reset Inputs					Out	put		
R <sub>01</sub>	R <sub>02</sub>	R <sub>91</sub>	R <sub>92</sub>	$Q_D$	Q <sub>C</sub>	Q <sub>B</sub>	$Q_A$	
Н	Н	L	Х	L	L	L	L	
Н	Н	X	L	L	L	L	L	
Х	X	Н	Н	Н	L	L	Н	
Х	L	X	L	Count				
L	X	L	Χ	Count				
L	X	X	L	Count				
Х	L	L	Χ	Count				

#### **Reset/Count Function Table**

Reset			Out	put	
Inputs					
R <sub>01</sub>	R <sub>02</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
Н	Н	L	L	L	L
L	X	Count			
Х	L	Count			

## Absolute Maximum Ratings(Note 1)

Voltage at Any Pin (Note 1) -0.3V to V<sub>CC</sub> +0.3V

Operating Temperature Range (T<sub>A</sub>)

Power Dissipation (P<sub>D</sub>)

Dual-In-Line 700 mW
Small Outline 500 mW

 $\begin{array}{ll} \mbox{Operating V}_{\mbox{CC}} \mbox{ Range} & \mbox{3V to 15V} \\ \mbox{Absolute Maximum V}_{\mbox{CC}} & \mbox{18V} \end{array}$ 

Storage Temperature Range (T<sub>S</sub>) -65°C to +150°C

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds) 260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

### **DC Electrical Characteristics**

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Тур	Max	Units
CMOS TO	CMOS		'			
V <sub>IN(1)</sub>	Logical "1" Input Voltage	V <sub>CC</sub> = 5V	3.5			V
		V <sub>CC</sub> = 10V	8.0			V V
V <sub>IN(0)</sub>	Logical "0" Input Voltage	V <sub>CC</sub> = 5V			1.5	V
		V <sub>CC</sub> = 10V			2.0	V V
V <sub>OUT(1)</sub>	Logical "1" Output Voltage	$V_{CC} = 5V, I_{O} = -10 \mu A$	4.5			V
		$V_{CC} = 10V$ , $I_{O} = -10 \mu A$	9.0			V V
V <sub>OUT(0)</sub>	Logical "0" Output Voltage	$V_{CC} = 5V, I_{O} = +10 \mu A$			0.5	V
		$V_{CC} = 10V$ , $I_{O} = +10 \mu A$			1.0	v
I <sub>IN(1)</sub>	Logical "1" Input Current	V <sub>CC</sub> = 15V, V <sub>IN</sub> = 15V		0.005	1.0	μΑ
I <sub>IN(0)</sub>	Logical "0" Input Current	V <sub>CC</sub> = 15V, V <sub>IN</sub> = 0V	-1.0	-0.005		μА
Icc	Supply Current	V <sub>CC</sub> = 15V		0.05	300	μА
CMOS/LP	TTL INTERFACE		'			
V <sub>IN(1)</sub>	Logical "1" Input Voltage					
	MM74C90, MM74C93	V <sub>CC</sub> = 4.75V	V <sub>CC</sub> -1.5			V
V <sub>IN(0)</sub>	Logical "0" Input Voltage					
	MM74C90, MM74C93	V <sub>CC</sub> = 4.75V			0.8	V
V <sub>OUT(1)</sub>	Logical "1" Output Voltage					
	MM74C90, MM74C93	$V_{CC} = 4.75V$ , $I_{O} = -360 \mu A$	2.4			V
V <sub>OUT(0)</sub>	Logical "0" Output Voltage					
	MM74C90, MM74C93	$V_{CC} = 4.75V$ , $I_{O} = -360 \mu A$			0.4	V
OUTPUT I	ORIVE (See Family Characteristics	Data Sheet) (Short Circuit Current)				•
I <sub>SOURCE</sub>	Output Source Current	$V_{CC} = 5V$ , $V_{OUT} = 0V$	-1.75	-3.3		mA
	(P-Channel)	T <sub>A</sub> = 25°C	-1.75	-5.5		IIIA
I <sub>SOURCE</sub>	Output Source Current	V <sub>CC</sub> = 10V, V <sub>OUT</sub> = 0V	-8.0	-15		mA
	(P-Channel)	T <sub>A</sub> = 25°C	-0.0	-13		IIIA
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 5V$ , $V_{OUT} = V_{CC}$	1.75	3.6		mA
	(N-Channel)	$T_A = 25^{\circ}C$	1.75	3.0		IIIA
I <sub>SINK</sub>	Output Sink Current	$V_{CC} = 10V$ , $V_{OUT} = V_{CC}$	8.0	16		mA
	(N-Channel)	T <sub>A</sub> = 25°C	6.0	10		IIIA

# AC Electrical Characteristics (Note 2)

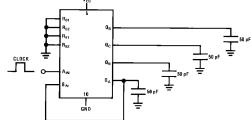
Symbol	Parameter	Conditions	Min	Тур	Max	Units
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time	V <sub>CC</sub> = 5V		200	400	
	from A <sub>IN</sub> to Q <sub>A</sub>	V <sub>CC</sub> = 10		80	150	ns
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		450	850	ns
	A <sub>IN</sub> to Q <sub>B</sub> (MM74C93)	V <sub>CC</sub> = 10V		160	300	
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		450	800	ns
	A <sub>IN</sub> to Q <sub>B</sub> (MM74C90)	V <sub>CC</sub> = 10V		160	300	
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time	V <sub>CC</sub> = 5V		500	1050	
	from A <sub>IN</sub> to Q <sub>C</sub> (MM74C93)	V <sub>CC</sub> = 10		200	400	ns
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		500	1000	
	A <sub>IN</sub> to Q <sub>C</sub> (MM74C93)	V <sub>CC</sub> = 10V		200	400	ns
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		600	1200	
	A <sub>IN</sub> to Q <sub>D</sub> (MM74C93)	V <sub>CC</sub> = 10V		250	500	ns
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		450	800	ne
	A <sub>IN</sub> to Q <sub>D</sub> (MM74C90)	V <sub>CC</sub> = 10V		160	300	ns
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	V <sub>CC</sub> = 5V		150	300	no
	$R_{01}$ or $R_{02}$ to $Q_A$ , $Q_B$ , $Q_C$ or $Q_D$	V <sub>CC</sub> = 10V		75	150	ns
	(MM74C93)					
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	me from V <sub>CC</sub> = 5V		200	400	ns
	$R_{01}$ or $R_{02}$ to $Q_A$ , $Q_B$ , $Q_C$ or $Q_D$	V <sub>CC</sub> = 10V		75	150	
	(MM74C90)					
t <sub>pd0</sub> , t <sub>pd1</sub>	Propagation Delay Time from	$V_{CC} = 5V$		250	500	ns
	R <sub>91</sub> or R <sub>92</sub> to Q <sub>A</sub> or Q <sub>D</sub>	V <sub>CC</sub> = 10V		100	200	113
	(MM74C90)					
t <sub>PW</sub>	Min. R <sub>01</sub> or R <sub>02</sub> Pulse Width	$V_{CC} = 5V$	600	250		ns
	(MM74C93)	V <sub>CC</sub> = 10V	30	125		113
t <sub>PW</sub>	Min. R <sub>01</sub> or R <sub>02</sub> Pulse Width	V <sub>CC</sub> = 5V	600	250		ns
	(MM74C90)	V <sub>CC</sub> = 10V	300	125		113
t <sub>PW</sub>	Min. R <sub>91</sub> or R <sub>92</sub> Pulse Width	$V_{CC} = 5V$	500	200		ns
	(MM74C90)	V <sub>CC</sub> = 10V	250	100		110
$t_r$ , $t_f$	Maximum Clock Rise	V <sub>CC</sub> = 10V			15	μs
	and Fall Time	V <sub>CC</sub> = 10V			5	μο
t <sub>W</sub>	Minimum Clock Pulse Width	V <sub>CC</sub> = 5V	250	100		ns
		V <sub>CC</sub> = 10V	100	50		110
f <sub>MAX</sub>	Maximum Clock Frequency	V <sub>CC</sub> = 5V	2			MHz
		V <sub>CC</sub> = 10V	5			1711 12
C <sub>IN</sub>	Input Capacitance	Any Input (Note 3)		5		pF
C <sub>PD</sub>	Power Dissipation Capacitance	Per Package (Note 4)		45		pF

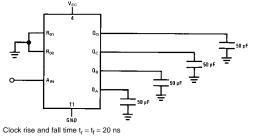
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C<sub>PD</sub> determines the no load ac power consumption of any CMOS device. For complete explanation see Family Characteristics application note—AN-90.

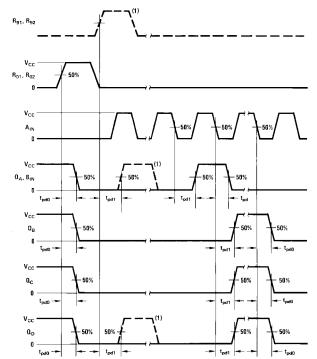
# AC Test Circuits MM74C90 MM74C93





# **Switching Time Waveforms**

Clock rise and fall time  $t_{\rm r}=t_{\rm f}=20~{\rm ns}$ 



MM74C90 and MM74C93 are solid line waveforms. Dashed line waveforms are for MM74C90 only.

#### Physical Dimensions inches (millimeters) unless otherwise noted 0.740 - 0.770 (18.80 - 19.56)(2.286) 14 13 12 11 10 9 8 14 13 12 $0.250 \pm 0.010$ (6.350 ± 0.254) PIN NO. 1 1 2 3 4 5 6 1 2 3 IDENT $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 02 OPTION 1 $0.135 \pm 0.005$ 0.300 - 0.320 $(3.429 \pm 0.127)$ (7.620 - 8.128)0.065 0.145 - 0.200 0.060 4° TYP Optional (1.651) (3.683 - 5.080)(1.524)0.008 - 0.016 TYP 95° ± 5° 0.020 (0.203 - 0.406)(0.508) MIN 0.125 - 0.150 $0.075 \pm 0.015$ (3.175 - 3.810)0.280 $(1.905 \pm 0.381)$ (7.112) MIN 0.014 - 0.023TYP $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)} \text{ TYP}$ 0.325 <sup>+0.040</sup> -0.015 $8.255 + 1.016 \\ -0.381$

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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N14A (REV F)