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Team Nexperia

# PMF370XN

## N-channel TrenchMOS extremely low level FET

Rev. 03 — 20 June 2008 | Product data sheet

# 1. Product profile

## 1.1 General description

Extremely low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

## 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Saves PCB space due to small footprint (40 % smaller than SOT23)
- Surface-mounted package
- Low threshold voltage
- Suitable for low gate drive sources

## 1.3 Applications

- Driver circuits
- Switching in portable appliances

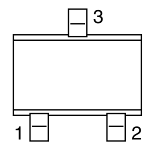
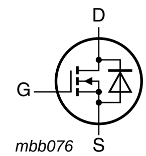
## 1.4 Quick reference data

**Table 1. Quick reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | - | 30 | V |
| $I_D$ | drain current | $T_{sp} = 25$ °C; $V_{GS} = 4.5$ V; see Figure 1 and 3 | - | - | 0.87 | A |
| $P_{tot}$ | total power dissipation | $T_{sp} = 25$ °C; see Figure 2 | - | - | 0.56 | W |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 4.5$ V; $I_D = 0.2$ A; $T_j = 25$ °C; see Figure 9 and 10 | - | 370 | 440 | mΩ |

## 2. Pinning information

**Table 2. Pinning**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |   SOT323 (SC-70) |   |
| 2 | S | source | | |
| 3 | D | drain | | |

## 3. Ordering information

**Table 3. Ordering information**

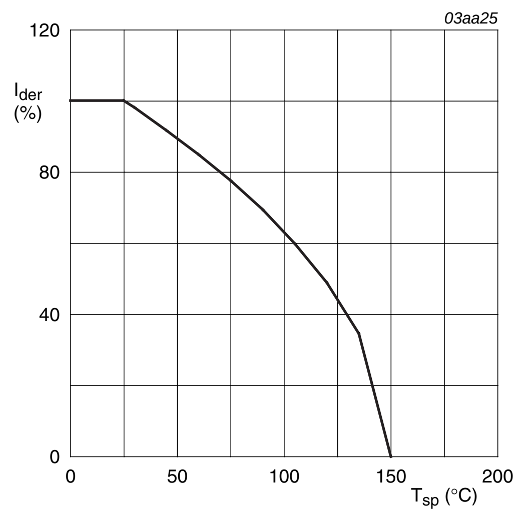
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PMF370XN | SC-70 | plastic surface-mounted package; 3 leads | SOT323 |

## 4. Limiting values

**Table 4. Limiting values**

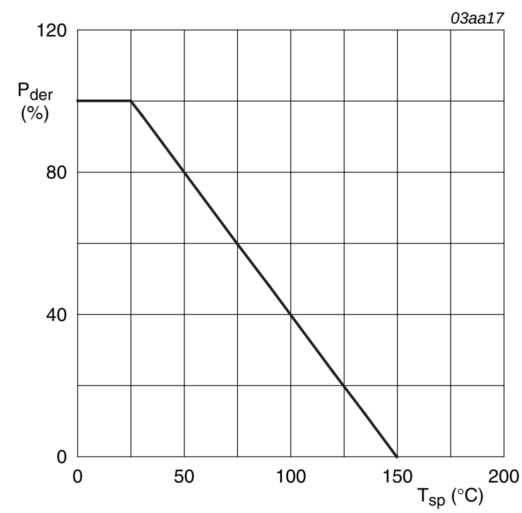
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \leq 150$ °C; $T_j \geq 25$ °C; $R_{GS} = 20$ kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | -12 | 12 | V |
| $I_D$ | drain current | $T_{sp} = 25$ °C; $V_{GS} = 4.5$ V; see Figure 1 and 3 | - | 0.87 | A |
| | | $T_{sp} = 100$ °C; $V_{GS} = 4.5$ V; see Figure 1 | - | 0.55 | A |
| $I_{DM}$ | peak drain current | $T_{sp} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3 | - | 1.74 | A |
| $P_{tot}$ | total power dissipation | $T_{sp} = 25$ °C; see Figure 2 | - | 0.56 | W |
| $T_{stg}$ | storage temperature | | -55 | 150 | °C |
| $T_j$ | junction temperature | | -55 | 150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source current | $T_{sp} = 25$ °C | - | 0.47 | A |
| $I_{SM}$ | peak source current | $T_{sp} = 25$ °C; $t_p \leq 10$ µs; pulsed | - | 0.94 | A |



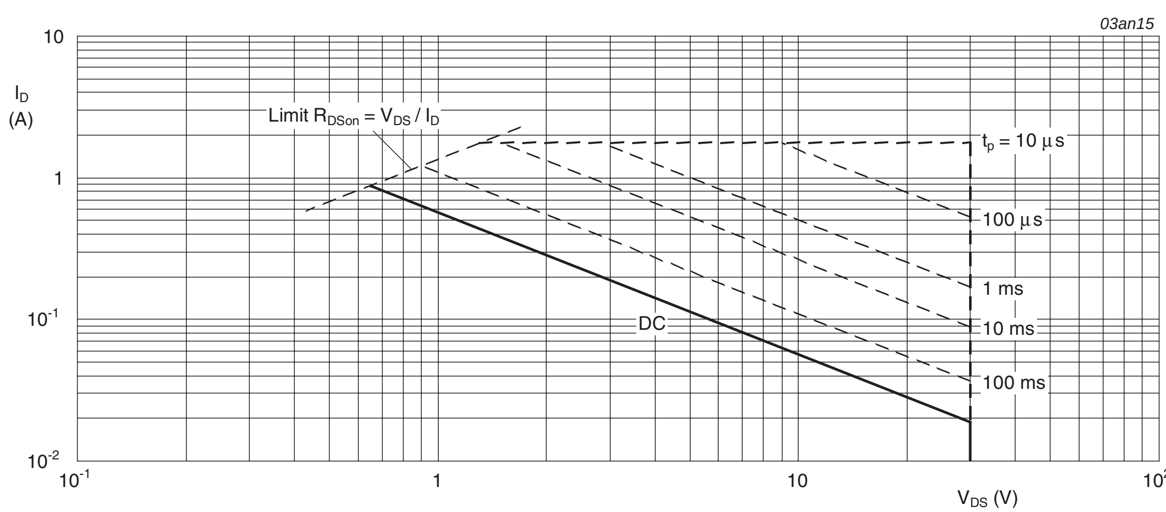

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**




$T_{sp} = 25°C$; $I_{DM}$ is single pulse; $V_{GS} = 4.5V$

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

# 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see Figure 4 | - | - | 220 | K/W |

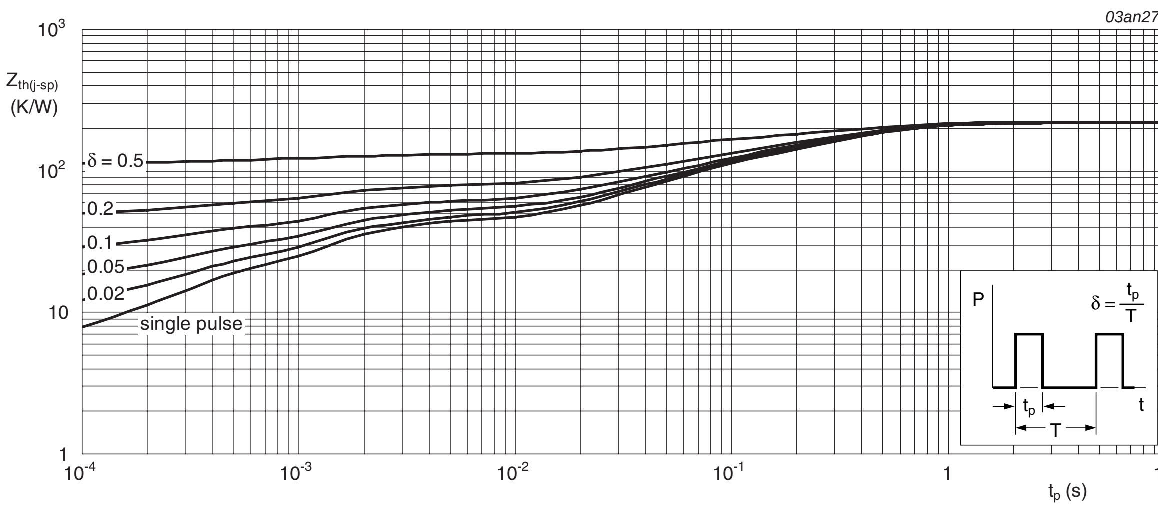



Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

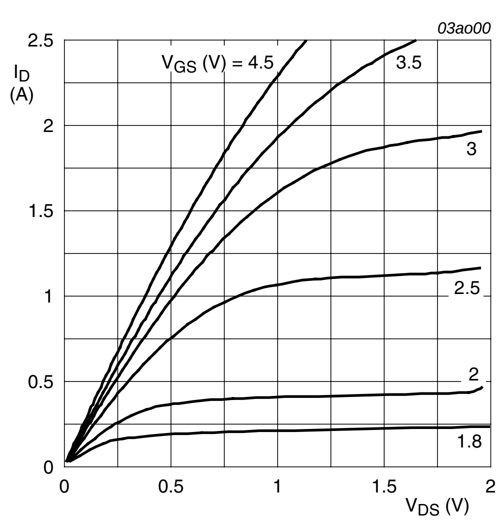
# 6. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 1 μA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 27 | - | - | V |
| | | $I_D$ = 1 μA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 30 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 7 | - | - | 1.8 | V |
| | | $I_D$ = 0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C; see Figure 7 and 8 | 0.35 | - | - | V |
| | | $I_D$ = 0.25 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 7 and 8 | 0.5 | 1 | 1.5 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | - | 1 | μA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 70 °C | - | - | 2 | μA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C | - | - | 10 | μA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 12 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |
| | | $V_{GS}$ = -12 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 10 | 100 | nA |

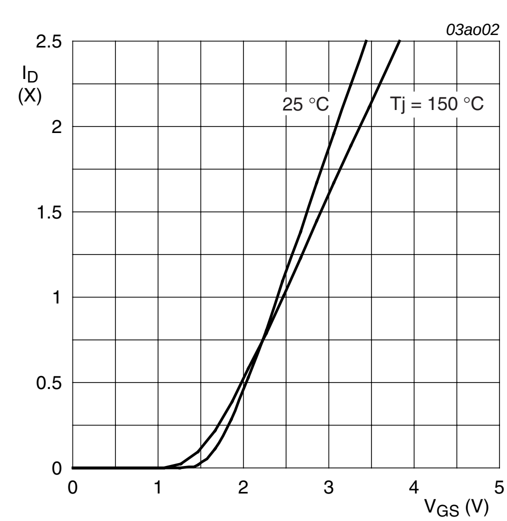
**Table 6. Characteristics** *...continued*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 2.5 V; $I_D$ = 0.1 A; $T_j$ = 25 °C; see Figure 9 and 10 | - | 550 | 650 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 0.2 A; $T_j$ = 150 °C; see Figure 10 | - | 629 | 748 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 0.2 A; $T_j$ = 25 °C; see Figure 9 and 10 | - | 370 | 440 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 1 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C; see Figure 11 and 12 | - | 0.65 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 0.14 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 0.18 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 13 | - | 37 | - | pF |
| $C_{oss}$ | output capacitance | | - | 8.5 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 5.5 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $R_{G(ext)}$ = 6 Ω; $R_L$ = 15 Ω; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; $T_j$ = 25 °C | - | 6.5 | - | ns |
| $t_r$ | rise time | | - | 9.5 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 14 | - | ns |
| $t_f$ | fall time | | - | 5.5 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 0.3 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 14 | - | 0.81 | 1.2 | V |



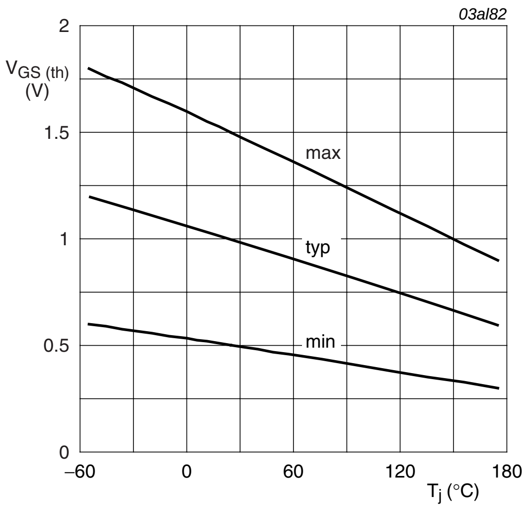

$T_j$ = 25°C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



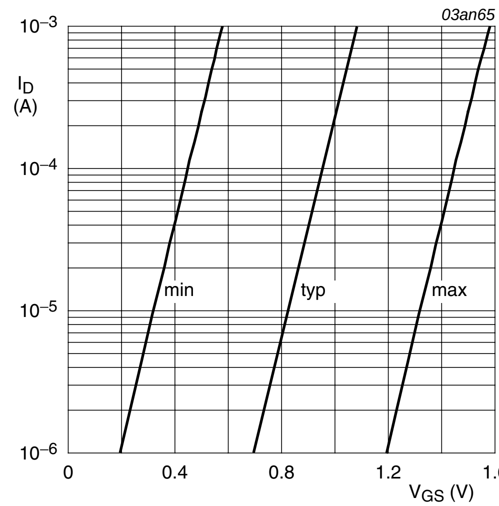

$T_j$ = 25°C and 150°C; $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



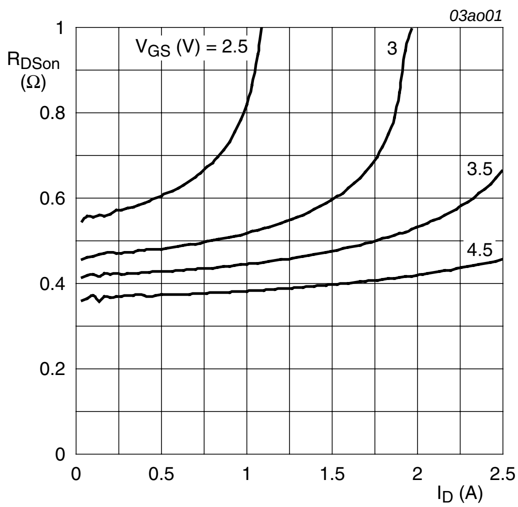

$I_D = 0.25A; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



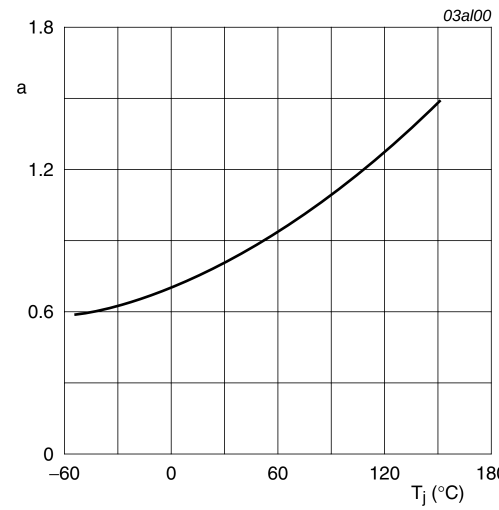

$T_j = 25°C; V_{DS} = 5V$

**Fig 8. Subthreshold drain current as a function of gate-source voltage**




$T_j = 25°C$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**

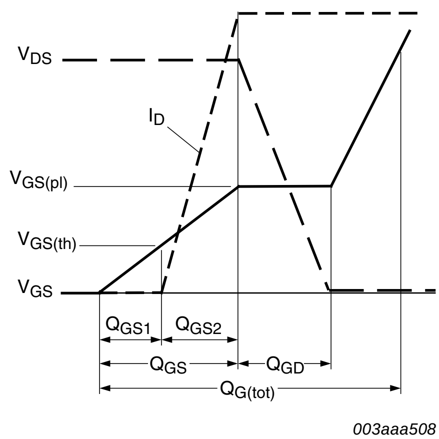
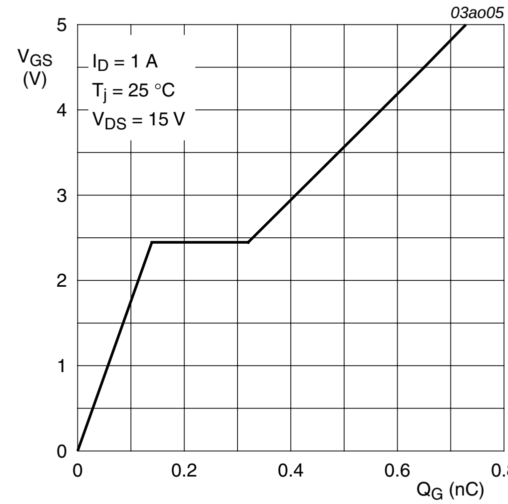
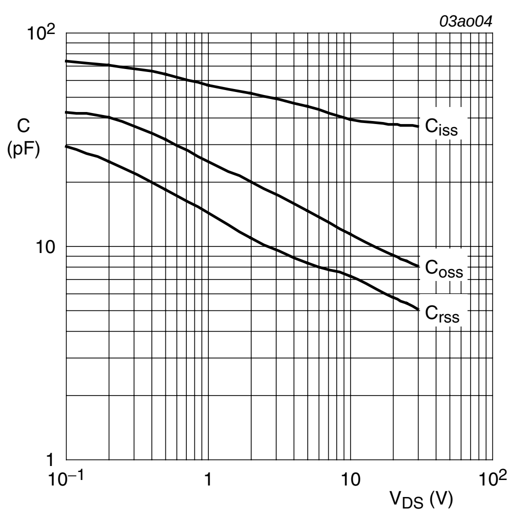



**Fig 11. Gate charge waveform definitions**



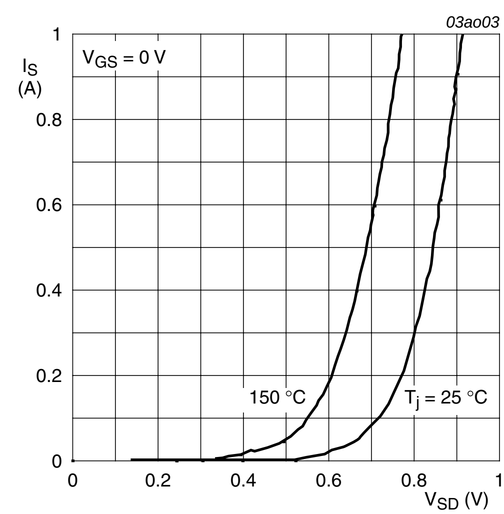

$I_D = 1A; V_{DS} = 15V$

**Fig 12. Gate-source voltage as a function of gate charge; typical values**




$V_{GS} = 0V;\ f = 1MHz$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

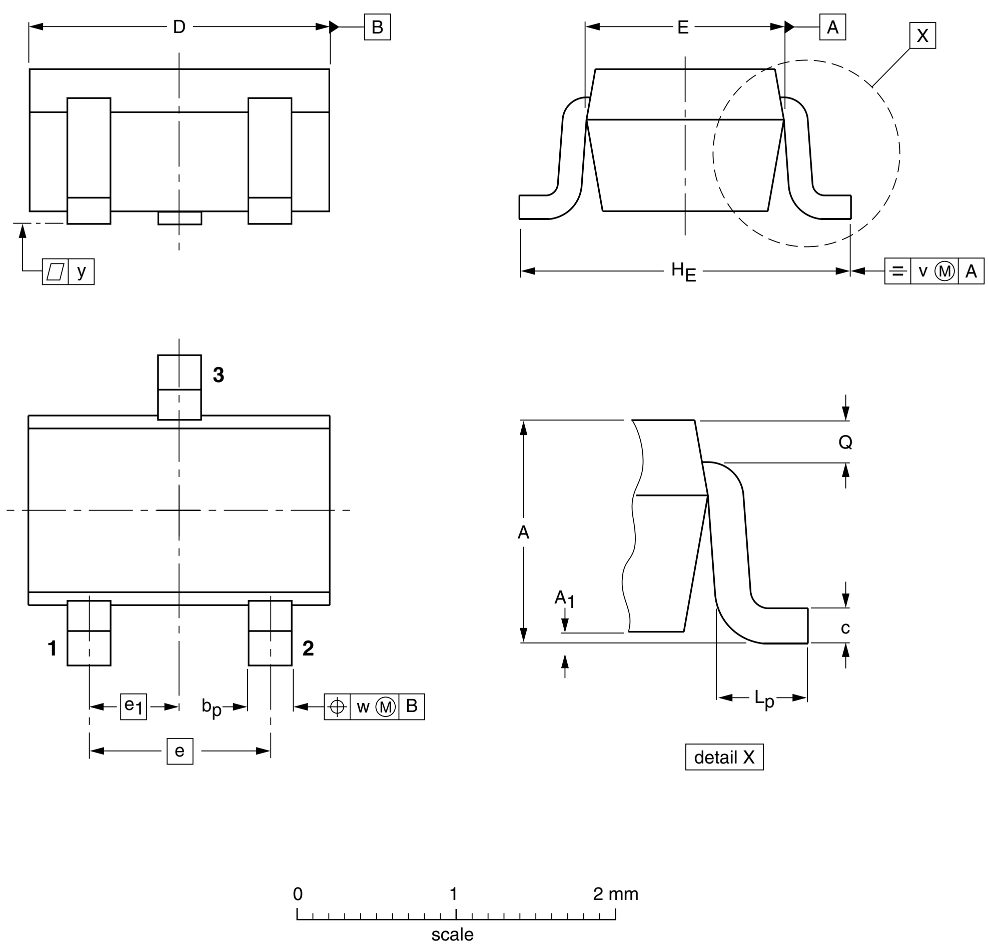



$T_j = 25°C$ and $150°C; V_{GS} = 0V$

**Fig 14. Source current as a function of source-drain voltage; typical values**

# 7. Package outline

**Plastic surface-mounted package; 3 leads** **SOT323**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.8 | 0.1 | 0.4<br>0.3 | 0.25<br>0.10 | 2.2<br>1.8 | 1.35<br>1.15 | 1.3 | 0.65 | 2.2<br>2.0 | 0.45<br>0.15 | 0.23<br>0.13 | 0.2 | 0.2 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT323 | | | SC-70 | | | ~~04-11-04~~<br>06-03-16 |

**Fig 15. Package outline SOT323 (SC-70)**

## 8. Soldering

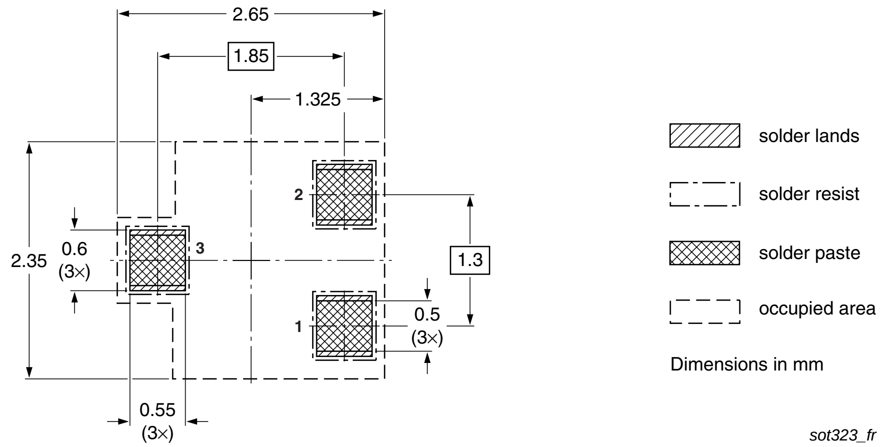



**Fig 16. SOT323 (SC-70)**

# 9. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PMF370XN_3 | 20080620 | Product data sheet | - | PMF370XN_2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate | | | |
| PMF370XN_2 | 20051206 | Product data sheet | - | PMF370XN-01 |
| PMF370XN-01 | 20040211 | Product data sheet | - | - |

# 10. Legal information

## 10.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 12. Contents





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**Date of release: 20 June 2008**

**Document identifier: PMF370XN_3**