AOD2610E/AOI2610E/AOY2610E

60V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- Low Eoss
- ESD protected
- RoHS and Halogen-Free Compliant

Applications

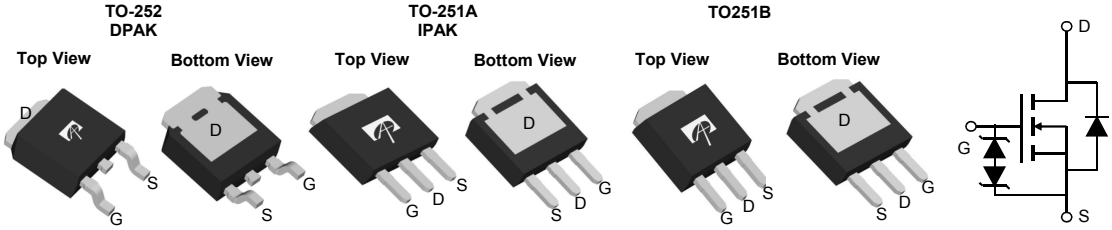
- High efficiency power supply
- Secondary synchronus rectifier

Product Summary

V_{DS}	60V
I_D (at V_{GS}=10V)	46A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 9.5mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 13.3mΩ
Typical ESD protection	**HBM Class 2**

100% UIS Tested
100% Rg Tested

Green Product



AOD2610E AOI2610E AOY2610E

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD2610E	TO-252	Tape & Reel	2500
AOI2610E	TO-251A	Tube	4000
AOY2610E	TO-251B	Tube	4000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	46	A
	T_C=100°C		36.5	
Pulsed Drain Current [C]		I_{DM}	110	
Continuous Drain Current	T_A=25°C	I_{DSM}	19	A
	T_A=70°C		15	
Avalanche Current [C]		I_{AS}	17	A
Avalanche energy	L=0.3mH [C]	E_{AS}	43	mJ
V_{DS} Spike [I]	10µs	V_{SPIKE}	72	V
Power Dissipation [B]	T_C=25°C	P_D	59.5	W
	T_C=100°C		23.5	
Power Dissipation [A]	T_A=25°C	P_{DSM}	6.2	W
	T_A=70°C		4.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.7	2.1	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	1.4	1.8	2.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		7.7	9.5	mΩ
		T_J=125°C		12.5	15.5	
		V_{GS}=4.5V, I_D=20A		10.3	13.3	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		52		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.72	1	V
I_S	Maximum Body-Diode Continuous Current [G]				46	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		1100		pF
C_{oss}	Output Capacitance			300		pF
C_{rss}	Reverse Transfer Capacitance			28		pF
R_g	Gate resistance	f=1MHz	0.6	1.2	2.0	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A		14.5	25	nC
Q_g(4.5V)	Total Gate Charge			7	13	nC
Q_{gs}	Gate Source Charge			2.5		nC
Q_{gd}	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=1.5Ω, R_{GEN}=3Ω		6.5		ns
t_r	Turn-On Rise Time			3.5		ns
$t_{D(off)}$	Turn-Off DelayTime			22		ns
t_f	Turn-Off Fall Time			3		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs		19		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs		65		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
I. The spike duty cycle 5% max, limited by junction temperature TJ(MAX)=125° C.

APPLICATIONS OR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

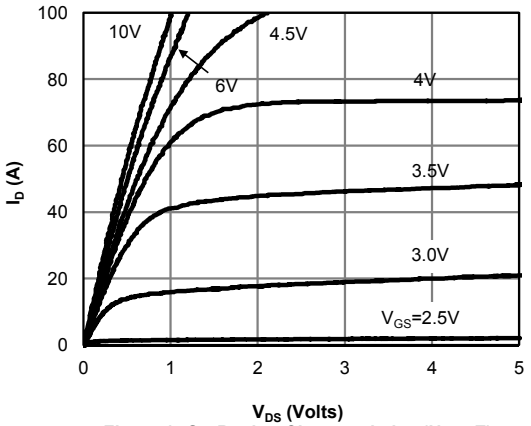


Figure 1: On-Region Characteristics (Note E)

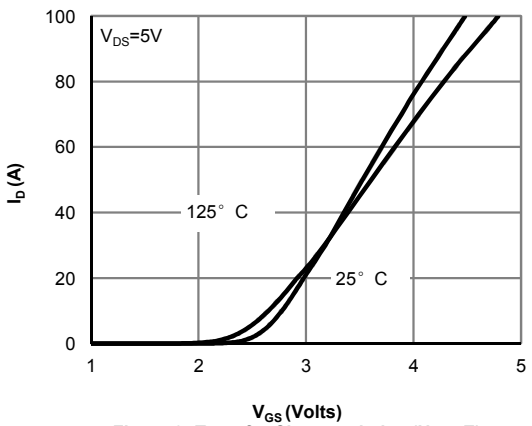


Figure 2: Transfer Characteristics (Note E)

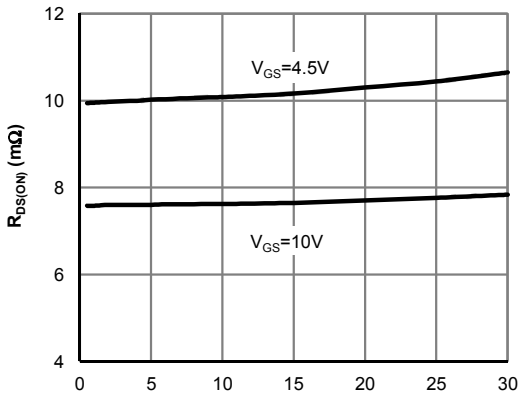


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

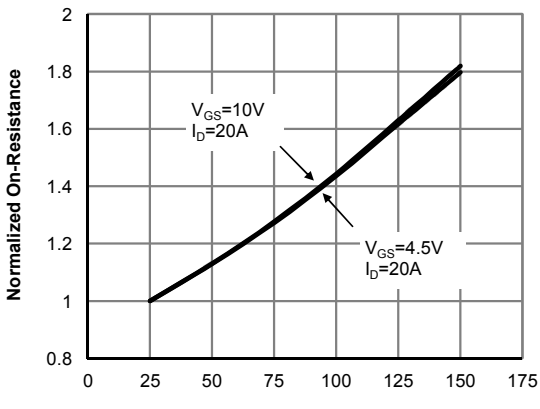


Figure 4: On-Resistance vs. Junction Temperature (Note E)

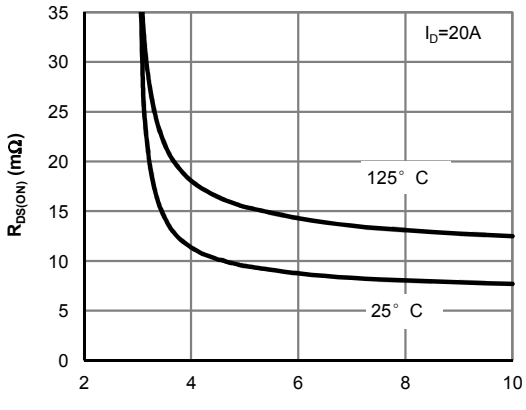


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

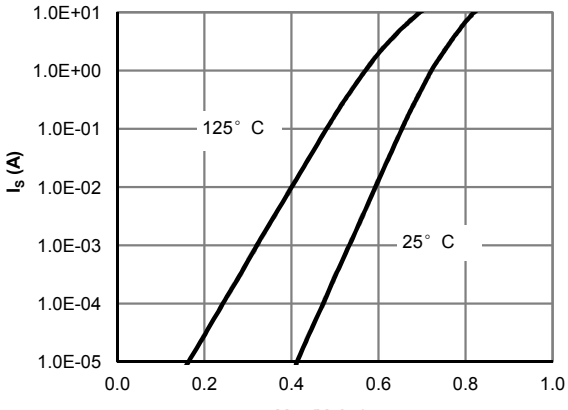


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

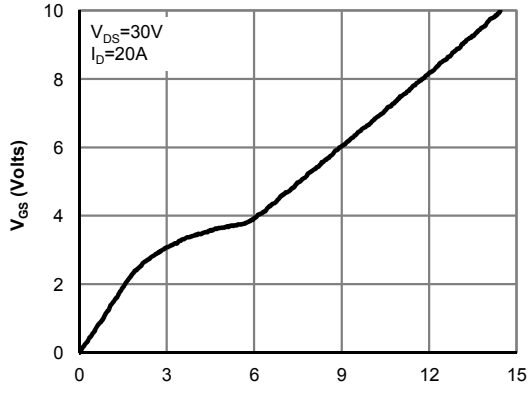


Figure 7: Gate-Charge Characteristics

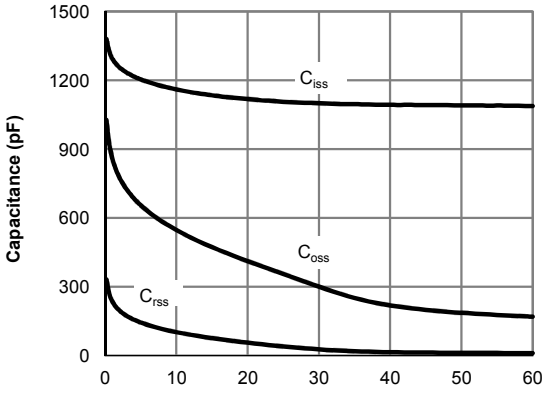


Figure 8: Capacitance Characteristics

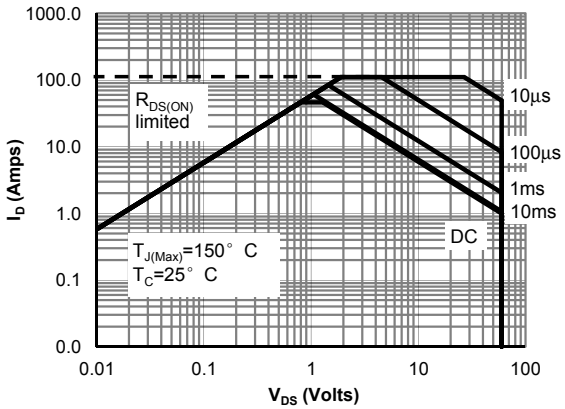


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

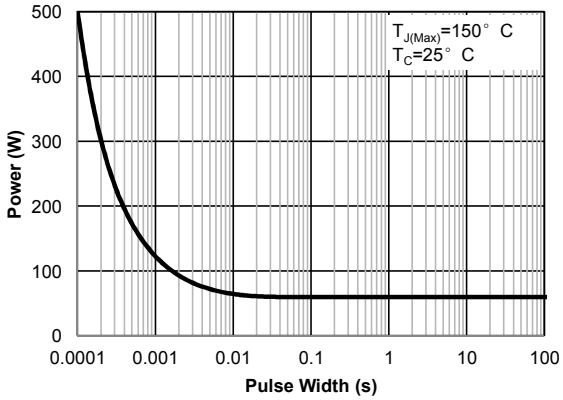


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

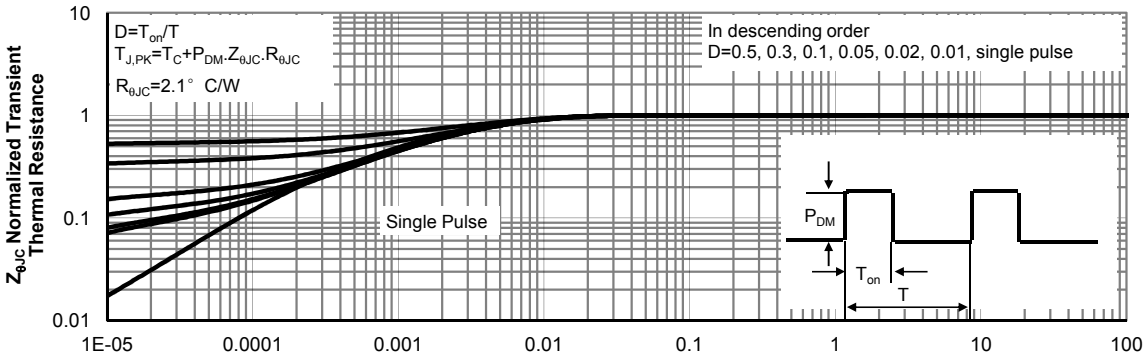


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

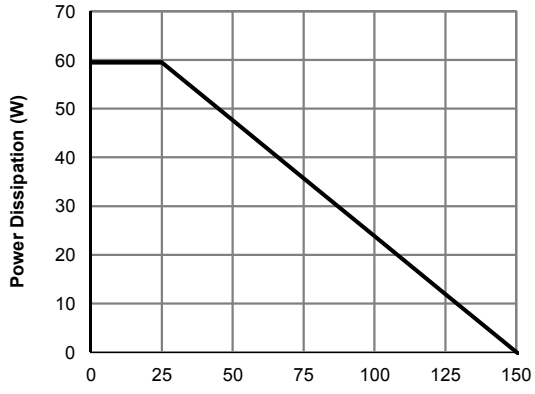


Figure 12: Power De-rating (Note F)

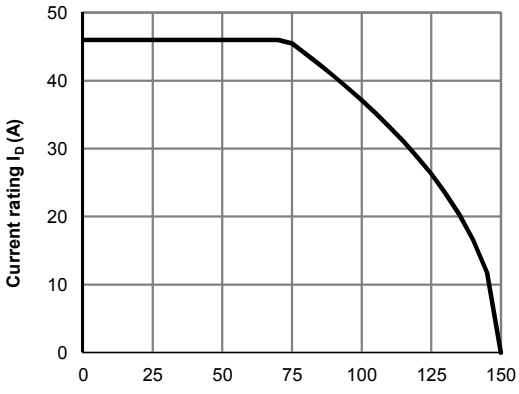


Figure 13: Current De-rating (Note F)

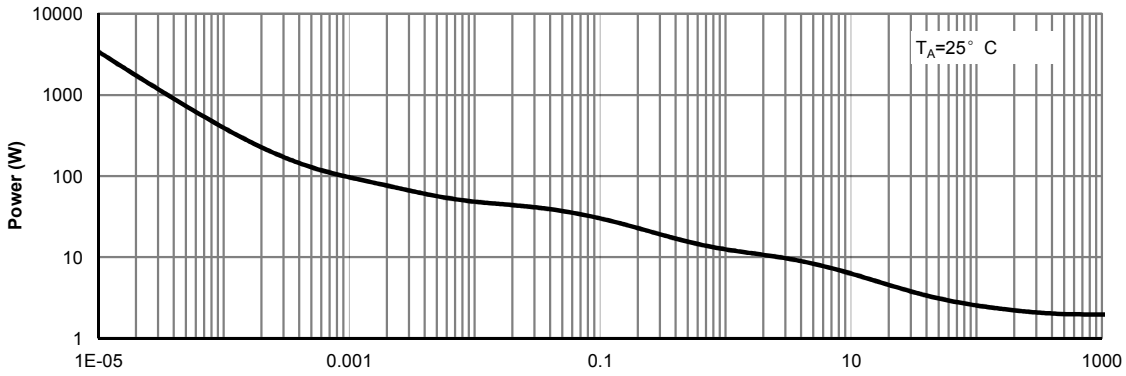


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

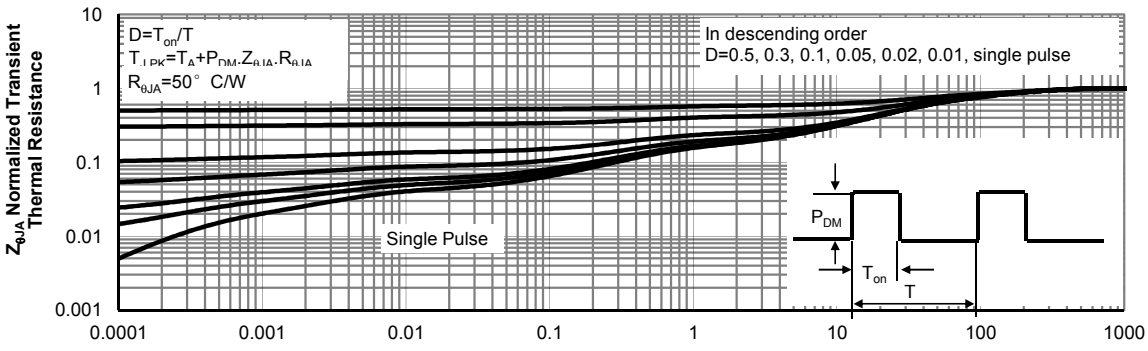


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

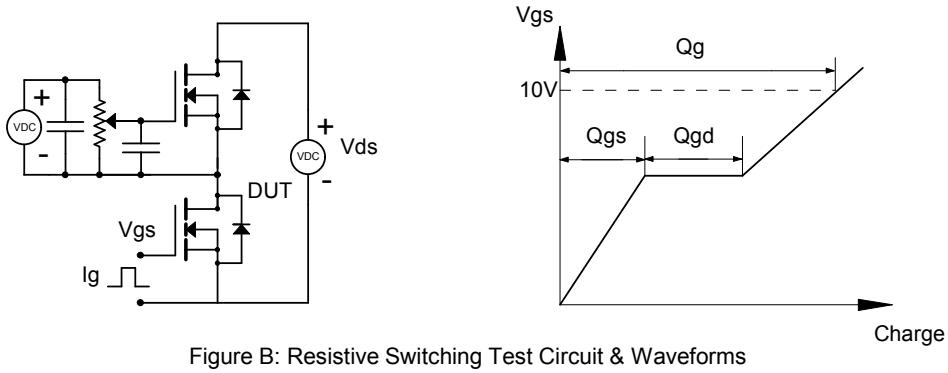


Figure B: Resistive Switching Test Circuit & Waveforms

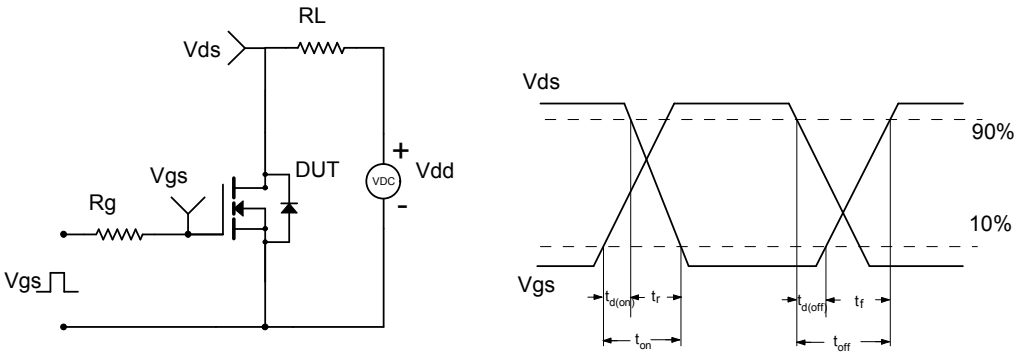


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

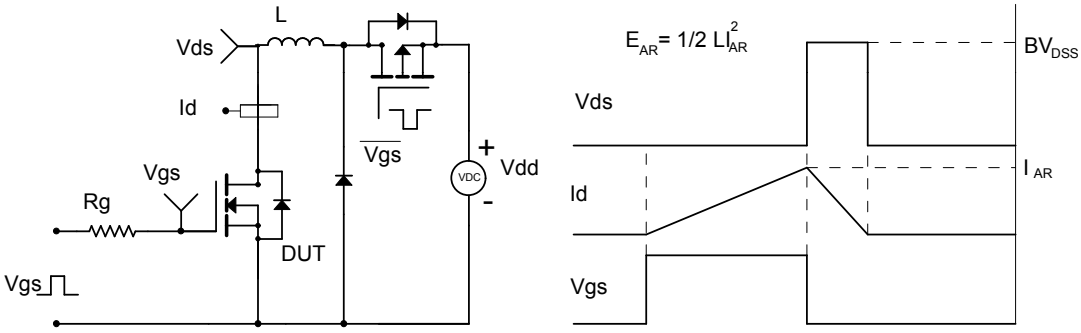


Figure D: Diode Recovery Test Circuit & Waveforms