BLC10G22XS-301AVT

Power LDMOS transistor

AMPLEON

Rev. 1 — 30 April 2020

Product data sheet

1. Product profile

1.1 General description

300 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2110 MHz to 2170 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 1.15 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2110 to 2170	30	47	16	47	–30 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

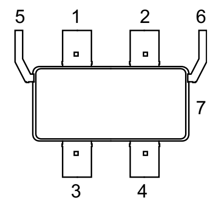
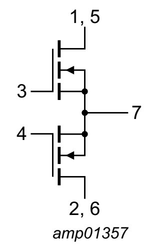
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2110 MHz to 2170 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G22XS-301AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 1.15 V; T_{case} = 80 °C		
		P_L = 50 W	0.27	K/W
		P_L = 80 W	0.22	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 90 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 540 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	17	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.15 A	-	9	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 3.15 A	-	144	243	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.9 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 190 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1140 mA	-	2.2	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	34	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 6.65 A	-	18.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 6.65 A	-	69	121	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2167.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 1.1 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 2110 MHz to 2170 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 52 W	13.8	15	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 52 W	-	–15	–9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 52 W	43	48	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 52 W	-	–26	–21	dBc

Table 8. RF characteristics

Test signal: pulsed CW; t_p = 100 μs; δ = 10 %; f_1 = 2110 MHz; f_2 = 2170 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V (typical); T_{case} = 25 °C; unless otherwise specified; in a Doherty production RF test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	-	280	350	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G22XS-301AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V; f = 2110 MHz; P_L = 180 W; CW.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 540 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
2110	14.2 + j8.4	3.4 – j5.8	131	57.7	20.2
2140	7.8 + j8.6	3.4 – j5.8	125	57.6	20.3
2170	4.7 + j6.5	3.6 – j6.3	135	59.4	20.0
Maximum drain efficiency load					
2110	14.2 + j8.4	3.6 – j3.4	97	64.3	18.7
2140	7.8 + j8.6	3.9 – j3.7	97	63.6	18.9
2170	4.7 + j6.5	3.6 – j3.4	92	66.6	18.7

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1100 mA (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
2110	4.0 – j11.0	4.2 – j6.1	265	62.7	17.1
2140	4.7 – j11.0	4.4 – j6.7	268	61.9	17.1
2170	5.9 – j12.0	4.6 – j7.4	262	59.4	17.1
Maximum drain efficiency load					
2110	4.0 – j11.0	5.4 – j4.5	218	66.3	14.9
2140	4.7 – j11.0	5.0 – j4.1	204	66.4	15.1
2170	5.9 – j12.0	5.0 – j5.0	217	65.0	15.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

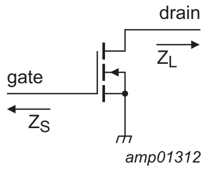
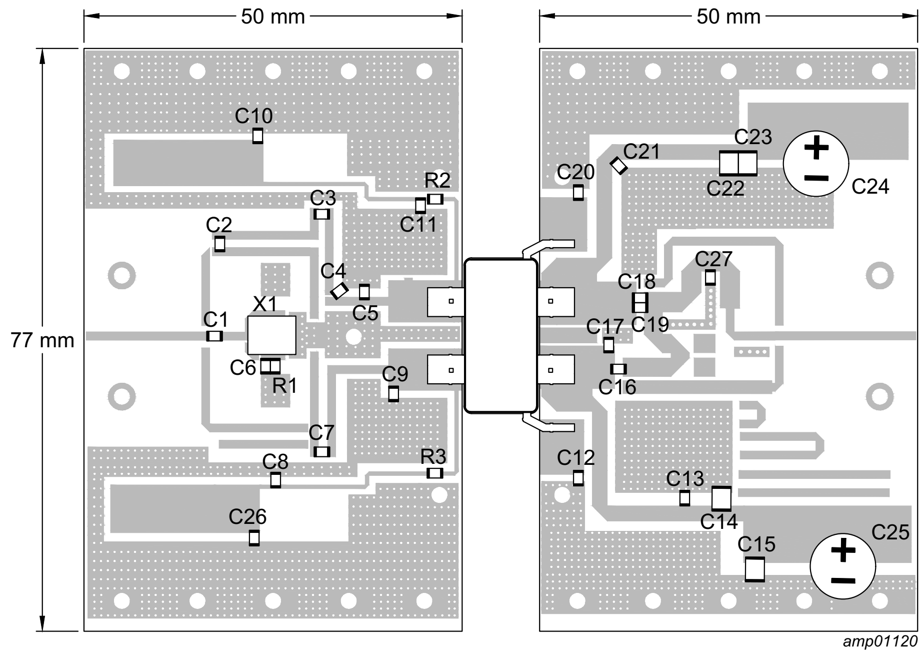


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm; thickness copper plating = 35 μm both sides.

See Table 11 for a list of components.

Fig 2. Component layout

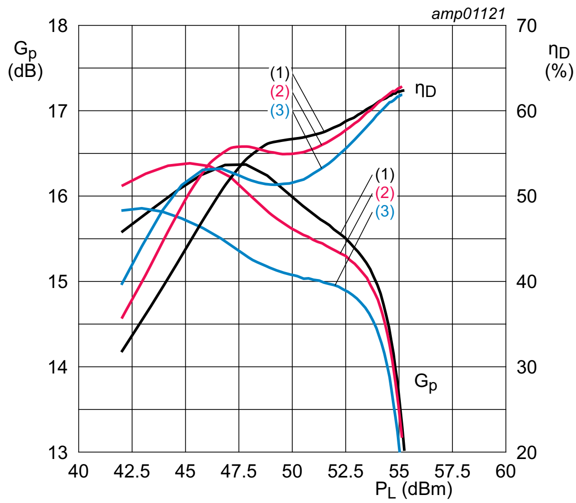
Table 11. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C7, C8, C11, C13, C21	multilayer ceramic chip capacitor	10 pF	ATC: SMD 0805
C4, C17	multilayer ceramic chip capacitor	1 pF	ATC: SMD 0805
C5	multilayer ceramic chip capacitor	1.3 pF	ATC: SMD 0805
C6	multilayer ceramic chip capacitor	0.6 pF	ATC: SMD 0805
C9	multilayer ceramic chip capacitor	0.5 pF	ATC: SMD 0805
C10, C14, C15, C22, C23	multilayer ceramic chip capacitor	10 μF, 100 V	Murata: SMD 1210
C12, C20	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: SMD 1210
C16	multilayer ceramic chip capacitor	11 pF	ATC 800B
C18, C19	multilayer ceramic chip capacitor	1.2 pF	ATC 800B
C24, C25	electrolytic capacitor	1000 μF, 100 V	
C27	multilayer ceramic chip capacitor	0.4 pF	ATC: SMD 0805
R1	resistor	50 Ω, 25 W	Anaren: C16A50Z4
R2, R3	resistor	5.6 Ω, 1 %	SMD 0805
X1	hybrid coupler	5 dB	X3C21P1-05S

7.4 Graphical data

7.4.1 Pulsed CW



V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V; t_p = 100 μs; δ = 10 %.

(1) f = 2110 MHz

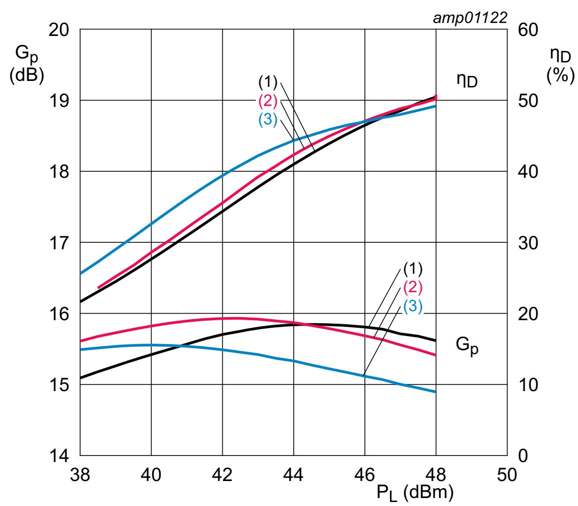
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.



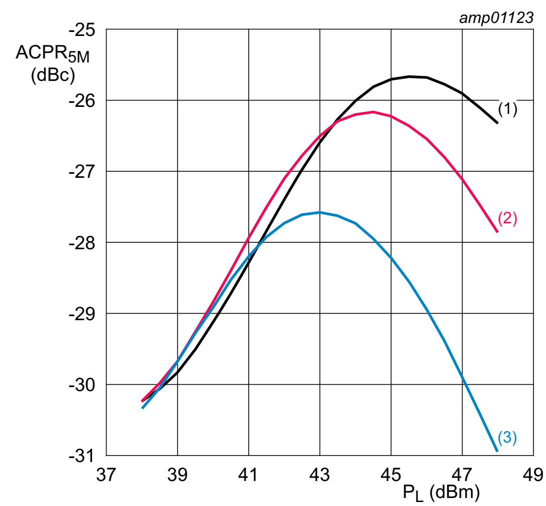
V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



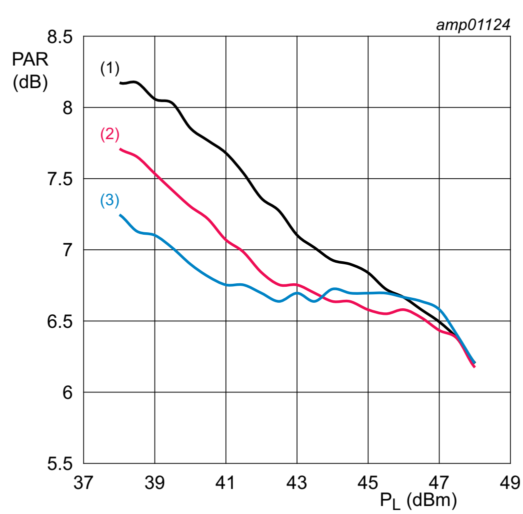
V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V.

(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V.

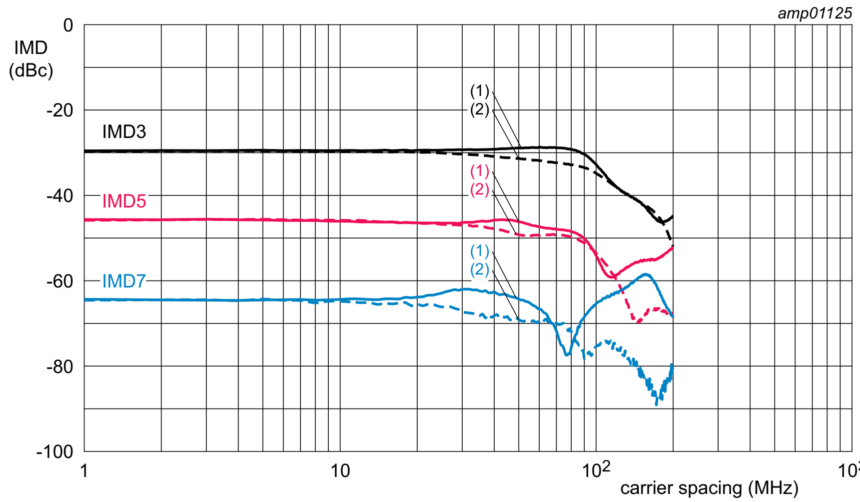
(1) f = 2112.5 MHz

(2) f = 2140 MHz

(3) f = 2167.5 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.1 V; f = 2140 MHz

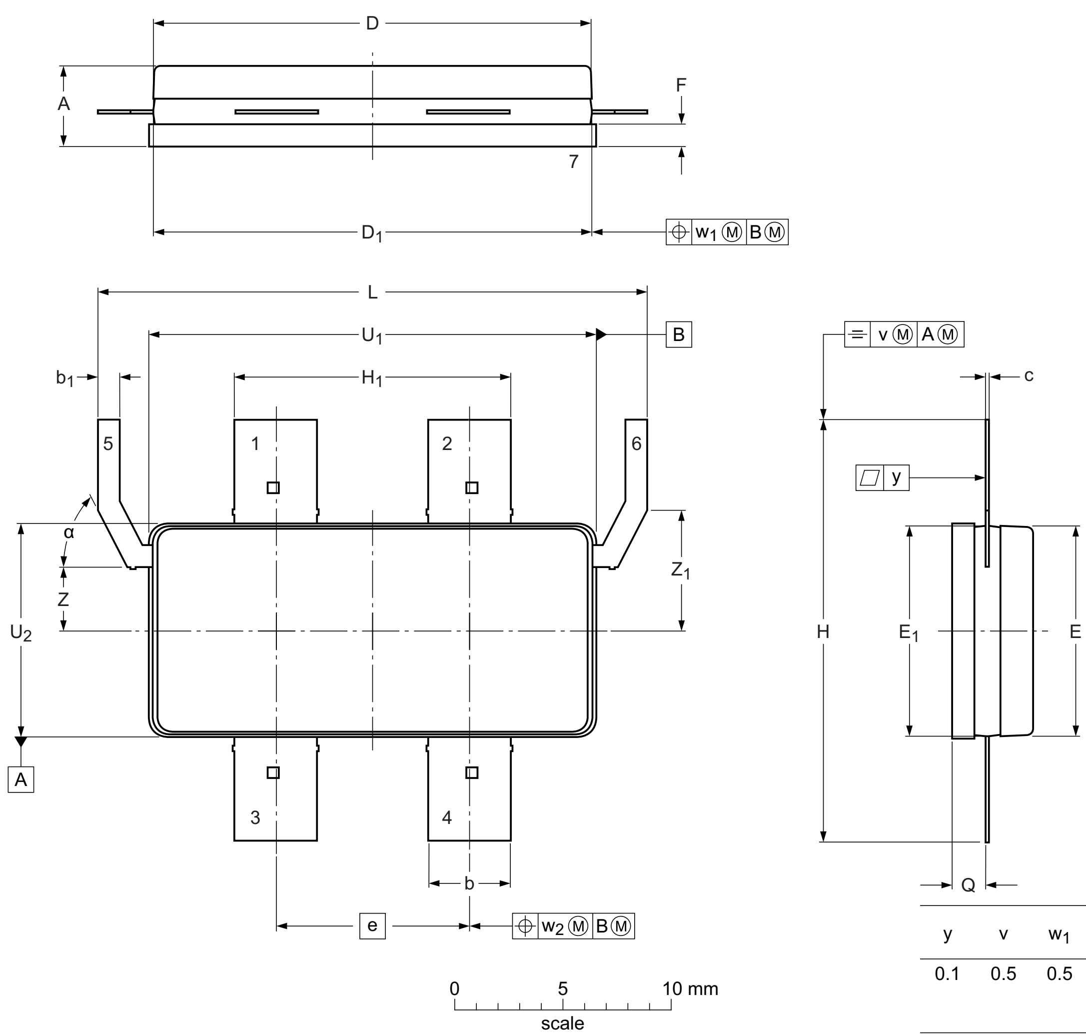
(1) IMD low

(2) IMD high

Fig 7. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1275-1**



y	v	w_1	w_2
0.1	0.5	0.5	0.5

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Q(1)	U_1	U_2	Z	Z_1	α
mm	max	4.01	3.94	1.14	0.178	20.42	20.37	9.80	9.75		1.14	19.53	12.80	25.40	1.68	20.70	9.91	3.17	5.79	65°
	nom									8.89										
	min	3.40	3.68	0.89	0.127	20.12	20.17	9.50	9.55		0.94	19.33	12.60	25.20	1.45	20.50	9.70	2.67	5.29	61°

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1275-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1275-1						~~16-11-15~~ 17-04-13

Fig 8. Package outline SOT1275-1

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G22XS-301AVT v.1	20200430	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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