DS160UP822 UPI 2.0 16-Gbps 8-Channel Linear Redriver with Four 2x2 Crosspoint

1 Features

- Eight channel linear equalizer supporting UPI 2.0 up to 16 Gbps
- Protocol agnostic linear redriver supporting many high speed interface including DisplayPort, SAS, SATA, XFI
- Provides four 2x2 Crosspoint mux function
- CTLE boosts up to 18 dB at 8 GHz
- Ultra-low latency of 90 ps
- Low additive random jitter of 70 fs with PRBS data
- Single 3.3 V supply
- Low active power of 107 mW/channel
- No heat sink required
- Pin-strap, SMBus/I ^{2} C or EEPROM programming
- Seamless support for link training
- Support for x4, x8, x16, x24 bus width with one or multiple DS160UP822
- Industrial temperature range of –40°C to 85°C
- 5.5 mm × 10 mm, 64-pin WQFN package

2 Applications

- Rack server
- Microserver & tower server
- High performance computing
- Hardware accelerator

3 Description

The DS160UP822 is an eight channel low-power high-performance linear redriver designed to support Ultra Path Interface (UPI) 2.0 up to 16 Gbps. The device is a protocol agnostic linear redriver that can operate for many differential interfaces.

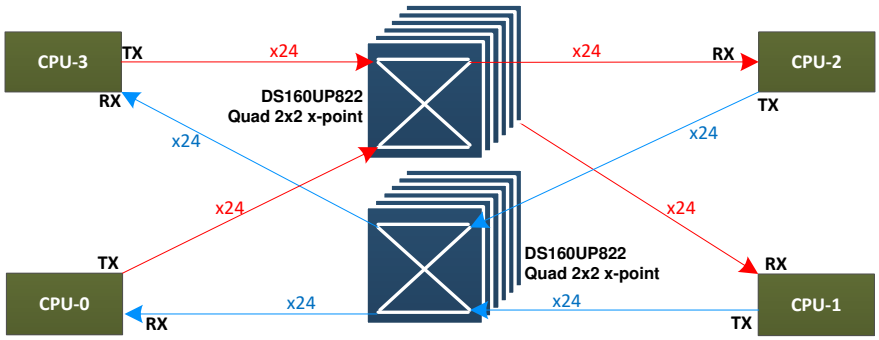
The DS160UP822 receivers deploy continuous time linear equalizers (CTLE) to provide a high-frequency boost. The equalizer can open an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces and cables. The linear redriver along with the passive channel as a whole get link trained for best transmit and receive equalization settings resulting in best electrical link and lowest possible latency. Low channel-channel cross-talk, low additive jitter and excellent return loss allows the device to become almost a passive element in the link. The devices has internal linear voltage regulator to provide clean power supply for high speed datapaths that provides high immunity to any supply noise on the board.

The DS160UP822 implements high speed testing during production for reliable high volume manufacturing. The device also has low AC and DC gain variation providing consistant equalization in high volume platform deployment.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS160UP822	WQFN (64)	5.5 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

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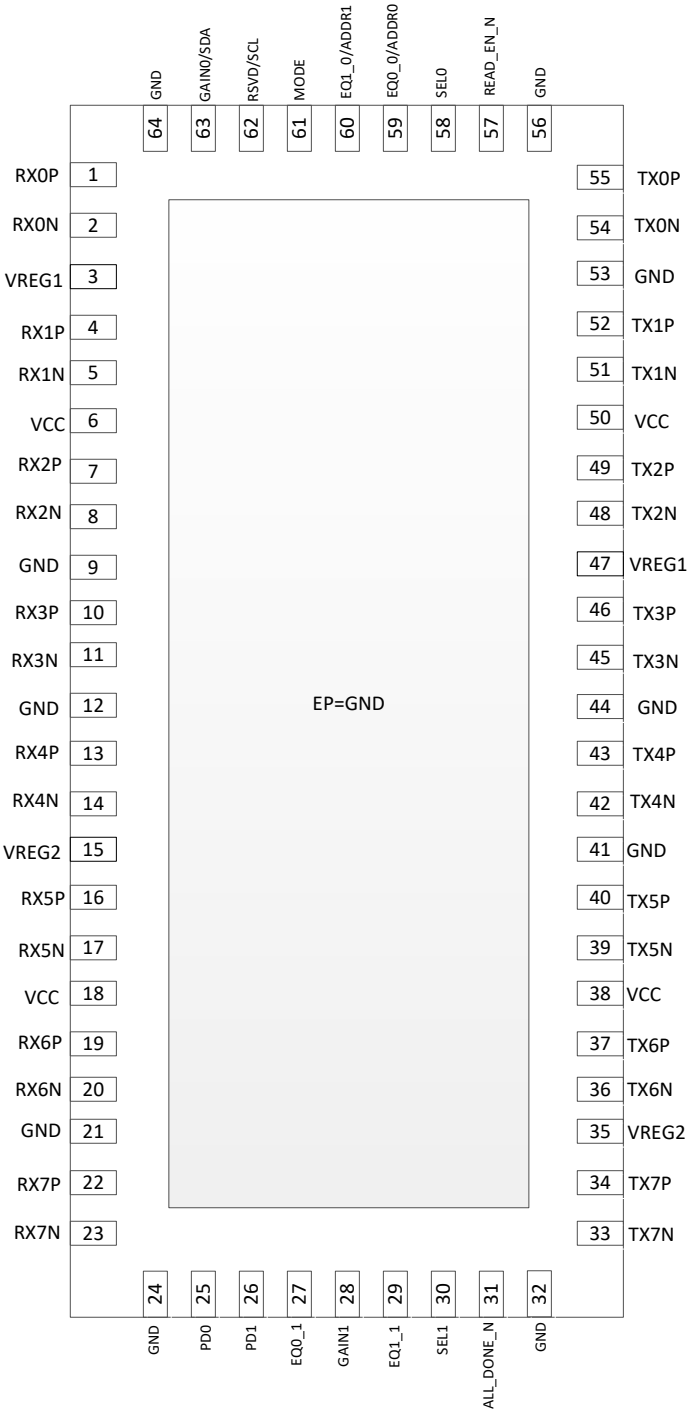
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release

5 Pin Configuration and Functions

Figure 5-1. NJX Package 64-Pin WQFN Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
ALL_DONE_N	31	O, 3.3 V open drain	In **SMBus/I²C Master Mode**: Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7 kΩ required for operation. High: External EEPROM load failed or incomplete Low: External EEPROM load successful and complete In **SMBus/I²C slave/Pin Mode**: This output is High-Z. The pin can be left floating.
MODE	61	I, 4-level	Sets device control configuration modes. 4-level IO pin as defined in Table 7-1. The pin can be exercised at device power up or in normal operation mode. L0: **Pin Mode** – device control configuration is done solely by strap pins. L1: **SMBus/I²C Master Mode** - device control configuration is read from external EEPROM. When the device has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C slave operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I²C master wants to access the device registers it must support arbitration. L2: **SMBus/I²C Slave Mode** – device control configuration is done by an external controller with SMBus/I²C master. L3 (Float): RESERVED – TI internal test mode.
EQ0_0 / ADDR0	59	I, 4-level	In **Pin Mode:** Sets receiver linear equalization (CTLE) for channels 0-3 according to Table 7-2. These pins are sampled at device power-up only. In **SMBus/I²C Mode:** Sets SMBus / I²C slave address according to Table 7-3. These pins are sampled at device power-up only.
EQ1_0 / ADDR1	60	I, 4-level	
EQ0_1	27	I, 4-level	Sets receiver linear equalization (CTLE) for channels 4-7 according to Table 7-2 in Pin mode. The pin is sampled at device power-up only.
EQ1_1	29	I, 4-level	Sets receiver linear equalization (CTLE) for channels 4-7 according to Table 7-2 in Pin mode. The pin is sampled at device power-up only.
GAIN0 / SDA	63	I, 4-level / I/O, 3.3 V LVCMOS, open drain	In **Pin Mode:** Flat gain (DC and AC) from the input to the output of the device for channels 0-3. The pin is sampled at device power-up only. In **SMBus/I²C Mode:** 3.3 V SMBus/I²C data. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I²C interface standard.
GAIN1	28	I, 4-level	Flat gain (DC and AC) from the input to the output of the device for channels 4-7 in Pin mode. The pin is sampled at device power-up only.
GND	EP, 9, 12, 21, 24, 32, 41, 44, 53, 56, 64	P	Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to ground plane(s) through low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation.
PD0	25	I, 3.3 V LVCMOS	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1-MΩ weak pulldown resistor. High: Power down for channels 0-3 Low: Power up, normal operation for channels 0-3
PD1	26	I, 3.3 V LVCMOS	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1-MΩ weak pulldown resistor. High: Power down for channels 4-7 Low: Power up, normal operation for channels 4-7
READ_EN_N	57	I, 3.3 V LVCMOS	In **SMBus/I²C Master Mode**: After device power up, when the pin is low, it initiates the SMBus / I²C master mode EEPROM read function. Once EEPROM read is complete (indicated by assertion of ALL_DONE_N low), this pin can be held low for normal device operation. During the EEPROM load process the device's signal path is disabled. In **SMBus/I²C Slave and Pin Modes:** In these modes the pin is not used. The pin can be left floating. The pin has internal 1-MΩ weak pulldown resistor.

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
SEL0	58	I, 3.3 V LVCMOS	The pin selects the mux path for channels 0-3. L: straight data path - RX[0/1/2/3][P/N] connected to TX[0/1/2/3][P/N] through the redriver. H: cross data path - RX[0/1/2/3][P/N] connected to TX[1/0/3/2][P/N] through the redriver Active in all device control modes. 59 kΩ internal pull-down.
SEL1	30	I, 3.3 V LVCMOS	The pin selects the mux path for channels 4-7. L: straight data path - RX[4/5/6/7][P/N] connected to TX[4/5/6/7][P/N] through the redriver. H: cross data path - RX[4/5/6/7][P/N] connected to TX[5/4/7/6][P/N] through the redriver Active in all device control modes. 59 kΩ internal pull-down.
RSVD / SCL	62	I/O, 3.3 V LVCMOS, open drain	In **Pin Mode:** Reserved for TI internal use. The pin must be pulled down to GND through 1 kΩ resistor In **SMBus/I^{2}C Mode:** 3.3V SMBus/I^{2}C clock. External 1 kΩ to 5 kΩ pullup resistor is required as per SMBus / I^{2}C interface standard.
RX0N	2	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX0P	1	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 0.
RX1N	5	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX1P	4	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 1.
RX2N	8	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.
RX2P	7	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 2.
RX3N	11	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
RX3P	10	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 3.
RX4N	14	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 4.
RX4P	13	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 4.
RX5N	17	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 5.
RX5P	16	I	Noninverting differential inputs to the equalizer. An on-chip, 100 Ω termination resistor connects RXP to RXN. Channel 5.
RX6N	20	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 6.
RX6P	19	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 6.
RX7N	23	I	Inverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 7.
RX7P	22	I	Noninverting differential inputs to the equalizer. Integrated 50 Ω termination resistor from the pin to internal CM bias voltage. Channel 7.
TX0N	54	O	Inverting pin for 100 Ω differential driver output. Channel 0.
TX0P	55	O	Non-inverting pin for 100 Ω differential driver output. Channel 0.
TX1N	51	O	Inverting pin for 100 Ω differential driver output. Channel 1.
TX1P	52	O	Non-inverting pin for 100 Ω differential driver output. Channel 1.
TX2N	48	O	Inverting pin for 100 Ω differential driver output. Channel 2.
TX2P	49	O	Non-inverting pin for 100 Ω differential driver output. Channel 2.
TX3N	45	O	Inverting pin for 100 Ω differential driver output. Channel 3.

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
TX3P	46	O	Non-inverting pin for 100 Ω differential driver output. Channel 3.
TX4N	42	O	Inverting pin for 100 Ω differential driver output. Channel 4.
TX4P	43	O	Non-inverting pin for 100 Ω differential driver output. Channel 4.
TX5N	39	O	Inverting pin for 100 Ω differential driver output. Channel 5.
TX5P	40	O	Non-inverting pin for 100 Ω differential driver output. Channel 5.
TX6N	36	O	Inverting pin for 100 Ω differential driver output. Channel 6.
TX6P	37	O	Non-inverting pin for 100 Ω differential driver output. Channel 6.
TX7N	33	O	Inverting pin for 100 Ω differential driver output. Channel 7.
TX7P	34	O	Non-inverting pin for 100 Ω differential driver output. Channel 7.
VCC	6, 18, 38, 50	P	Power supply pins. VCC = 3.3 V ±10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane.
VREG1	3, 47	P	Internal voltage regulator output. Must add decoupling caps of 0.1 µF near each pins. The regulator is only for internal use. Do not use to provide power to any external component. Do not connect to VREG2.
VREG2	15, 35	P	Internal voltage regulator output. Must add decoupling caps of 0.1 µF near each pins. The regulator is only for internal use. Do not use to provide power to any external component. Do not connect to VREG1.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC_{ABSMAX}	Supply voltage (VCC)	–0.5	4.0	V
$VIO_{CMOS,ABSMAX}$	3.3 V LVCMOS and open drain I/O voltage	–0.5	4.0	V
$VIO_{4LVL,ABSMAX}$	4-level input I/O voltage	–0.5	2.75	V
$VIO_{HS\text{-}RX,ABSMAX}$	High-speed I/O voltage (RXnP, RXnN)	–0.5	3.2	V
$VIO_{HS\text{-}TX,ABSMAX}$	High-speed I/O voltage (TXnP, TXnN)	–0.5	2.75	V
$T_{J,ABSMAX}$	Junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±3 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage, VCC to GND	DC plus AC power should not exceed these limits	3.0	3.3	3.6	V
N_{VCC}	Supply noise tolerance[1]	DC to <50 Hz, sinusoidal			250	mVpp
		50 Hz to 500 kHz, sinusoidal			100	mVpp
		500 kHz to 2.5 MHz, sinusoidal			33	mVpp
		>2.5 MHz, sinusoidal			10	mVpp
$T_{RampVCC}$	VCC supply ramp time	From 0 V to 3.0 V	0.150		100	ms
T_J	Operating junction temperature		–40		115	°C
T_A	Operating ambient temperature		–40		85	°C
PW_{LVCMOS}	Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs	PD1/0, and READ_EN_N	200			uS
VCC_{SMBUS}	SMBus/I²C SDA and SCL open drain termination voltage	Supply voltage for open drain pull-up resistor			3.6	V
F_{SMBus}	SMBus/I²C clock (SCL) frequency in SMBus slave mode		10		400	kHz
VID_{LAUNCH}	Source differential launch amplitude		800		1200	mVpp
DR	Data rate		1		16	Gbps

6.4 Thermal Information

THERMAL METRIC[1]		DS160 UP8 NJX, 64 Pins	UNIT
$R_{\theta JA\text{-}High\ K}$	Junction-to-ambient thermal resistance	22.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

6.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$POWER_{CH}$	Active power **per channel**	GAIN1/0 = L3 (default)		107		mW
		GAIN1/0 = L0		99		mW
$I_{ACTIVE\text{-}8CH}$	Device current consumption when **all eight channels** are active	GAIN1/0 = L3		260	360	mA
I_{STBY}	Device current consumption in standby power mode	All channels disabled (PD1,0 = H)		30	45	mA
V_{REG}	Internal regulator output			2.5		V
Control IO (SDA, SCL, PD1, PD0, READ_EN_N, SEL1, SEL0 pins)						
V_{IH}	High level input voltage	SDA, SCL, PD1, PD0, READ_EN_N, SEL1, SEL0 pins	2.1			V
V_{IL}	Low level input voltage	SDA, SCL, PD1, PD0, READ_EN_N, SEL1, SEL0 pins			1.08	V
V_{OH}	High level output voltage	$R_{pull\text{-}up}$ = 4.7 kΩ (SDA, SCL, ALL_DONE_N pins)	2.1			V
V_{OL}	Low level output voltage	I_{OL} = –4 mA (SDA, SCL, ALL_DONE_N pins)			0.4	V
$I_{IH,SEL}$	Input high leakage current for SEL pins	V_{Input} = VCC for SEL1, SEL0 pins			80	µA
I_{IH}	Input high leakage current	V_{Input} = VCC, (SCL, SDA, PD1, PD0, READ_EN_N pins)			10	µA
I_{IL}	Input low leakage current	V_{Input} = 0 V, (SCL, SDA, PD1, PD0, READ_EN_N, SEL1, SEL0 pins)	-10			µA
$I_{IH,FS}$	Input high leakage current for fail safe input pins	V_{Input} = 3.6 V, VCC = 0 V, (SCL, SDA, , PD1, PD0, READ_EN_N, SEL1, SEL0 pins)			200	µA
$C_{IN\text{-}CTRL}$	Input capacitance	SDA, SCL, PD1, PD0, READ_EN_N, SEL1, SEL0 pins		1.5		pF
4 Level IOs (MODE, GAIN0, GAIN1, EQ0_0, EQ1_0, EQ0_1, EQ1_1, RX_DET pins)						
I_{IH_4L}	Input high leakage current, 4 level IOs	VIN = 2.5 V			10	µA
I_{IL_4L}	Input low leakage current for all 4 level IOs except MODE.	VIN = GND	-10			µA
$I_{IL\_4L,MODE}$	Input low leakage current for MODE pin	VIN = GND	-200			µA
Receiver						
$V_{RX\text{-}DC\text{-}CM}$	RX DC common mode (CM) voltage	Device is in active or standby state		2.5		V

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{RX-DC}	Rx DC single-ended impedance			50		Ω
$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance during Reset or power-down	Inputs are at CM voltage	20			kΩ
Transmitter						
$Z_{TX-DIFF-DC}$	DC differential Tx impedance	Impedance of Tx during active signaling, VID,diff = 1Vpp		100		Ω
$V_{TX-DC-CM}$	Tx DC common mode Voltage			0.75		V
$I_{TX-SHORT}$	Tx Short circuit current	Total current the Tx can supply when shorted to GND			90	mA

6.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver						
$RL_{RX-DIFF}$	Input differential return loss	50 MHz to 1.25 GHz		-25		dB
		1.25 GHz to 2.5 GHz		-22		dB
		2.5 GHz to 4.0 GHz		-21		dB
		4.0 GHz to 8.0 GHz		-16		dB
XT_{RX}	Receive-side pair-to-pair isolation	Pair-to-pair isolation (SDD21) between two adjacent receiver pairs from 10 MHz to 8 GHz.		-47		dB
Transmitter						
$RL_{TX-DIFF}$	Output differential return loss	50 MHz to 1.25 GHz		-20		dB
		1.25 GHz to 2.5 GHz		-18		dB
		2.5 GHz to 4.0 GHz		-18		dB
		4.0 GHz to 8.0 GHz		-17		dB
XT_{TX}	Transmit-side pair-to-pair isolation	Minimum pair-to-pair isolation (SDD21) between two adjacent transmitter pairs from 10 MHz to 8 GHz.		-48		dB
Device Datapath						
$T_{PLHD/PHLD}$	Input-to-output latency (propagation delay) through a data channel	For either low-to-high or high-to-low transition.		90	120	ps
$L_{TX-SKEW}$	Lane-to-lane output skew	Between any two lanes within a single transmitter.	-20		20	ps
$T_{RJ-DATA}$	Additive random jitter with data	Jitter through redriver minus the calibration trace. 16Gbps PRBS15. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		70		fs
$T_{RJ-INTRINSIC}$	Intrinsic additive random jitter with clock	Jitter through redriver minus the calibration trace. 8 Ghz CK. Minimal input/output channels. Minimum EQ. 400 mVpp-diff input swing.		90		fs
$JITTER_{TOTAL-DATA}$	Additive total jitter with data	Jitter through redriver minus the calibration trace. 16 Gbps PRBS15. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		4		ps
$JITTER_{TOTAL-INTRINSIC}$	Intrinsic additive total jitter with clock	Jitter through redriver minus the calibration trace. 8 Ghz CK. Minimal input/output channels. Minimum EQ. 800 mVpp-diff input swing.		1		ps

over operating free-air temperature and voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLAT-GAIN	Flat gain (DC and AC) input to output	Minimum EQ, GAIN1/0=L0		-4.2		dB
		Minimum EQ, GAIN1/0=L1		-1.8		dB
		Minimum EQ, GAIN1/0=L2		0.25		dB
		Minimum EQ, GAIN1/0=L3 (float, default)		2		dB
$EQ\text{-}MAX_{8G}$	EQ boost at max setting (EQ INDEX = 15)	AC gain at 8 GHz relative to gain at 100 MHz. GAIN1/0=L3 (float, default).		18.0		dB
$DCGAIN_{VAR}$	DC gain variation	GAIN1/0 = L2, minimum EQ setting. Max-Min.	-2.3		1.7	dB
$EQGAIN_{VAR}$	EQ boost variation	At 8 Ghz. GAIN1/0 = L2, maximum EQ setting. Max-Min.	-3.3		3.7	dB
LIN_{DC}	Output DC linearity	GAIN1/0 = L3 (float, default). 128T pattern at 2.5 Gbps.		1000		mVpp
LIN_{AC}	Output AC linearity	GAIN1/0 = L3 (float, default). 1T pattern at 16 Gbps.		750		mVpp

6.7 SMBUS/I2C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slave Mode						
t_{SP}	Pulse width of spikes which must be suppressed by the input filter				50	ns
$t_{HD\text{-}STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
T_{HIGH}	HIGH period of the SCL clock		0.6			µs
$t_{SU\text{-}STA}$	Set-up time for a repeated START condition		0.6			µs
$t_{HD\text{-}DAT}$	Data hold time		0			µs
$t_{SU\text{-}DAT}$	Data setup time		0.1			µs
t_r	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns
t_f	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
$t_{SU\text{-}STO}$	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between a STOP and START condition		1.3			µs
$t_{VD\text{-}DAT}$	Data valid time				0.9	µs
$t_{VD\text{-}ACK}$	Data valid acknowledge time				0.9	µs
C_b	capacitive load for each bus line				400	pF
Master Mode						
$f_{SCL\text{-}M}$	SCL clock frequency	MODE = L1 (Master Mode)		303		kHz
$t_{LOW\text{-}M}$	SCL low period			1.9		µs
$t_{HIGH\text{-}M}$	SCL high period			1.4		µs
$t_{SU\text{-}STA\text{-}M}$	Set-up time for a repeated START condition			2		µs
$t_{HD\text{-}STA\text{-}M}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated			1.5		µs
$t_{SU\text{-}DAT\text{-}M}$	Data setup time			1.4		µs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{HD-DAT-M}$	Data hold time			0.5		µs
t_{R-M}	Rise time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		120		ns
t_{F-M}	Fall time of both SDA and SCL signals	Pull-up resistor = 4.7 kΩ, Cb = 10pF		2		ns
$t_{SU-STO-M}$	Stop condition setup time			1.5		µs
EEPROM Timing						
T_{EEPROM}	EEPROM configuration load time	Time to assert ALL_DONE_N after READ_EN_N has been asserted. Single device reading its configuration from an EEPROM with **common channel configuration with individual channel settings**. This time scales with the number of devices reading from the same EEPROM. Does not include power-on reset time.		7.5		ms
T_{POR}	Time to first SMBus access	Power supply stable after initial ramp. Includes initial power-on reset time.		50		ms

6.8 Typical Characteristics

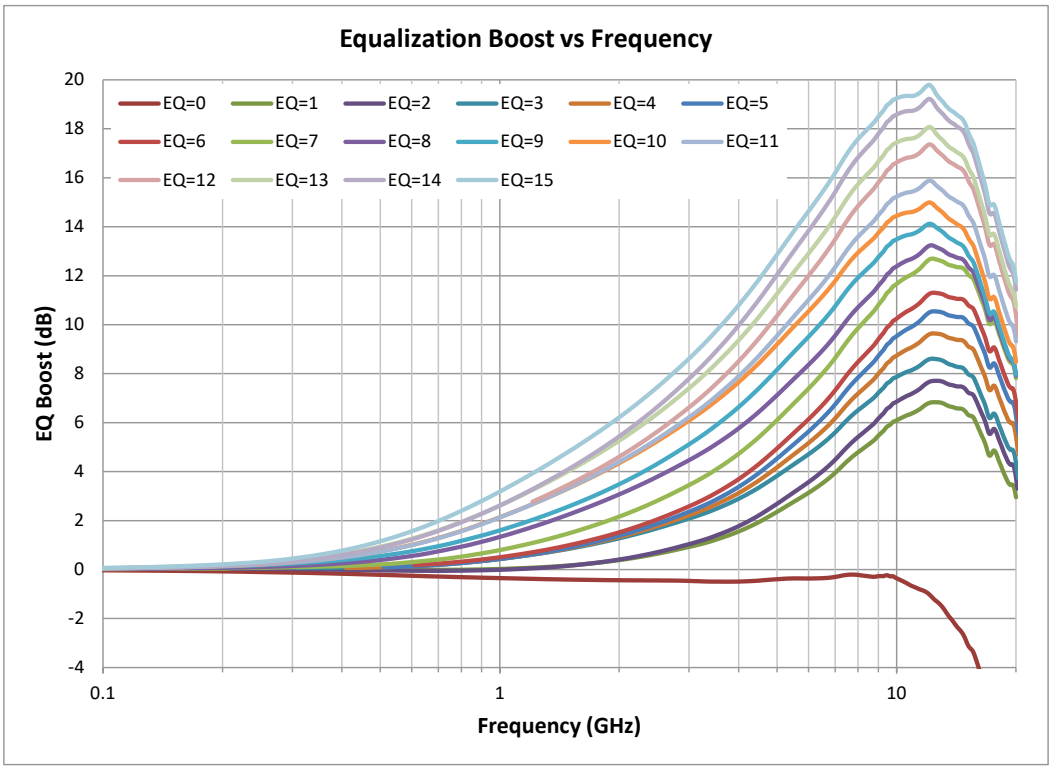


Figure 6-1. Typical EQ Boost vs Frequency

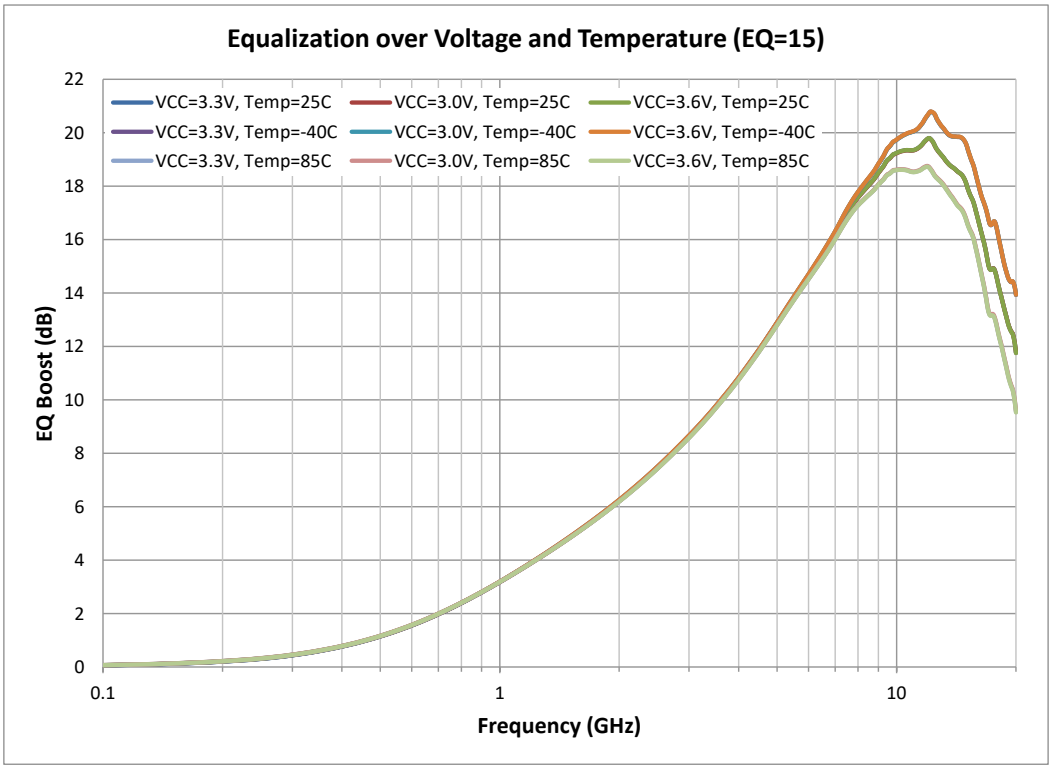


Figure 6-2. Typical EQ Boost over Voltage and Temperature with EQ=15

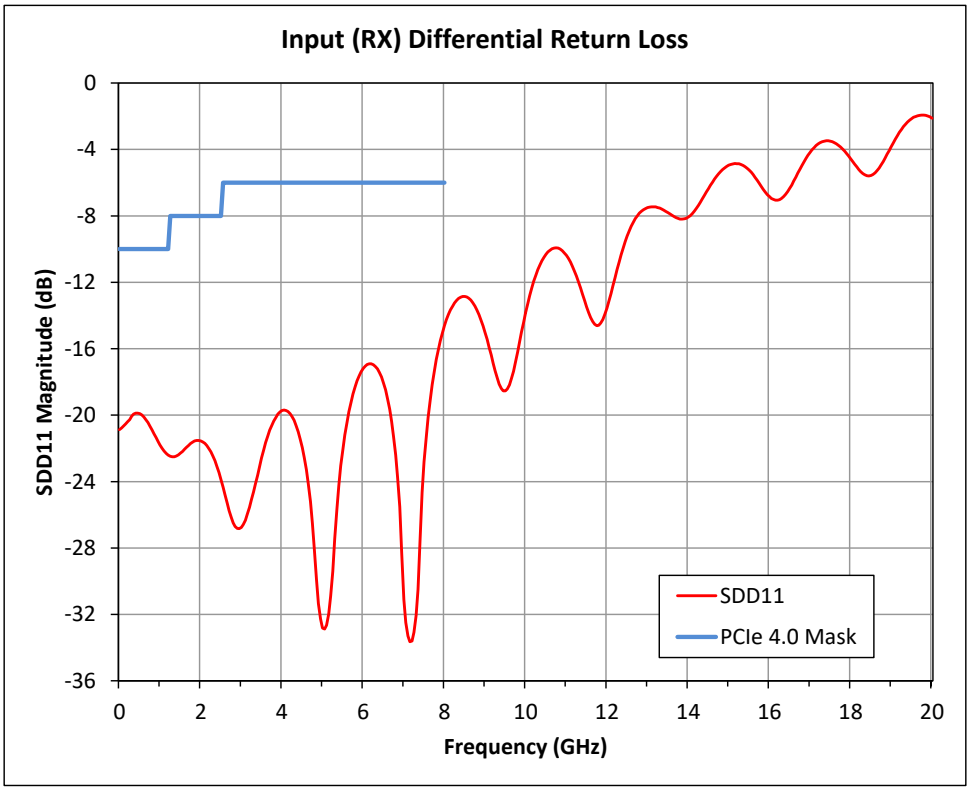


Figure 6-3. Typical RX Differential Return Loss

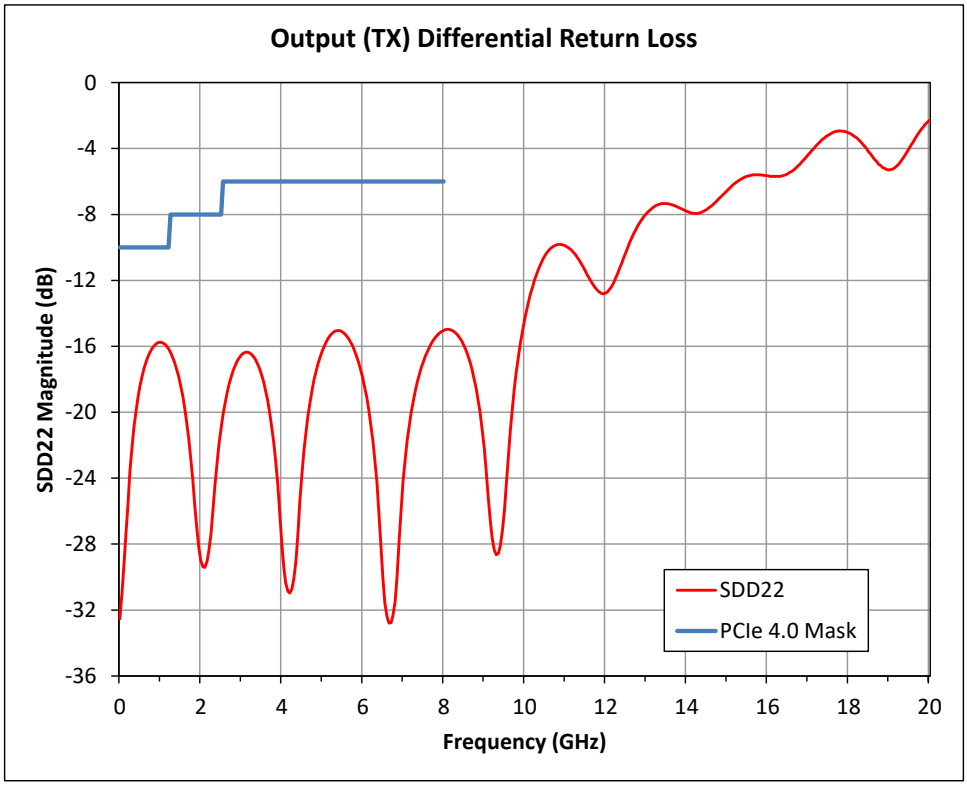


Figure 6-4. Typical TX Differential Return Loss

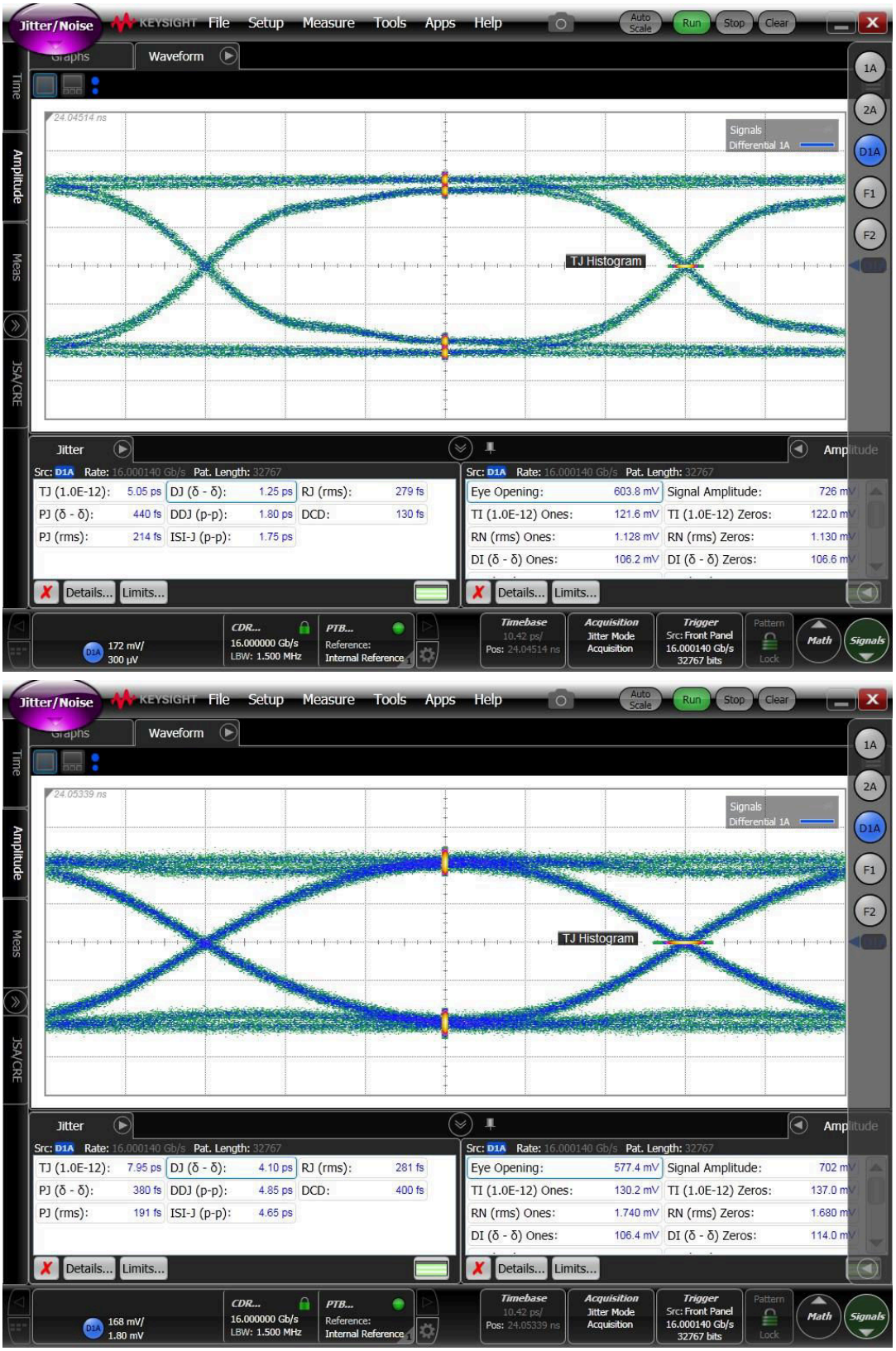


Figure 6-5. Typical Jitter Characteristics - Top: 16Gbps PRBS15 Input to the Device, Bottom: Output of the Device.

7 Detailed Description

7.1 Overview

The DS160UP822 is an eight-channel multi-rate linear repeater with integrated signal conditioning. The device provides quad 2x2 crosspoint mux functionality selectable by pin control or SMBus/I^{2}C. The device's signal channels operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

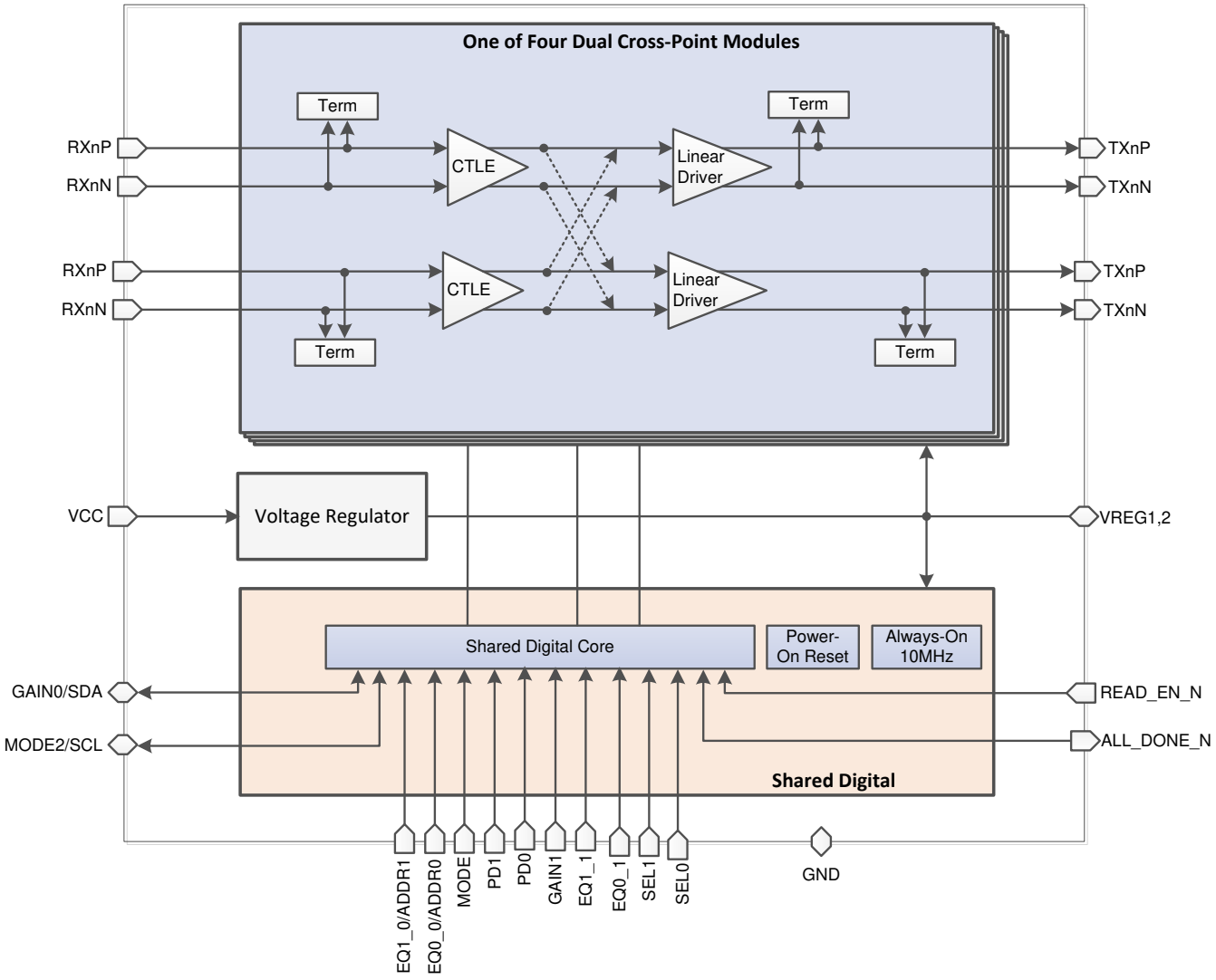
The DS160UP822 can be configured three different ways:

Pin Mode – device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I^{2}C Master Mode - device control configuration is read from external EEPROM. When the device has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I^{2}C slave operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I^{2}C master wants to access device registers it must support arbitration. The mode is prefferred when software implementation is not desired.

SMBus/I^{2}C Slave Mode - provides most flexibility. Requires a SMBus/I^{2}C master device to configure the device through writing to its slave address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Linear Equalization

The DS160UP822 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 7-1 shows available equalization boost through EQ control pins (EQ1_0 and EQ0_0 for channels 0-3 and EQ1_1 and EQ0_1 for channels 4-7), when in Pin Control mode (MODE = L0).

Table 7-1. Equalization Control Settings

EQUALIZATION SETTING			TYPICAL EQ BOOST (dB)	
EQ INDEX	EQ1_0 (Ch 0-3) / EQ1_1 (Ch 4-7)	EQ0_0 (Ch0-3) / EQ0_1 (Ch 4-7)	@ 4 GHz	@ 8 GHz
0	L0	L0	0.0	-0.2
1	L0	L1	1.5	4.5
2	L0	L2	2.0	5.5
3	L0	L3	2.5	6.5
4	L1	L0	2.7	7.0
5	L1	L1	3.0	8.0
6	L1	L2	4.0	9.0

Table 7-1. Equalization Control Settings (continued)

EQUALIZATION SETTING			TYPICAL EQ BOOST (dB)	
EQ INDEX	EQ1_0 (Ch 0-3) / EQ1_1 (Ch 4-7)	EQ0_0 (Ch0-3) / EQ0_1 (Ch 4-7)	@ 4 GHz	@ 8 GHz
7	L1	L3	5.0	10.0
8	L2	L0	6.0	11.0
9	L2	L1	7.0	12.0
10	L2	L2	7.5	13.0
11	L2	L3	8.0	13.5
12	L3	L0	8.5	15.0
13	L3	L1	9.5	16.5
14	L3	L2	10.0	17.0
15	L3	L3	11.0	18.0

The equalization of the device can also be set by writing to SMBus/I^{2}C registers in slave or master mode. Refer to the *DS160UP822 Programming Guide* (SNLU279) for details.

7.3.2 Flat Gain

The GAIN1 and GAIN0 pins can be used to set the overall datapath flat gain (DC and AC) of the DS160UP822 when the device is in Pin Mode. The pin GAIN0 sets the flat gain for channels 0-3 and GAIN1 sets the same for channels 4-7. The default recommendation for most systems will be GAIN1,0 = L3 (float).

The flat gain and equalization of the DS160UP822 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

7.3.3 Cross Point

The DS160UP822 provides quad 2x2 cross-point function. Using pin SEL1, SEL0 pins the 8 channel signal paths can be configured as staright connection or quad cross connections. SEL1 pin impacts channel 0-3 and SEL1 configures channels 4-7.

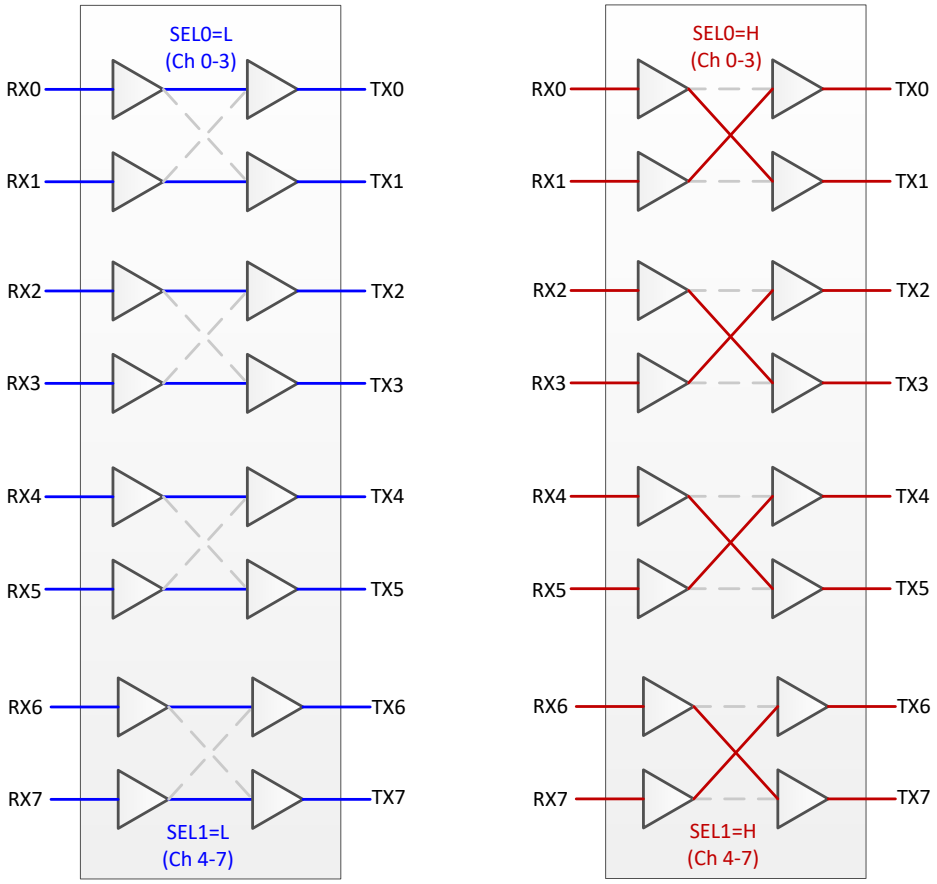


Figure 7-1. DS160UP822 Signal Flow Diagram for Cross-Point Mux Operation

7.4 Device Functional Modes

7.4.1 Active Mode

The device is in normal operation. In this mode PD0/PD1 pins are driven low in a system.

7.4.2 Standby Mode

The device is in standby mode invoked by PD1,0 = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Control and Configuration Interface

7.5.1.1 Pin Mode

The DS160UP822 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 4-level pins for device control and signal integrity optimum settings. The *Section 5* section defines the control pins.

7.5.1.1.1 Four-Level Control Inputs

The DS160UP822 has 4-level inputs pins (EQ0_0, EQ1_0, EQ0_1, EQ1_1, GAIN0, GAIN1, and MODE) that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the 4 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The pins are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

Table 7-2. 4-Level Control Pin Settings

LEVEL	SETTING
L0	1 kΩ to GND

Table 7-2. 4-Level Control Pin Settings (continued)

LEVEL	SETTING
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	F (Float)

7.5.1.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus / I²C slave control mode), the DS160UP822 is configured for best signal integrity through a standard I²C or SMBus interface that may operate up to 400 kHz. The slave address of the device is determined by the pin strap settings on the ADDR1 and ADDR0 pins. Note slave addresses to access channel 0-3 and Channels 4-7 is different. Channel bank 4-7 has address which is Channel bank 0-3 address +1. The sixteen possible slave addresses (8-bit) for each channel banks of the the device are shown in Table 7-3. In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 50 pF.

Refer to the *DS160UP822 Programming Guide* (SNLU279) for register map details.

Table 7-3. SMBUS/I2C Slave Address Settings

ADDR1	ADDR0	7-bit Slave Address Channels 0-3	7-bit Slave Address Channels 4-7
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

7.5.1.3 SMBus/I ² C Master Mode Configuration (EEPROM Self Load)

The DS160UP822 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after device's initial power-up. If the device is configured for SMBus master mode, it will remain in the SMBus IDLE state until the READ_EN_N pin is asserted to LOW. After the READ_EN_N pin is driven LOW, the device becomes an SMBus master and attempts to self-configure by reading device settings stored in an external EEPROM (SMBus 8-bit address 0xA0). When the device has finished reading from the EEPROM successfully, it will drive the ALL_DONE_N pin LOW. SMBus/I²C slave operation is available in this mode before, during or after EEPROM reading. Note during EEPROM reading if the external SMBus/I²C master wants to access the device registers it must support arbitration. Refer to the *Understanding EEPROM Programming for PCI-Express 4.0 Redrivers* (SNLA342) application report for more information.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2 kb (256 × 8-bit) is recommended.

- Set MODE = L1, configure for SMBus master mode
- The external EEPROM device address byte must be 0xA0 and capable of 400 kHz operation at 3.3 V supply
- In SMBus/I^{2}C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Figure 7-2 shows a use case with four DS160UP822 to implement a configuration, but the user can cascade any number of DS160UP822 devices in a similar way. Tie first device's READ_EN_N pin low to automatically initiate EEPROM read at power up. Alternately the READ_EN_N pin of the first device can also be controlled by a microcontroller to initiate the EEPROM read manually. Leave the final device's ALL_DONE_N pin floating, or connect the pin to a microcontroller input to monitor the completion of the final EEPROM read.

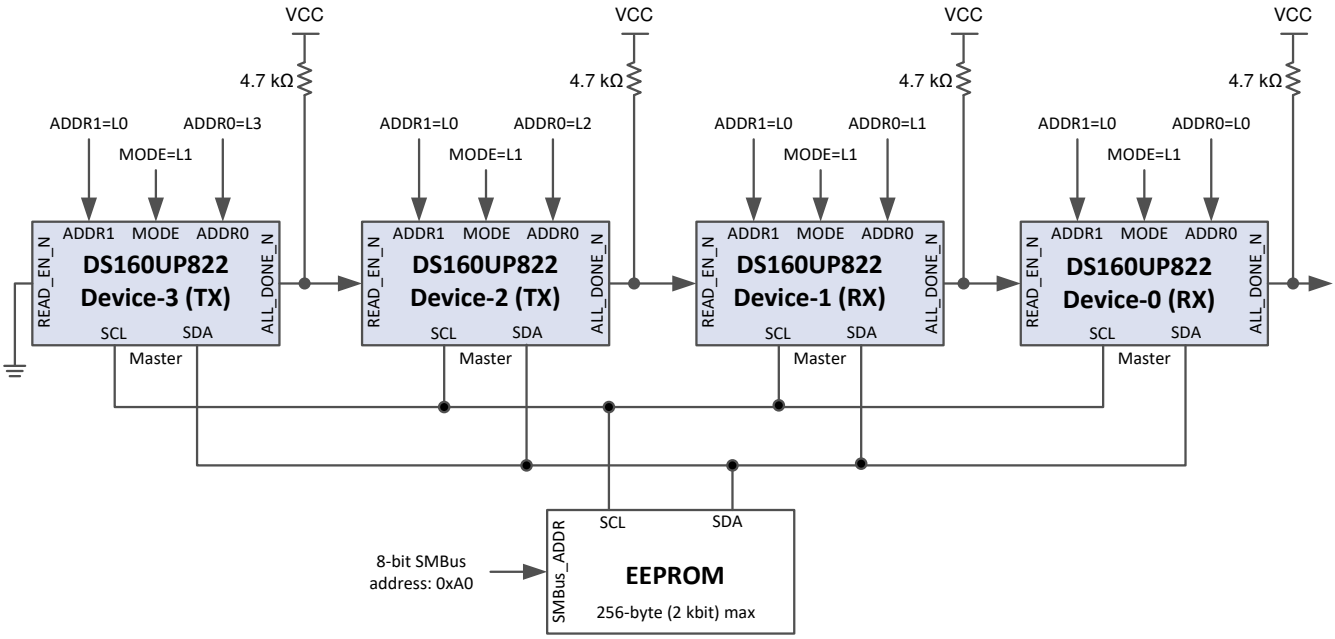


Figure 7-2. Daisy Chain Four DS160UP822 Devices to Read from Single EEPROM

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS160UP822 is a high-speed linear repeater which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The DS160UP822 is a protocol and interface agnostic linear redriver that can be used in wide range of interfaces including:

- Ultra Path Interconnect (UPI) 1.0/2.0
- DisplayPort 2.0
- SAS
- SATA
- XFI

The DS160UP822 is a protocol agnostic linear redriver. Figure 8-1 shows how eight DS160UP822 devices can be used to implement 2x2 crosspoint for x24 bus width to connect four CPUs to provide flexible interconnectivity between them.

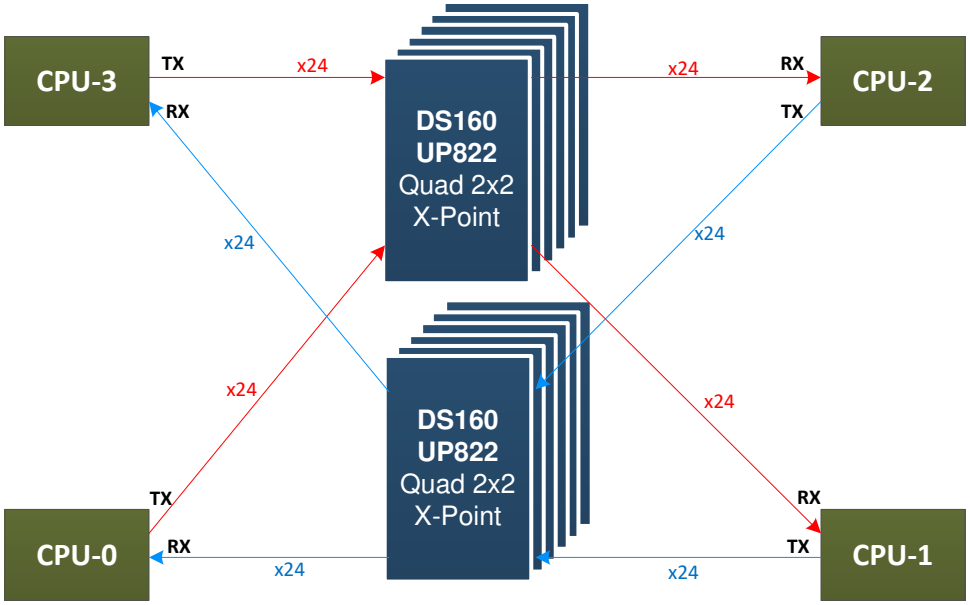


Figure 8-1. 2x2 Cross point for x24 bus width using DS160UP822

8.2.1 UPI 2x2 Cross Point Mux for x24 Lane Configuration

The DS160UP822 can be used in server or motherboard applications as cross point mux to create a flexible CPU to CPU connectivity. The section outlines detailed procedure and design requirement for a typical UPI x24 lane Mux configuration. However, the design recommendations can be used in any lane configuration.

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Use 85 Ω impedance traces . Length matching on the P and N traces should be done on the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

For operation in UPI 2.0 links, the DS160UP822 is designed with linear datapth to pass the Tx preset signaling (by root complex and end point) onto the Rx (of root complex and end point) to train and optimize the equalization settings. The linear redriver device helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream Rx more easily. The device must be placed in between the Tx and Rx (of root complex and end point) such a way that both RX and TX signal swing stays within the linearity range of the device. Adjustments to the device EQ setting should be performed based on the channel loss to optimize the eye opening in the Rx partner. The available EQ gain settings are provided in Table 7-1. For most systems the default DC gain setting GAIN = floating would be sufficient.

The DS160UP822 can be optimized for a given system utlizing its three configuration modes - Pin Mode, SMBus/I^2C Master Mode and SMBus/I^2C Slave Mode. In SMBus/I^2C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

Figure 8-2 shows a simplified schematic for UPI 2x2 cross-point mux for x24 lane configuration in SMBus/I2C Master Mode.

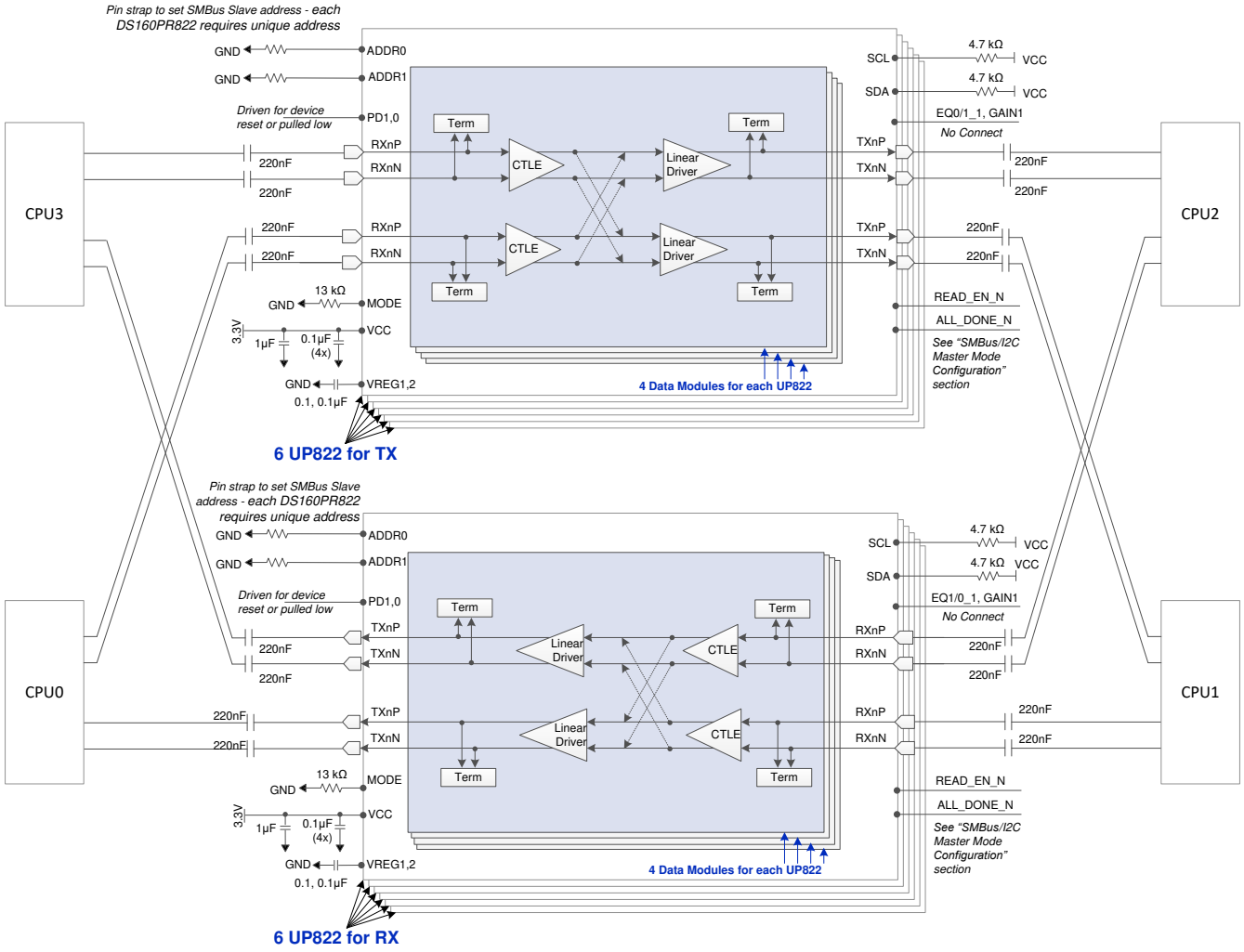


Figure 8-2. Simplified Schematic for UPI 2x2 cross-point mux for x24Lane Configuration in SMBus/I2C Master Mode

8.2.1.3 Application Curves

The DS160UP822 is a linear redriver that can be used to extend channel reach of a UPI link. Normally, PCIe-compliant TX and RX are equipt with signal-conditioning functions and can handle channel losses of up to 28 dB at 8 GHz. With the DS160UP822 in the link, the total channel loss between two CPUs can be up to 42 dB at 8 GHz.

Figure 8-3 shows an electric link that models a single channel of a UPI link and eye diagrams measured at different locations along the link. The source that models a UPI TX sends a 16 Gbps PRBS-15 signal with P7 presets. After a transmission channel with –30 dB at 8 GHz insertion loss, the eye diagram is fully closed. The DS160UP822 with its CTLE set to the maximum (18 dB boost) together with the source TX equalization compensates for the losses of the pre-channel (TL1) and opens the eye at the output of the device.

The post-channel (TL2) losses mandate the use of UPI RX equalization functions such as CTLE and DFE that are normally available in receivers.

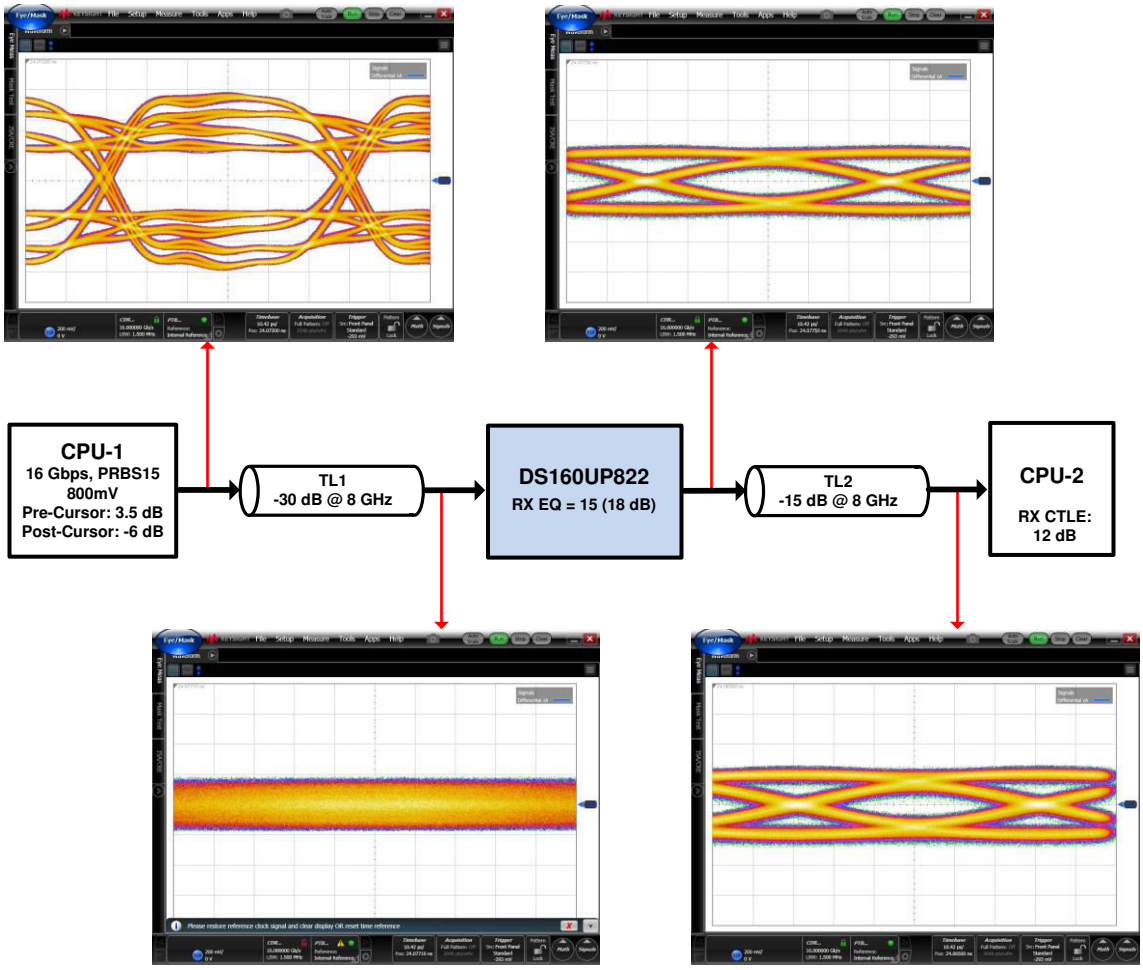


Figure 8-3. UPI 2.0 Link Reach Extension Using DS160UP822

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The DS160UP822 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 µF capacitor per VCC pin, one 1.0 µF bulk capacitor per device, and one 10 µF bulk capacitor per power bus that delivers power to one or more devices. The local decoupling (0.1 µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the device ground pad.
3. The DS160UP822 voltage regulator output pins require decoupling caps of 0.1 µF near each pins. The regulator is only for internal use. Do not use to provide power to any external component.

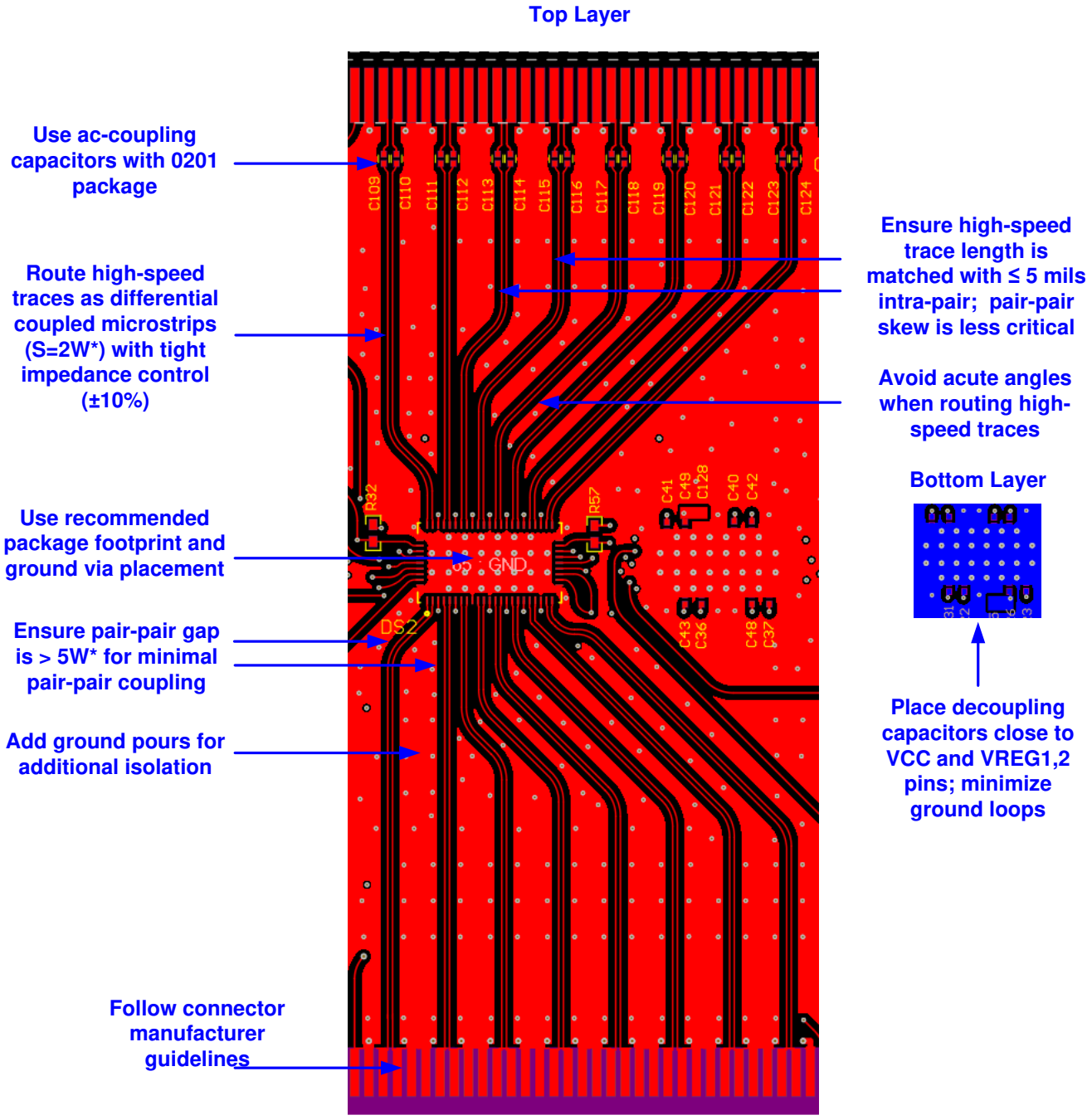
10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most/all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

10.2 Layout Example



*W is a trace width. S is a gap between adjacent traces.

Figure 10-1. DS160UP822 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

11.3 Trademarks

All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS160UP822NJXR	ACTIVE	WQFN	NJX	64	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PR8XX	Samples
DS160UP822NJXT	ACTIVE	WQFN	NJX	64	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PR8XX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

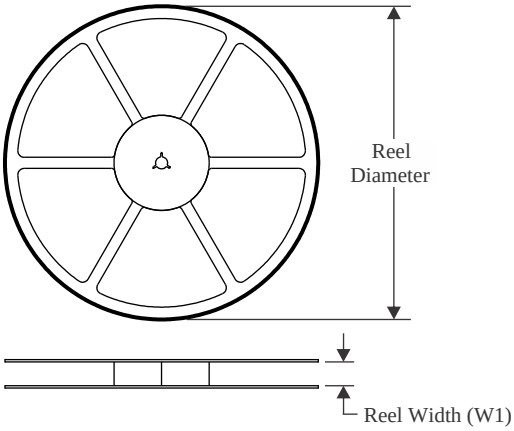
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

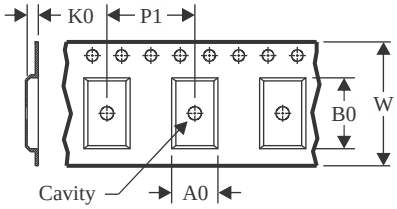
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

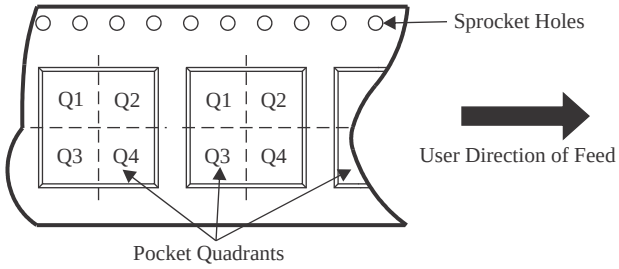


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

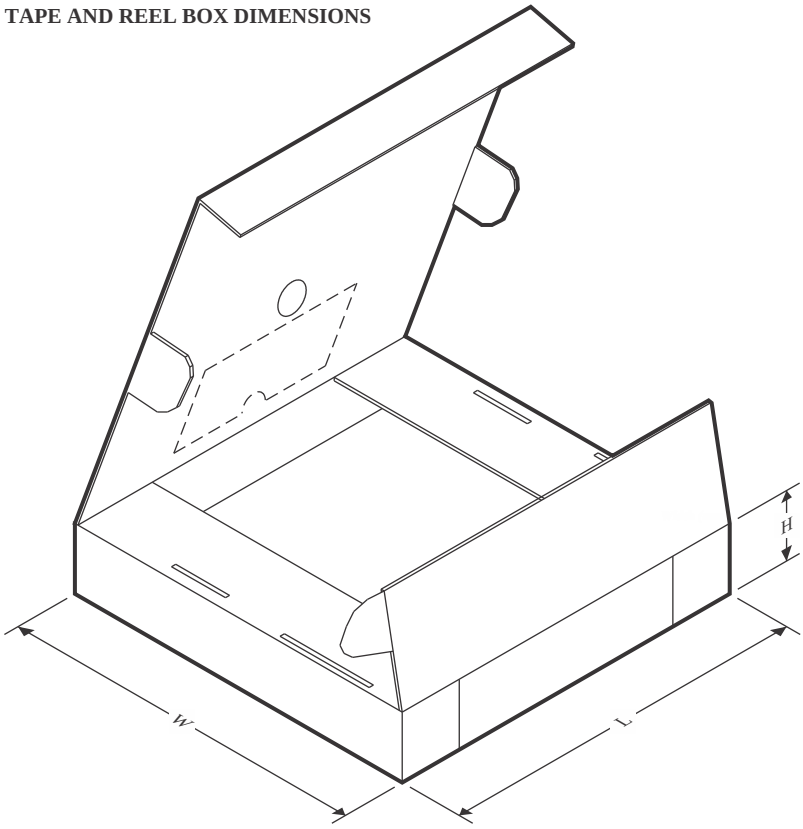
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS160UP822NJXR	WQFN	NJX	64	3000	330.0	16.4	5.8	10.3	1.2	12.0	16.0	Q1
DS160UP822NJXT	WQFN	NJX	64	250	180.0	16.4	5.8	10.3	1.2	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

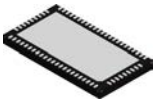


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS160UP822NJXR	WQFN	NJX	64	3000	367.0	367.0	35.0
DS160UP822NJXT	WQFN	NJX	64	250	210.0	185.0	35.0

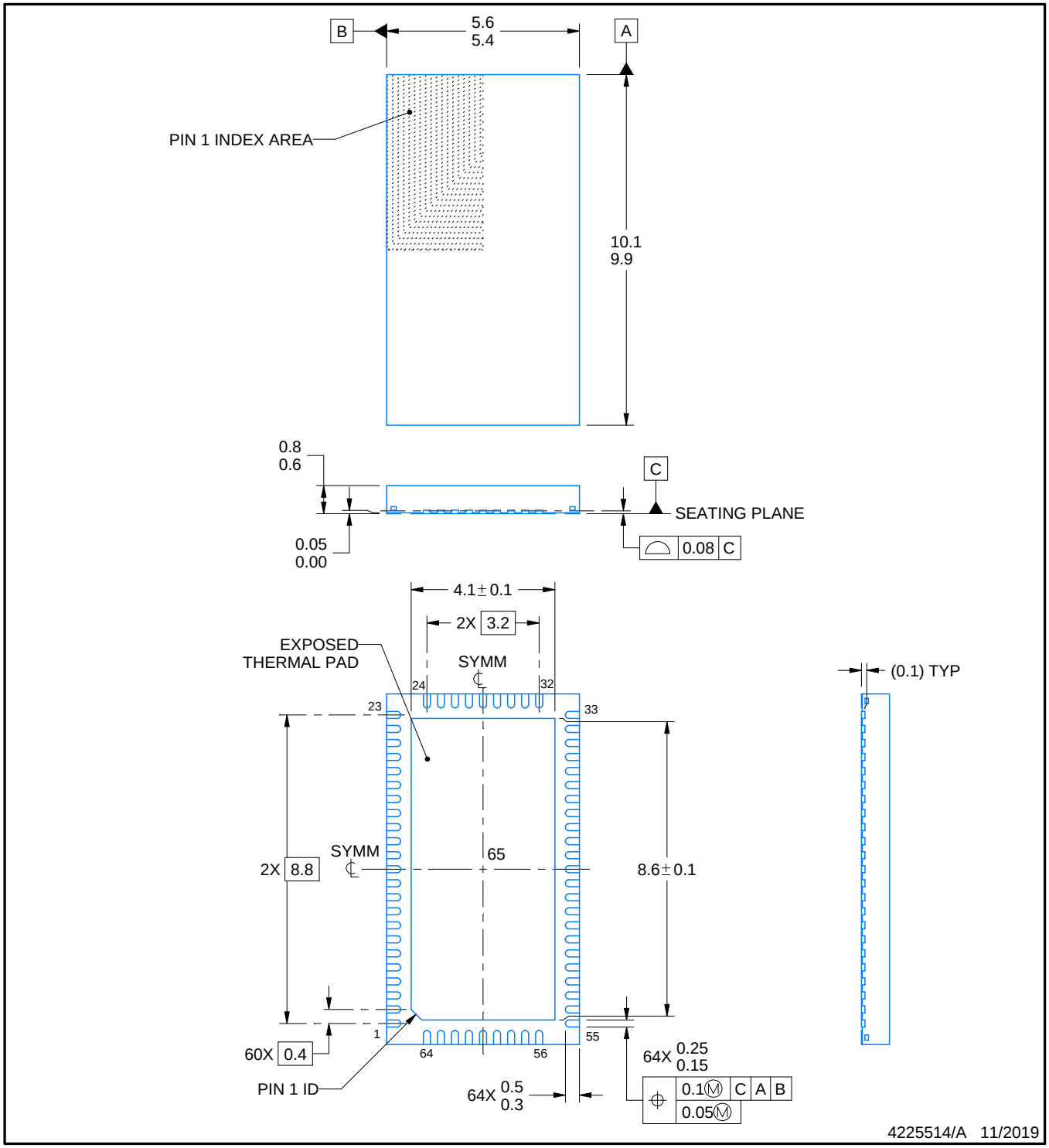
PACKAGE OUTLINE

NJX0064A



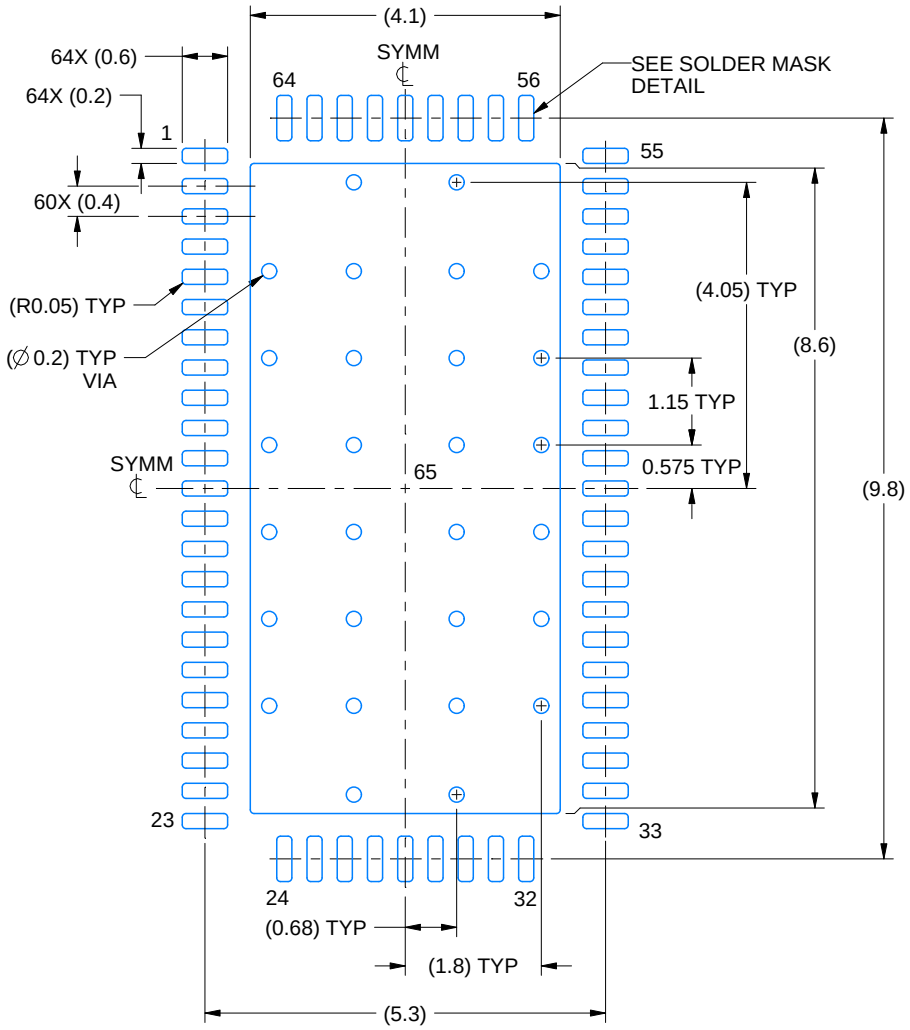
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

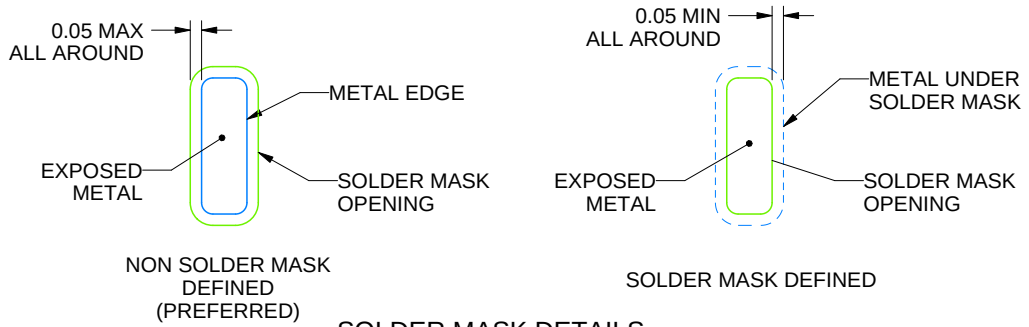


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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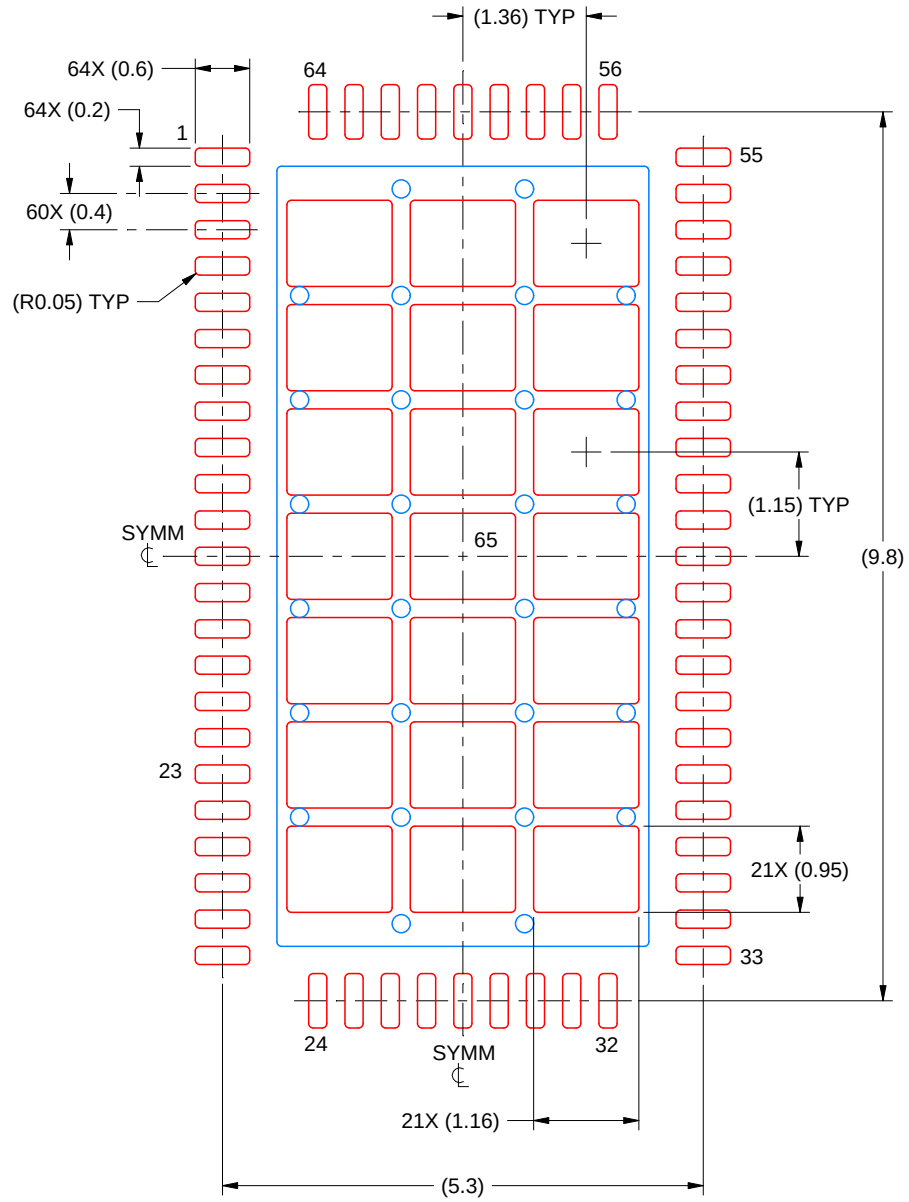
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 65
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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