TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

SSM6J206FE

Power Management Switch Applications

High-Speed Switching Applications

• 1.8 V drive

• Low ON-resistance: $R_{on} = 320 \text{ m}\Omega \text{ (max) (@V_{GS} = -1.8 V)}$

 R_{on} = 186 m Ω (max) (@V_{GS} = -2.5 V) R_{on} = 130 m Ω (max) (@V_{GS} = -4.0 V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit		
Drain-source voltage	V_{DS}	-20	V		
Gate-source voltage	V _{GSS}	± 8	V		
Drain current	DC	I _D	-2	Α	
	Pulse	I _{DP}	-4		
Drain power dissipation		P _D (Note 1)	500	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature		T _{stg}	-55 to 150	°C	

Note:

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ t}, \text{ Cu Pad: } 645 \text{ mm}^2)$

1.6±0.05 1.2±0.05 1.2±0.05 1, 2, 5, 6 : Drain 3 : Gate 4 : Source ES6 JEDEC — JEITA — TOSHIBA 2-2N1A

Weight: 3 mg (typ.)

Electrical Characteristics (Ta = 25°C)

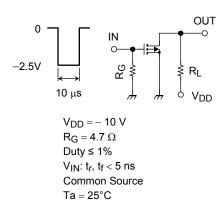
Charac	teristic	Symbol	Test Condition		Min	Тур.	Max	Unit
Drain–source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0$		-20	_	_	V
		V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-12	_	_	V	
Drain cutoff current	t	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0		_	_	-10	μА
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$		_	_	±1	μА
Gate threshold volt	age	V _{th}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V
Forward transfer a	dmittance	Y _{fs}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ A}$	(Note 2)	2.4	4	_	S
Drain-source ON-resistance		R _{DS (ON)}	I _D = -1.0 A, V _{GS} = -4 V	(Note 2)		91	130	mΩ
			I _D = -0.5 A, V _{GS} = -2.5 V	(Note 2)		130	186	
			I _D = -0.2 A, V _{GS} = -1.8 V	(Note 2)		180	320	
Input capacitance		C _{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$			335	_	pF
Output capacitance	;	Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$			70	_	pF
Reverse transfer ca	verse transfer capacitance C_{rss} $V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		Hz		56	_	pF	
Switching time	Turn-on time	t _{on}	$V_{DD} = -10 \text{ V}, I_{D} = -1 \text{ A},$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_{G} = 4.7 \Omega$		_	20	_	ns
	Turn-off time	t _{off}			_	20	_	
Drain-source forward voltage		V_{DSF}	$I_D = 2 \text{ A}, V_{GS} = 0$ (Note 2)		_	0.85	1.2	V

Note 2: Pulse test

Start of commercial production 2005-11

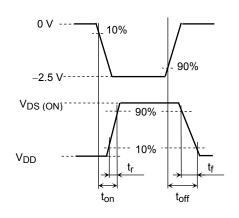
Switching Time Test Circuit

(a) Test circuit



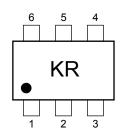
(b) V_{IN}

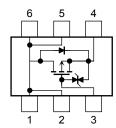
(c) V_{OUT}



Marking

Equivalent Circuit (top view)





Notice on Usage

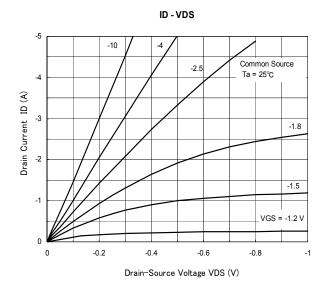
 V_{th} can be expressed as the voltage between gate and source when the low operating current value is I_D = -1 mA for this product. For normal switching operation, V_{GS} (on) requires a higher voltage than V_{th} and V_{GS} (off) requires a lower voltage than V_{th} .

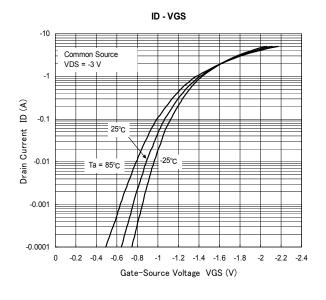
(The relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on).)

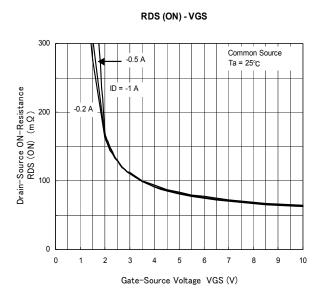
Take this into consideration when using the device.

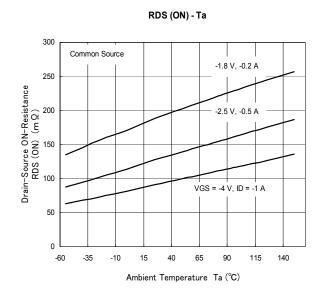
Handling Precaution

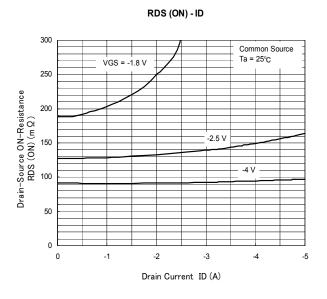
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

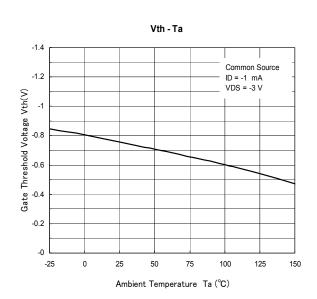


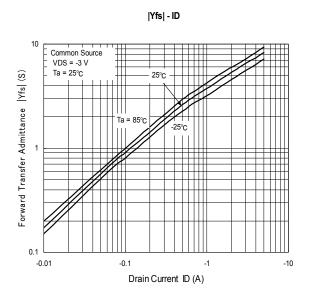


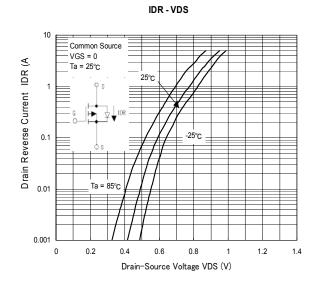


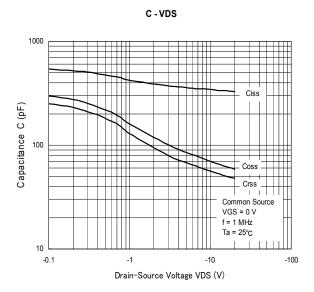


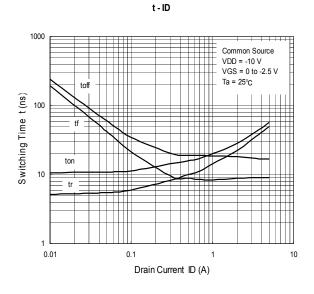


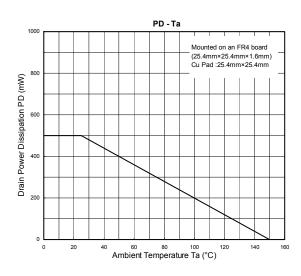












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