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DM74S161 • DM74S163 Synchronous 4-Bit Binary Counters

General Description

FAIRCHILD

SEMICONDUCTOR

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positivegoing) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a LOW level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be HIGH to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a HIGH-level output pulse with a duration approximately equal to the HIGH-level portion of the Q_A output. This HIGH-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Ordering Code:

Order Number	Package Number	Package Description
DM74S161N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74S163N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Connection Diagram





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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	
V _{CC}	Supply Voltage		4.75	5	5.25	V	
V _{IH}	HIGH Level Input Voltage		2			V	
V _{IL}	LOW Level Input Voltage				0.8	V	
I _{OH}	HIGH Level Output Current				-1	mA	
I _{OL}	LOW Level Output Current				20	mA	
f _{CLK}	Clock Frequency (Note 2)		0		40	MHz	
	Clock Frequency (Note 3)		0		35		
t _W	Pulse Width (Note 2)	Clock	10			ns	
		Clear (Note 5)	10				
	Pulse Width (Note 3)	Clock	12			-	
		Clear (Note 5)	12				
t _{SU}	Setup Time (Note 2)	Data	4			ns	
		Enable P or T	12				
		Load	14				
		Clear (Note 4)	14				
	Setup Time (Note 3)	Data	5				
		Enable P or T	14				
		Load	16				
		Clear (Note 4)	16				
t _H	Hold Time (Note 2)	Data	3			ns	
		Others	0			1	
	Hold Time (Note 3)	Data	5			1	
		Others	2			1	
t _{REL}	Load or Clear Release Time (Note 2)		12			ns	
	Load or Clear Release Time (Note 3)		14			115	
T _A	Free Air Operating Temperature		0		70	°C	

Note 2: C_L = 15 pF, R_L = 280 $\Omega,~T_A$ = 25 $^{\circ}C$ and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: Applies only to the DM74S163 which has synchronous clear inputs.

Note 5: Applies only to the DM74S161 which has asynchronous clear inputs.

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Electrical Characteristics

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units	
V _I	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.2	V	
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min		2.7	3.4		V	
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IH} = Min, V_{IL} = Max$				0.5	V	
1	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$				1	mA	
IIH	LOW Level	V _{CC} = Max	CLK, Data			50		
	Input Current	$V_{I} = 2.7V$	Others	-10		-200	μA	
-1L	LOW Level	V _{CC} = Max	Enable T			-4	mA	
	Input Current	$V_{I} = 0.5V$	Others			-2		
OS	Short Circuit Output Current	V _{CC} = Max (Note 7)		-40		-100	mA	
CC	Supply Current	V _{CC} = Max			95	160	mA	

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

Symbol	Parameter	From (Input) To (Output)	$R_L = 280\Omega$				
			C _L = 15 pF		$C_L = 50 \text{ pF}$		Units
			Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency		40		35		MHz
t _{PLH}	Propagation Delay Time	Clock to Ripple Carry		25		25	ns
	LOW-to-HIGH Level Output						
t _{PHL}	Propagation Delay Time	Clock to Ripple Carry		25		28	ns
	HIGH-to-LOW Level Output			20			
t _{PLH}	Propagation Delay Time	Clock to Any Q		15		15	ns
	LOW-to-HIGH Level Output			10			
t _{PHL}	Propagation Delay Time	Clock to Any Q	15	15	15	18	ns
	HIGH-to-LOW Level Output			15			
t _{PLH}	Propagation Delay Time	Enable T to Ripple Carry		15		18	ns
	LOW-to-HIGH Level Output						
t _{PHL}	Propagation Delay Time	Enable T to Ripple Carry		15		18	
	HIGH-to-LOW Level Output			15		10	ns
t _{PHL}	Propagation Delay Time	Ole and a Anna O	20		24		
	HIGH-to-LOW Level Output (Note 8)	Clear to Any Q		20		24	ns

Note 8: Propagation delay for clearing is measured from clear input for the DM74S161 and from the clock input transition for the DM74S163.

