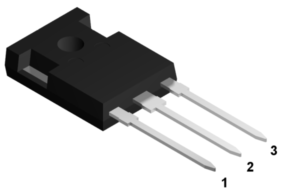
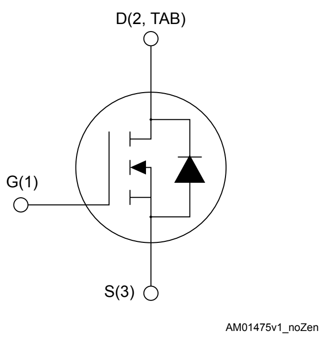
N-channel 650 V, 19.9 mΩ typ., 95 A MDmesh M9 Power MOSFET in a TO-247 long leads package



TO-247 long leads



Product status link
STWA65N023M9

Product summary	
Order code	STWA65N023M9
Marking	65N023M9
Package	TO-247 long leads
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STWA65N023M9	650 V	23.0 mΩ	95

- Worldwide best FOM $R_{DS(on)}$*Q_g among silicon-based devices
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

Applications

- High efficiency switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low $R_{DS(on)}$ per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	95	A
	Drain current (continuous) at T_C = 100 °C	60	
I_{DM} (2)	Drain current (pulsed)	440	A
P_{TOT}	Total power dissipation at T_C = 25 °C	463	W
dv/dt (3)	Peak diode recovery voltage slope	50	V/ns
di/dt (3)	Peak diode recovery current slope	900	A/µs
dv/dt (4)	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Referred to TO-247 package.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 48 A, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.27	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	12	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	1307	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C[(1)]			200	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 48 A		19.9	23.0	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 400 V, f = 1 MHz, V_{GS} = 0 V	-	8844	-	pF
C_{oss}	Output capacitance		-	140	-	pF
$C_{oss\ eq.}$[(1)]	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	1750	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, open drain	-	0.8	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 48 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	230	-	nC
Q_{gs}	Gate-source charge		-	52	-	nC
Q_{gd}	Gate-drain charge		-	108	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 48 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 17. Turn-off switching time waveform on inductive loadFigure 5)	-	140	-	ns
$t_{r(v)}$	Voltage rise time		-	4	-	ns
$t_{f(i)}$	Current fall time		-	33	-	ns
$t_{c(off)}$	Crossing time off		-	38	-	ns
$t_{d(i)}$	Current delay time	V_{DD} = 400 V, I_D = 48 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 18. Turn-on switching time waveform on inductive load)	-	47	-	ns
$t_{r(i)}$	Current rise time		-	64	-	ns
$t_{f(v)}$	Voltage fall time		-	70	-	ns
$t_{c(on)}$	Crossing time on		-	90	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		95	A
I_{SDM} (2)	Source-drain current (pulsed)		-		440	A
V_{SD} (3)	Forward on voltage	I_{SD} = 95 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 95 A, di/dt = 100 A/µs,	-	330		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	5.45		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 95 A, di/dt = 100 A/µs,	-	465		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	10.85		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	34		A

1. *Referred to TO-247 package.*
2. *Pulse width is limited by safe operating area.*
3. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

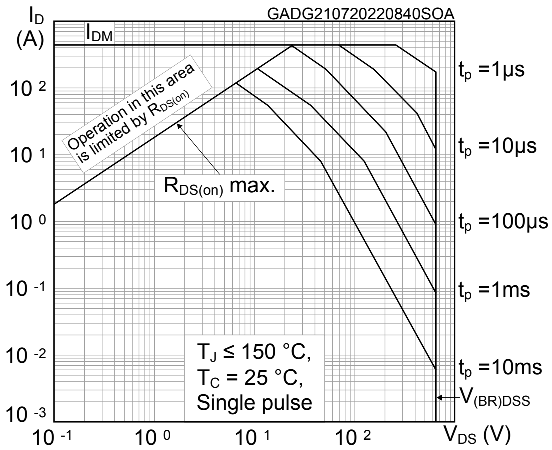


Figure 2. Maximum transient thermal impedance

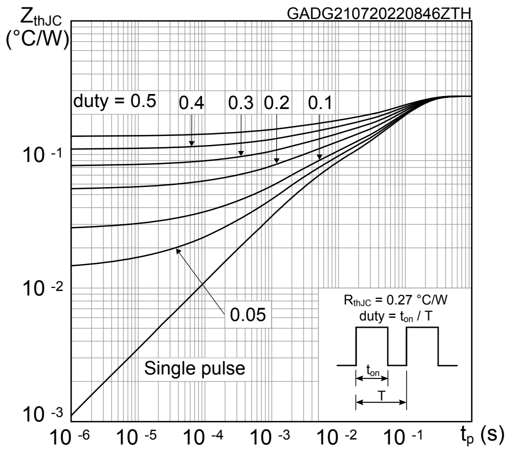


Figure 3. Typical output characteristics

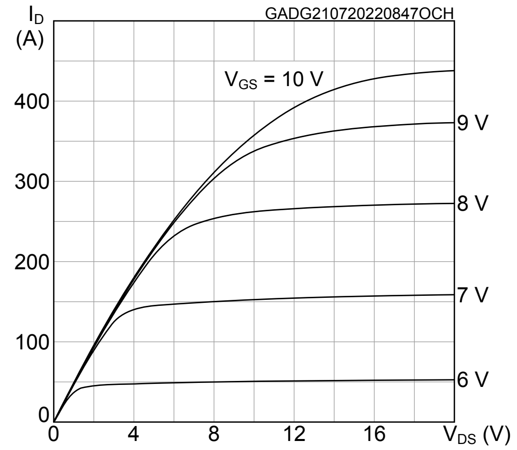


Figure 4. Typical transfer characteristics

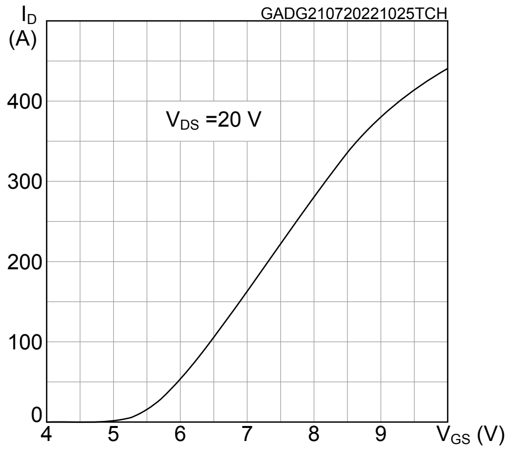


Figure 5. Typical gate charge characteristics

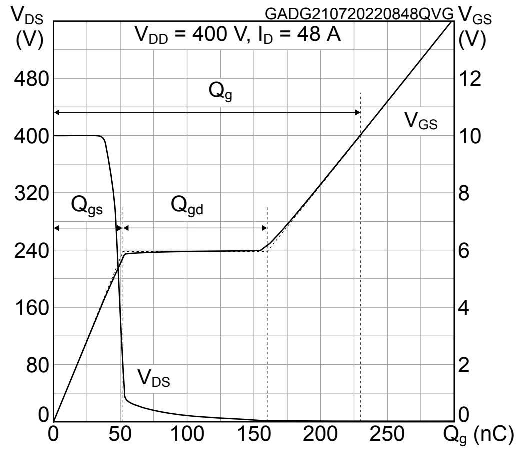


Figure 6. Typical capacitance characteristics

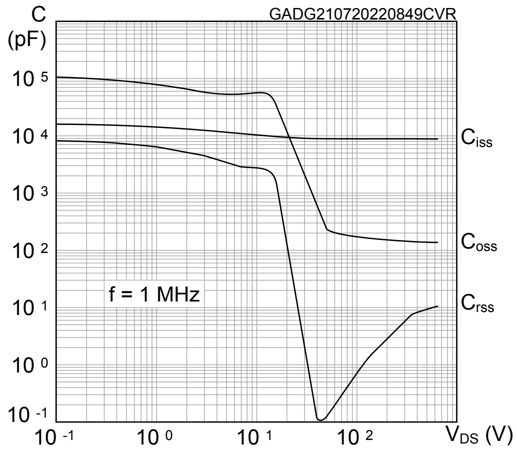


Figure 7. Typical drain-source on-resistance

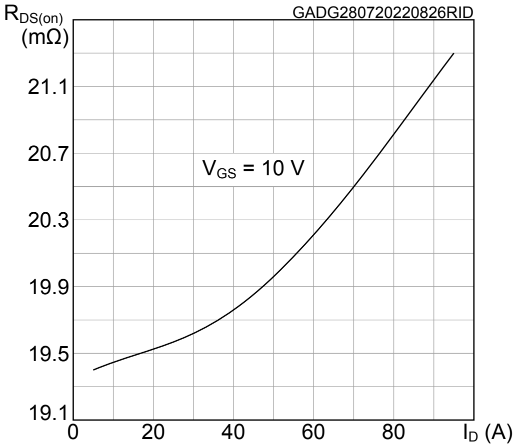


Figure 8. Normalized on-resistance vs temperature

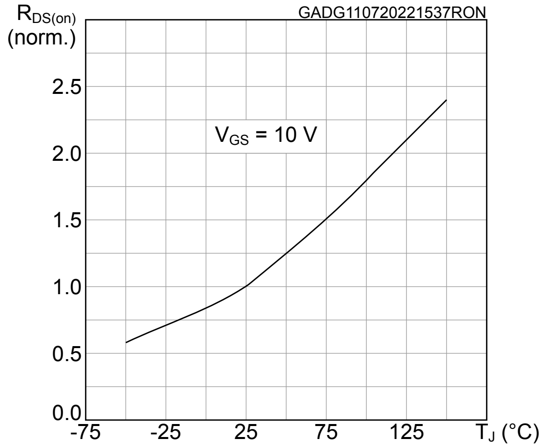


Figure 9. Normalized gate threshold vs temperature

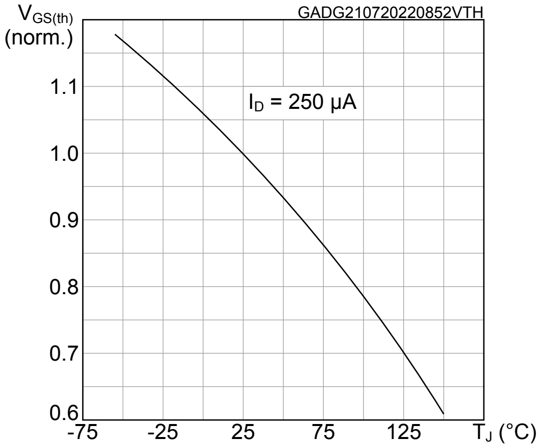


Figure 10. Normalized breakdown voltage vs temperature

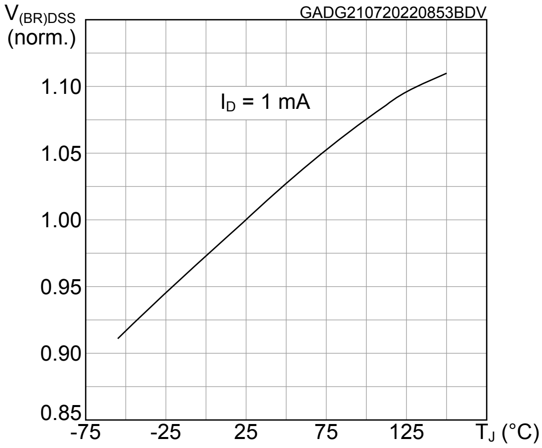


Figure 11. Typical reverse diode forward characteristics

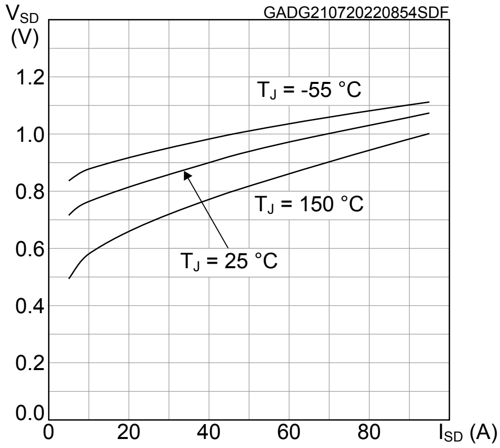
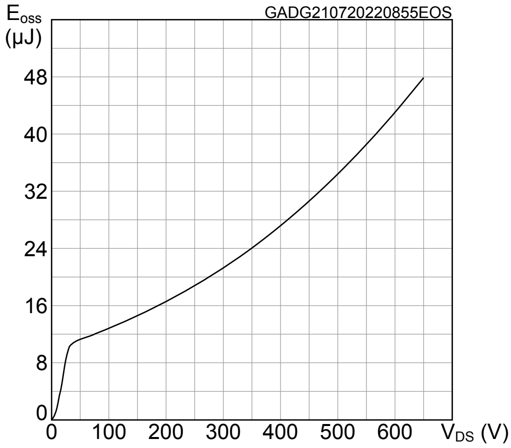


Figure 12. Typical output capacitance stored energy



3 Test circuits

Figure 13. Unclamped inductive load test circuit

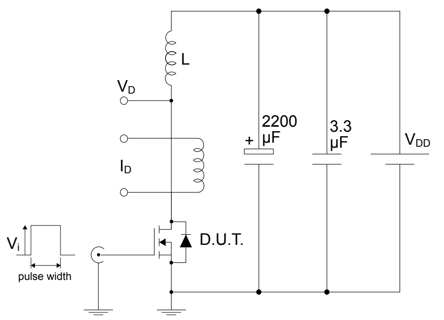


Figure 14. Unclamped inductive waveform

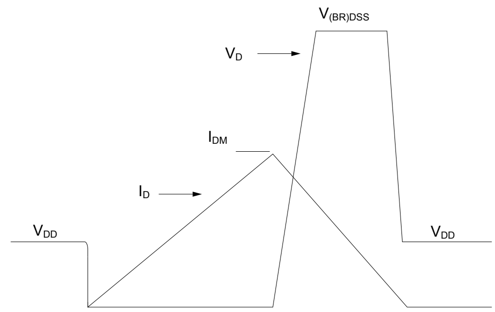


Figure 15. Test circuit for gate charge behavior

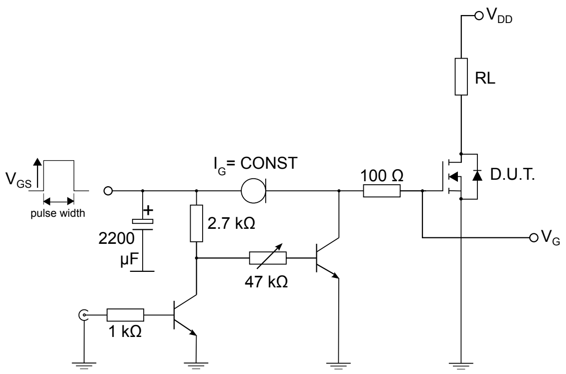


Figure 16. Test circuit for inductive load switching and diode recovery times

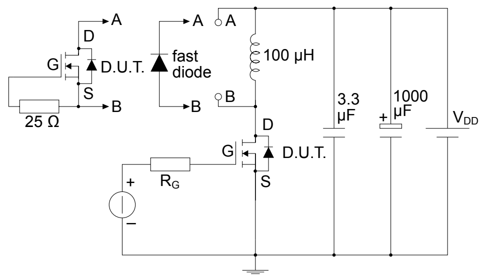


Figure 17. Turn-off switching time waveform on inductive load

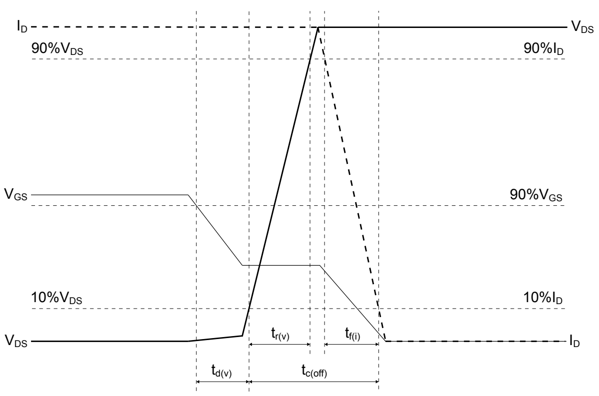
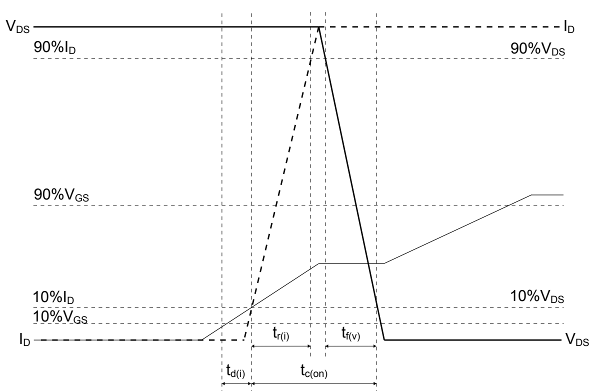


Figure 18. Turn-on switching time waveform on inductive load



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 19. TO-247 long leads package outline

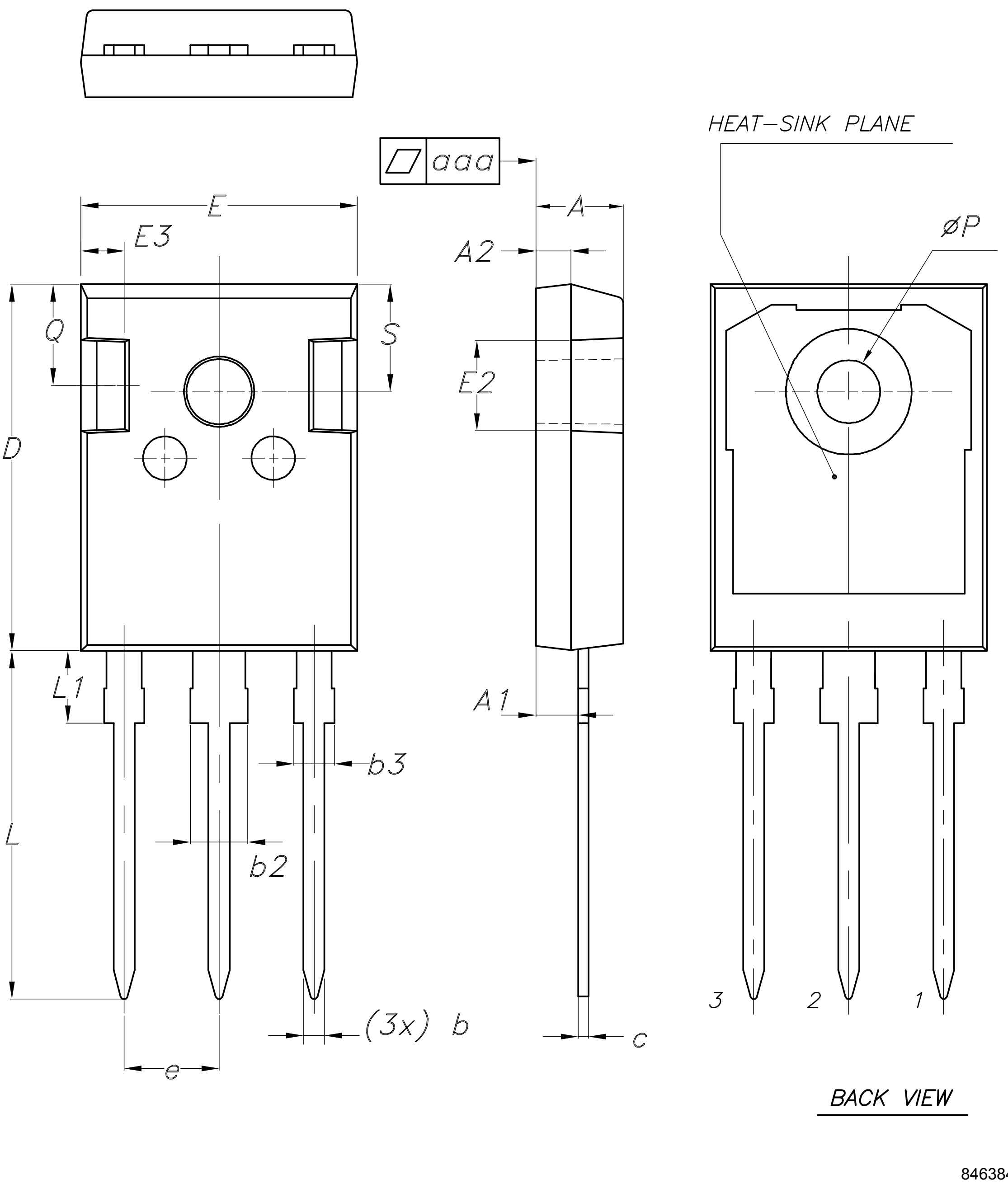


Table 8. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25
aaa		0.04	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Dec-2022	1	First release.
27-Feb-2023	2	Updated Table 4. On-/off-states.

Contents