



Si5341-D EVALUATION BOARD USER'S GUIDE

Description

The Si5341-D-EVB is used for evaluating the Si5341 Any-Frequency, Any-Output, Jitter-Attenuating Clock Multiplier revision D. The device revision is distinguished by a white 1 inch x 0.187 inch label with the text "SI5341-D-EB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)

EVB Features

- Powered from USB port or external power supply.
- Onboard 48 MHz XTAL allows free-run mode of operation on the Si5341 or up to 3 input clocks for synchronous clocking.
- Feedback clock input for optional zero delay mode.
- CBProTM GUI programmable V_{DD} supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable V_{DDO} supplies allow each of the 10 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI-controlled voltage, current, and power measurements of V_{DD} and all V_{DDO} supplies.
- Status LEDs for power supplies and control/status signals of Si5341.
- SMA connectors for input and output clocks.



Figure 1. Si5341-D Evaluation Board

1. Functional Block Diagram

Below is a functional block diagram of the Si5341-D-EB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See section "3. Quick Start" or section "8. Installing ClockBuilderPro (CBPro) Desktop Software" for more information.



Figure 2. Si5341-D-EB Functional Block Diagram



2. Si5341-D-EVB Support Documentation and ClockBuilderPro™Software

All Si5341-D-EVB schematics, BOMs, User's Guides, and software can be found online at the following link: http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

3. Quick Start

- 1. Install ClockBuilderPro desktop software from http://www.silabs.com/CBPro.
- 2. Connect a USB cable from Si5341-D-EB to the PC where the software was installed.
- 3. Leave the jumpers as installed from the factory, and launch the ClockBuilderPro software.
- 4. You can use ClockBuilderPro to create, download, and run a frequency plan on the Si5341-D-EB.
- 5. For the Si5341 data sheet, go to http://www.silabs.com/timing.



4. Jumper Defaults

Location	Туре	I = Installed 0 = Open		Location	Туре	l = Installed 0 = Open
JP1	2 pin	0		JP23	2 pin	0
JP2	2 pin	I		JP24	2 pin	0
JP3	2 pin	0		JP25	2 pin	0
JP4	2 pin	I		JP26	2 pin	0
JP5	2 pin	I		JP27	2 pin	0
JP6	2 pin	I		JP28	2 pin	0
JP7	2 pin	I		JP29	2 pin	0
JP8	2 pin	I		JP30	2 pin	0
JP9	2 pin	0		JP31	2 pin	0
JP10	2 pin	I		JP32	2 pin	0
JP13	2 pin	0		JP33	2 pin	0
JP14	2 pin	I		JP34	2 pin	0
JP15	3 pin	1 to 2		JP35	2 pin	0
JP16	3 pin	1 to 2		JP36	2 pin	0
JP17	2 pin	0		JP38	3 pin	All Open
JP18	2 pin	0		JP39	2 pin	0
JP19	2 pin	0		JP40	2 pin	0
JP20	2 pin	0		JP41	2 pin	0
JP21	2 pin	0		J36	5 x 2 Hdr	All 5 installed
JP22	2 pin	0				
Note: Refer to	the Si5341	-D-EB schematics for	the	functionality ass	sociated with ea	ich jumper.

Table 1. Si5341-D-EB Jumper Defaults

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5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D27	5VUSBMAIN	Blue	Main USB +5 V present
D22	3P3V	Blue	DUT +3.3 V is present
D26	VDD DUT	Blue	DUT VDD voltage present
D25	INTR	Red	MCU INTR (Interrupt) active
D21	READY	Green	MCU Ready
D24	BUSY	Green	MCU Busy

Table 2. Si5341-D-EB Status LEDs

D27, D22, and D26 are illuminated when USB +5 V, Si5341 +3.3 V, and Si5341 V_{DD} supply voltages, respectively, are present. D25, D21, and D24 are status LEDs showing on-board MCU activity.



Figure 3. Status LEDs



6. Clock Input Circuits (INx/INxB and FB_IN/FB_INB)

The Si5341-D-EB has eight SMA connectors (IN0/IN0B–IN2/IN3B and FB_IN/FB_INB) for receiving external clock signals. All input clocks are terminated as shown in Figure 4 below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5341 data sheet.



Figure 4. Input Clock Termination Circuit

7. Clock Output Circuits (OUTx/OUTxB)

Each of the twenty output drivers (10 differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 5 below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5341-D-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with schematic "NI" designation are not normally populated on the Si5341-D-EB and provide locations on the PCB for optional dc/ac terminations by the end user.



Figure 5. Output Clock Termination Circuit



8. Installing ClockBuilderPro (CBPro) Desktop Software

To install the CBOPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilderPro software.

Installation instructions and User's Guide for ClockBuilderPro can be found at the download link shown above. Please follow the instructions as indicated.

9. Using the Si5341-D-EVB

9.1. Connecting the EVB to Your Host PC

Once ClockBuilderPro software is installed, connect to the evaluation board with a USB cable as shown below.



Figure 6. EVB Connection Diagram



9.2. Additional Power Supplies

Although additional power (besides the power supplied by the host PC's USB port) is not needed for most configurations, two additional +5 VDC power supplies (MAIN and AUX) can be connected to J33 and J34 (located on the bottom of the board, near the USB connector). Refer to the Si5341-D-EB schematic for details.

The Si5341-EB comes preconfigured with jumpers installed at JP15 and JP16 (pins 1-2 in both cases) in order to select "USB". These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J37. This setup is the default configuration and should normally be sufficient.

Figure 7 shows the correct installation of the jumper shunts at JP15 and JP16 for default or standard operation.



Figure 7. JP15-JP16 Standard Jumper Shunt Installation

Errata Note:Some early versions of the 64-pin Si534x-EBs may have the silkscreen text at JP15-JP16 reversed regarding EXT and USB, i.e., USB EXT instead of EXT USB. Regardless, the correct installation of the jumper shunts for default or standard operation is on the right hand side as read and viewed in Figure 7.

The general guidelines for single USB power supply operation are listed below:

- Use either a USB 3.0 or USB 2.0 port. These ports are specified to supply 900 mA and 500 mA respectively at +5 V.
- If you are working with a USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤ 470 mA. (Note: USB 2.0 ports may supply > 500 mA. Provided the nominal +5 V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 2.0 and you are current limited and need all output clock drivers enabled, re-configure the EB to drive the DUT output voltage regulators from an external +5 V power supply as follows:
 - Connect external +5 V power supply to terminal block J33 on the back side of the PCB.
 - Move the jumper at JP15 from pins 1-2 USB to pins 2-3 EXT.



9.3. Overview of ClockBuilderPro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilderPro[™] installer will install **two** main applications:



Figure 8. Application #1: ClockbuilderPro Wizard

Use the CBPro Wizard to:

- Create a new design
- Review or edit an existing design
- Export: create in-system programming

the DUTSPI D	C DUT	Repe	er Editor	Repulators	Al voltages	GPI0 Status	Registers	· Control Weighters
				Voltag	Carter	nt Power		Soft Reset and Calibrat
VDD	1.807		04		ý	4 ···· V	Read	SOFT_RET
VODA			01	1 144	V	A	Read	Hard Reset, Sync, &
VD000	2.50V		01	9 -	· · · · ·	A	Read	Power Down
Y0001	2.57V	12	01	· · · · ·	Ý	A W	Kead	HARD_RST
V0002	2.304	12	0	-	v —	4	Read	SYNC
VDDOJ	2.50V		01	1	v +	A V	Red	PDN 0
V0004	2.50V		05	1	·	A	Read	Frequency Adjust
VDDDS	2.50V		0	2	v	A V	Read	FINC
V0006	2.50V	1	On I		ų (m.	a v	Real	FOEC
V0007	2.50V		01	1.000	¥ 4	A V	Read	
V0008	2.50V		01	1	v	A	Reat	
V0009	2.50V		0		v	a v	Read	
Al Cutput	Select	/oltarje	- 1	Teta	÷ –	A	V Read All	
Supplies 1	Power	06	Power Of	1	Compare Desk	pri Estimates to	Measurements -	

Figure 9. Application #2: EVB GUI

Use the EVB GUI to:

- Download configuration to EVB's DUT (Si5341)
- Control the EVB's regulators
- Monitor voltage, current, power on the EVB



9.4. Common ClockBuilderPro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5341-D-EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

9.5. Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 10. ClockBuilderPro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



Figure 11. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

Write Desig	n to EVB?	
	be out-of-sync with your design. Would y	ou like to
write your de	sign to the EVB?	

Figure 12. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5341 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.



(B Si5341 Design Write	
	Writing Si5341 Design to EVB Address 0x0119	

Figure 13. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.



Figure 14. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown below.

tfo DUTSPI L	2C DUT Re	gister Editor	Regulators	All Voltages	GPIO	Status Register	\$
			Voltage	Curre	nt	Power	
VDD	1.80V	On	1.306 V	488	mA	637 mW	Read
VDDA		On	3.294 V	112	mA	369 mW	Read
VDD00	2.50V	- On	2.514 V	14	мA	35 mW	Read
VDD01	2.50V	On	2.500 V	17	mĄ	43 mW	Read
VDDO2	2.50V	On .	2.507 V	14	mA.	35 mW	Read
VDD03	2.50V	On	2.496 V	14	mA	35 mW	Read
VDDO4	2.50V	- On	2.499 V	15	mA	37 mW	Read
VDDO5	2.50V	On	2.501 V	16	mA	40 mW	Read
VDDO6	2.50V	On	2.504 V		mA	35 mW	Read
VDDO7	2.50V	- On	2.485 V	14	Am	35 mW	Read
VDD08	2.50V	On	2.500 V	14	mA	35 mW	Read
VDD09	2.50V	- On	2.490 V	16	mA	40 mW	Read
All Output	Select Volt	00.011	Total	748	mA	1.376 W	Read Al

Figure 15. EVB GUI Window



9.5.1. Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":



Figure 16. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.



Figure 17. View Design Report



Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

Design Repor	t :	
5153418	100 Hr to 350 MHr *	14
\$19341C	100 Hz to 800 MHz Integer (150 fs) only	
\$153410	100 Hz to 350 MHz *	- 0
· Based or	your calculated frequency plan, a Sil341A grade device is	
required information	for your design. See the datasheet Ordering Guide for more Mn.	
Design		
Host Inte		
	ver Supply: VDD (Core) Se: 5-Nire	
	irens Hange: 116d to 119d / 0w74 to 0x77 (selected via AD/A1 pins)	
XA/X8:		
	(XTAL - Crystal)	
Inputes		
	48 10Kz	
	Differential	
	45 101z	
	Differential	
	(# 10fa	
33	Differential	
Outputsi		
	161.1528125 MMz [161 + 17/128 MMz]	
	Enabled, LVDH 2.5 V	
	(25 M)r	
	Inabled, 1903 3.5 V	
	156.25 MHz (156 + 1/4 MHz)	
	Enabled, LVDS 2.8 V	
	156.25 MOR [156 + 1/4 MRz] Inabled, LVDS 2.5 V	
	168.041015625 HBHz (168 + 21/513 HBHz) Enabled, LVDS 2.5 V	
	672.1640625 MHz [672 + 21/128 MHz]	
	Inabled, LVDS 2.5 V	
	174.7030837004405266 HHz (174 + 798/1105 NHz)	
	Inabled, LVDS 2.5 V	
	155.52 30Kz [155 + 13/25 30Kz]	
	Inabled, LVDS 2.5 V	
	155.52 101x (155 + 13/25 101x)	
112263	Inabled, LVDS 2.5 V	
107791	(22.08 MHz [622 + 2/28 MHz]	
100000	Inabled, LVDS 2.5 V	
		_
Copy to Clip	board Save Report Clo	

Figure 18. Design Report Window

9.5.2. Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.



9.6. Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



Figure 19. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

SISSAE EVE Diversity	Configuration - Dookhadder Pro	12:15				
	er Pro voor 🗣 standard heppensystement des antres svensleit	SILICON LAB				
tep 1 af 8 - Des	ign ID & Notes 🔻	Configuring SiS3				
Design ID The device has 8 r	registers. DESIGN 300 through DESIGN JD7, that can be used to store a design-configurat	Son, www.sigen.identifiler.				
Denign ID:	33436V83 (optional) mas 8 characters) The string you enter here is stored as ASC8 bytes in registers DCSRCH_300 through DC	SIGH (107,				
Padding Mode	INVLL Padded If you do not enter the full 8 characters, the reamining bytes of DESIGH JDx will b character).	e padded with 0x00 bytes (aka NULL				
	Space Padded If you do not ense the full I characters, the rearring bytes of OCSION, Dox will be padded with brook bytes (space character).					
Design Notes Enter anything yo	u want here. The text is stored in your project file and included in design reports (future f	natures.				
D Internet Par	Notes Constant OK Cope 1287 W. 12 97 TC Notes 10 295	t Next > Finish Carcel				

Figure 20. Design Wizard



Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

CB Si5341 Design Write	
Writing Si5341 Design to EVB Address 0x0119	

Figure 21. Writing Design Status

9.7. Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.

CoddSulder Pro Witterd - Silicon Lafa	
SILICOL LABS We Make Timing Simp	0
Work With a Design	Quick Links
Create New Design	litter Attenuator Clock Products
Dopen Design Project File	Knowledge Base Custom Part Number Lookup ClockBuilder Go IOS App
ex Open Sample Design	PROVIDE THE DOUBLE
Evaluation Board Detected Si5341 EVB Open Default Plan Open EVB GUL	
Quick Tools	
Export Configuration	
O ₄ instrumes	Version 3.304 Built on 7/3//2014

Figure 22. Open Design Project File



Si5341-D-EVB

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.



Figure 23. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:



Figure 24. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.



9.8. Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:



Figure 25. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.



Figure 26. Export Settings



10. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is **NOT** the same as writing a configuration into the Si5341 using Clock-BuilderPro on the Si5341-D-EB. Writing a configuration into the EVB from ClockBuilderPro is done using Si5341 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si534x/8x Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of **two** times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

11. Si5341-D-EVB Schematic and Bill of Materials (BOM)

The Si5341-D-EVB Schematic and Bill of Materials (BOM) can be found online at

http://www.silabs.com/products/clocksoscillators/pages/si538x-4x-evb.aspx

Note: Please be aware that the Si5341-D-EB schematic is in OrCad Capture *hierarchical format* and not in a typical "flat" schematic format.





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