

SX1504/SX1505/SX1506

4/8/16 Channel GPIO with NINT and NRESET

GENERAL DESCRIPTION

The SX1504, SX1505 and SX1506 are complete General Purpose parallel Input/Output (GPIO) expanders ideal for low power handheld battery powered equipment. They allow easy serial expansion of I/O through a standard I²C interface. GPIO devices can provide additional control and monitoring when the microcontroller or chipset has insufficient I/O ports, or in systems where serial communication and control from a remote location is advantageous.

These devices can also act as a level shifter to connect a microcontroller running at one voltage level to a component running at a different voltage level. The core is operating as low as 2.5V while the I/O banks can operate between 2.5V and 5.5V independent of the core voltage and each other.

Each GPIO is programmable via 8-bit configuration registers. Data registers, direction registers, pull-up/pull-down registers, interrupt mask registers and interrupt registers allow the system master to program and configure 4 or 8 or 16-GPIOs using a standard 400kHz I²C interface.

The SX1504, SX1505 and SX1506 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications.

The SX1504, SX1505 and SX1506 have the ability to generate mask-programmable interrupts based on falling/rising edge of any of its GPIO lines. A dedicated pin indicates to a host controller that a state change occurred in one or more of the GPIO lines.

The SX1504, SX1505 and SX1506 each come in a small QFN-UT-20/28 package. All devices are rated from -40 $^{\circ}$ to +85 $^{\circ}$ temperature range.

ORDERING INFORMATION

Part Number	I/O Channels	Package
SX1504I087TRT	4	QFN-UT-20
SX1505I087TRT	8	QFN-UT-20
SX1506I091TRT	16	QFN-UT-28
SX1502EVK ⁽¹⁾	8	Evaluation Kit

⁽¹⁾SX1502l087TRT based, unique evaluation kit for the three parts.

KEY PRODUCT FEATURES

- 4/8/16 channel of I/Os
 - True bi-directional style I/O
 - Programmable Pull-up/Pull-down
 - Push/Pull outputs
- 2.5V to 5.5V independent operating voltage for all supply rails (VDDM, VCC1, VCC2)
- 5.5V compatible I/Os, up to 24mA output sink (no total sink current limit)
- Fully programmable logic functions (PLD)
- 400kHz 2-wire I²C compatible slave interface
- Open drain active low interrupt output (NINT)
 Bit maskable
 - Programmable edge sensitivity
- Power-On Reset and reset input (NRESET)
- Ultra low current consumption of typ. 1uA
- -40℃ to +85℃ operating temperature range
- Ultra-Thin 3x3mm QFN-UT-20 package (SX1504/SX1505)
- Ultra-Thin 4x4mm QFN-UT-28 package (SX1506)
- Pb & Halogen Free, RoHS/WEEE compliant

TYPICAL APPLICATIONS

- Cell phones, PDAs, MP3 players
- Digital camera
- Portable multimedia player
- Notebooks
- GPS Units
- Industrial, ATE
- Any battery powered equipment





Table of Contents

GI	ENERAL	DESCRIPTION	. 1				
OI	ORDERING INFORMATION						
K	ey Pro	DUCT FEATURES	. 1				
ΤY	PICAL	APPLICATIONS	. 1				
1	PIN	DESCRIPTION	. 4				
	1.1	SX1504 4-channel GPIO	4				
	1.2	SX1505 8-channel GPIO	5				
	1.3	SX1506 16-channel GPIO	6				
2	ELE	CTRICAL CHARACTERISTICS	. 7				
	2.1	Absolute Maximum Ratings	7				
	2.2	Electrical Specifications	7				
3	TYF	PICAL OPERATING CHARACTERISTICS	10				
	3.1	IDDM vs. VDDM	10				
	3.2	VOL vs. IOL	10				
	3.3	VOH vs. IOH	11				
4	BLC	OCK DETAILED DESCRIPTION	12				
	4.1	SX1504 4-channel GPIO	12				
	4.2	SX1505 8-channel GPIO	12				
	4.3	SX1506 16-channel GPIO	13				
	4.4		13				
	4.5 4.5.		14 14				
	4.5.		14				
	4.5.3		15				
	4.6		16				
	4.7	5 5 7	16 16				
	4.7.		17				
			17				
_	4.7.4		18				
5			19				
	5.1		19				
	5.2		20				
_	5.3		22				
6	APF		26				
	6.1		26				
	6.2 6.2.		26 26				
	6.2.		20 27				
	6.3	•	27				
	6.4	Level Shifter Implementation Hints	27				
7	ΡΑΟ	CKAGING INFORMATION	28				



SX1504/SX1505/SX1506 4/8/16 Channel GPIO

WIRELESS & SENSING

	7.1	QFN-UT 20-pin Outline Drawing	28
	7.2	QFN-UT 20-pin Land Pattern	28
	7.3	QFN-UT 28-pin Outline Drawing	29
	7.4	QFN-UT 28-pin Land Pattern	29
8		SOLDERING PROFILE	



PIN DESCRIPTION 1

SX1504 4-channel GPIO 1.1

Pin	Symbol	Туре	Description		
1	NRESET	DIO	Active low reset		
2	SDA	DIO	I ² C serial data line		
3	NC1	-	Leave open, not connected		
4	SCL	DI	I ² C serial clock line		
5	I/O[0]	DIO (*1)	I/O[0], at power-on configured as an input		
6	I/O[1]	DIO (*1)	I/O[1], at power-on configured as an input		
7	VCC1	Р	I/O supply voltage		
8	GND	Р	Ground Pin		
9	I/O[2]	DIO ^(*1)	I/O[2], at power-on configured as an input High sink I/O.		
10	I/O[3]	DIO ^(*1)	I/O[3], at power-on configured as an input High sink I/O.		
11	NINT	DO	Active low interrupt output		
12	ADDR	DI	Address input, connect to VDDM or GND		
13	NC2	-	Leave open, not connected		
14	VDDM	Р	Main supply voltage		
15	NC3	-	Leave open, not connected		
16	NC4	-	Leave open, not connected		
17	NC7	-	Connect to VCC1		
18	GND	Р	Ground Pin		
19	NC5	-	Leave open, not connected		
20	NC6	-	Leave open, not connected		

A: Analog D: Digital I: Input O: Output

P: Power

(*1) This pin is programmable through the I²C interface

Table 1 – SX1504 Pin Description



Figure 1 - SX1504 QFN-UT-20 Pinout



SX1505 8-channel GPIO 1.2

WIRELESS & SENSING

Pin	Symbol	Туре	Description	
1	NRESET	DIO	Active low reset	
2	SDA	DIO	I ² C serial data line	
3	NC1	-	Leave open, not connected	
4	SCL	DI	I ² C serial clock line	
5	I/O[0]	DIO ^("1)	I/O[0], at power-on configured as an input	
6	I/O[1]	DIO ^(*1)	I/O[1], at power-on configured as an input	
7	VCC1	Р	Supply voltage for Bank A I/O[0-3]	
8	GND	Р	Ground Pin	
9	I/O[2]	DIO ^(*1)	I/O[2], at power-on configured as an input High sink I/O.	
10	I/O[3]	DIO ^(*1)	I/O[3], at power-on configured as an input High sink I/O.	
11	NINT	DO	Active low interrupt output	
12	ADDR	DI	Address input, connect to VDDM or GND	
13	NC2	-	Leave open, not connected	
14	VDDM	Р	Main supply voltage	
15	I/O[4]	DIO (*1)	I/O[4], at power-on configured as an input	
16	I/O[5]	DIO ^(*1)	I/O[5], at power-on configured as an input	
17	VCC2	Р	Supply voltage for Bank B I/O[4-7]	
18	GND	Р	Ground Pin	
19	I/O[6]	DIO ^(*1)	I/O[6], at power-on configured as an input	
20	I/O[7]	DIO ^(*1)	I/O[7], at power-on configured as an input	

A: Analog D: Digital I: Input O: Output P: Power

(*1) This pin is programmable through the I²C interface

Table 2 – SX1505 Pin Description



Figure 2 – SX1505 QFN-UT-20 Pinout



WIRELESS & SENSING SX1506 16-channel GPIO 1.3

Pin	Symbol	Туре	Description
1	GND	Р	Ground Pin
2	I/O[2]	DIO (*1)	I/O[2], at power-on configured as an input
3	I/O[3]	DIO ^(*1)	I/O[3], at power-on configured as an input
4	VCC1	Р	I/O supply voltage for Bank A I/O[0-7]
5	I/O[4]	DIO ^(~1)	I/O[4], at power-on configured as an input
6	I/O[5]	DIO ^(*1)	I/O[5], at power-on configured as an input
7	GND	Р	Ground Pin
8	I/O[6]	DIO ^(*1)	I/O[6], at power-on configured as an input High sink I/O.
9	I/O[7]	DIO ^(*1)	I/O[7], at power-on configured as an input High sink I/O.
10	NINT	DO	Active low interrupt output
11	NC	-	Leave open, not connected
12	VDDM	Р	Main supply voltage
13	I/O[8]	DIO ^(*1)	I/O[8], at power-on configured as an input
14	I/O[9]	DIO ^(*1)	I/O[9], at power-on configured as an input
15	GND	Р	Ground Pin
16	I/O[10]	DIO ^(~1)	I/O[10], at power-on configured as an input
17	I/O[11]	DIO ^(*1)	I/O[11], at power-on configured as an input
18	VCC2	Р	I/O supply voltage for Bank B I/O[8-15]
19	I/O[12]	DIO ^(*1)	I/O[12], at power-on configured as an input
20	I/O[13]	DIO ^(*1)	I/O[13], at power-on configured as an input
21	GND	Р	Ground Pin
22	I/O[14]	DIO ^(*1)	I/O[14], at power-on configured as an input High sink I/O.
23	I/O[15]	DIO ^(*1)	I/O[15], at power-on configured as an input High sink I/O.
24	NRESET	DIO	Active low reset
25	SDA	DIO	I ² C serial data line
26	SCL	DI	I ² C serial clock line
27	I/O[0]	DIO ^(*1)	I/O[0], at power-on configured as an input
28	I/O[1]	DIO ^(*1)	I/O[1], at power-on configured as an input

A: Analog D: Digital I: Input O: Output

P: Power

(*1) This pin is programmable through the I^2C interface



Figure 3 - SX1506 QFN-UT-28 Pinout



2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Stress above the limits listed in the following table may cause permanent failure. Exposure to absolute ratings for extended time periods may affect device reliability. The limiting values are in accordance with the Absolute Maximum Rating System (IEC 134). All voltages are referenced to ground (GND).

Symbol	Description	Min	Max	Unit
VDDM _{max}	Main supply voltage	- 0.4	6.0	V
VCC1,2 _{max}	I/O banks supply voltage	- 0.4	6.0	V
V _{ESD HBM}	Electrostatic handling HBM model ⁽¹⁾	-	1500	V
V _{ESD CDM}	Electrostatic handling CDM model	-	300	V
V _{ESD MM}	Electrostatic handling MM model	-	200	V
T _A	Operating Ambient Temperature Range	-40	+85	C
Tc	Junction Temperature Range	-40	+125	C
T _{STG}	Storage Temperature Range	-55	+150	C
l _{lat}	Latchup-free input pin current ⁽²⁾	+/-100	-	mA

(1) Tested according to JESD22-A114A

(2) Static latch-up values are valid at maximum temperature according to JEDEC 78 specification

Table 4 - Absolute Maximum Ratings

2.2 Electrical Specifications

Table below applies to default registers values, unless otherwise specified. Typical values are given for $T_A = +25$ °C, VDDM=VCC1=VCC2=3.3V.

Symbol	Description	Conditions	Min	Тур	Max	Unit
Supply	· · · · · · · · · · · · · · · · · · ·					
VDDM	Main supply voltage	-	2.5	-	5.5	V
VCC1,2	I/O banks supply voltage	-	2.5	-	5.5	V
IDDM	Main supply current (I ² C inactive)	-	-	1	5	μA
ICC1,2	I/O banks supply current ⁽¹⁾	-	-	1	2	μA
I/Os set a	as Input					
VIH	High level input voltage	-	0.7* VCC1,2	-	VCC1,2 +0.3	V
VIL	Low level input voltage	-	-0.4	-	0.3* VCC1,2	V
VHYS	Hysteresis of Schmitt trigger	-	-	0.1* VCC1,2	-	V
ILEAK	Input leakage current	Assuming no active pull-up/down	-1.5	-	1.5	μA
CI	Input capacitance	-	-	-	10	pF
I/Os set a	is Output					
VOH	High level output voltage	-	VCC1,2 - 0.3	-	VCC1,2	V
VOL	Low level output voltage	-	-0.4	-	0.3	V
IOH	High level output source current	-	-	-	8	mA
IOL	Low level output sink current for the high sink I/Os	-	-	-	24	mA
IOL	Low level output sink current for the other I/Os.	-	-	-	12	mA
t _{PV}	Output data valid timing	Cf. Figure 9	-	-	1.5	μs
NINT (Ou	tput)				•	
VOL	Low level output voltage	-	-	-	0.3	V
IOLM	Low level output sink current	-	-	-	12	mΑ
t _{IV}	Interrupt valid timing	From input data change	-	-	1	μs
t _{IR}	Interrupt reset timing	From RegInterruptSource clearing	-	-	2	μs



SymbolDescriptionConditionsMinTypMaxUnitVRESET (Input/Output)Unit0.3V0.3V0.3VIOL _M Low level output voltage12mAVH _{MR} High level input voltage-0.7*-12mAVH _{MR} Low level output sink current0.3*VVLMLow level input voltage0.4-VDDMVVLMLow level input voltage1.5µAVClInput capacitance10pFVPORPower-On-Reset voltageCl. Figure 7-0.9VVDROPLLow brown-out voltageCl. Figure 7-0.9VVDROPL Low brown-out voltageCl. Figure 77VIROPL Low brown-out voltageCl. Figure 77VHMALHigh level input voltage0.4-0.3*VHWRHugh level input voltage0.4-0.3*VHWSHugh level input voltage10pFVHMALHigh level input voltage0.4-0.3*VHKALLow level output voltage10pFSCLInput capacitance10pFVHMALHigh level input voltage	Cum k al	Description	Conditions	Mir	Turr	Mov	1 1
VOL Low level output voltage - - - 0.3 V IOL ₄ Low level output sink current - - 12 mA VH _{MR} High level input voltage - 0.7* - 12 mA VH _{MR} Low level output sink current - 0.4 - VDDM V VH _{MR} High level input voltage - 0.4 - VDDM V VHSw Hysteresis of Schmitt trigger - - 1.5 1.5 µA CI Input capacitance - - - 1.0 PF VDROP Nower-On-Reset voltage CI. Figure 7 - 0.2 V VDROPL Nower-On-Reset voltage CI. Figure 7 - 0.2 - V VILa Low level input voltage - 0.7* VDDM - 0.3* V VILa Low level input voltage - - 0.4 - 0.0* VDDM - </th <th></th> <th></th> <th>Conditions</th> <th>MIIN</th> <th>тур</th> <th>Max</th> <th>Unit</th>			Conditions	MIIN	тур	Max	Unit
$\begin{array}{c c c c c c c c c c c c c c c c c c c $						0.2	V
VIH _{MR} High level input voltage - 0.7'' VDDM - 5.5 V VIL _M Low level input voltage - -0.4 - 0.3'' VDM VHYS _M Hysteresis of Schmitt trigger - - 0.4 - VDM V VILA Input capacitance - - 1.5 µA CI Input capacitance - - 10 pV VDROP Low brown-out voltage CI. Figure 7 - 0.21 - V VDROPL High brown-out voltage CI. Figure 7 - 0.21 - V VDROPL Low brown-out voltage CI. Figure 7 - 0.21 - VDDM - VHROPL Low brown-out voltage - - 0.7'' VDDM + +0.3 V VILat Low brown-out voltage - - 0.4 + 0.3'' V VILat Low level input voltage - -			-	-	-		
VIFWR High level input voltage - VDDM - 5.5 V VILM Low level input voltage - -0.4 - 0.1* VDDM V VHYS Hysteresis of Schmitt trigger - - -0.4 - VDDM V VILAK Input leakage current - -1.5 - 1.5 µA CI Input capacitance - - 1.0 pF VDROPH High brown-out voltage Cf. Figure 7 - 0.2 - VDROPH High brown-out voltage Cf. Figure 7 - 0.2 - N VDROPH Low brown-out voltage Cf. Figure 7 - 0.2 - N VDROPH High level input voltage - - 0.7* NDDM - NDDM VH_Max High level input voltage - - 0.4 - 0.3* V VH_Max High level input voltage - - 1.5 µ		Low level output sink current	-	-	-	IZ	ΠA
VILM Low level input voltage - -0.4 - VDDM V VHYSM Hysteresis of Schmitt trigger - - 0.1* VDDM - V ILLEAK Input leakage current - -1.5 - 1.5 µA CI Input capacitance - - 10 pF VDROPH High brown-out voltage Cf. Figure 7 - 0.2 - V VDROPH Ihigh brown-out voltage Cf. Figure 7 - 0.2 - V VDROPH Ihigh brown-out voltage Cf. Figure 7 - 0.2 - V VBROPH High brown-out voltage Cf. Figure 7 - 0.2 - V VIH _{MA} High level input voltage - - 0.3* V VDDM - 0.3* V VIH _{MA} High level input voltage - - 0.4 - 0.3* V VHSM Hysteresis of Schmitt trigger -	VIH _{MR}	High level input voltage	-	-	-		V
VHTYS Hysteresis or Schmitt frigger - - - VDDM - V ILEAK Input leakage current - - 1.5 J pF VDROPH Input capacitance - - 1.0 pF VDROPH Low brown-out voltage Cf. Figure 7 - 0.9 V VDROPH Low brown-out voltage Cf. Figure 7 - 0.2 - V VDROPH Low brown-out voltage Cf. Figure 7 - - 7 ms tresset Reset time Cf. Figure 7 - - 7 ms VHM _{MA} High level input voltage - 0.7* VDDM V VDDM V VHM _{MA} Low level input voltage - - 0.1* VDM V VDDM V VDDM V VDDM V VDDM V VDDM V VDDM V VIL _M Low level output voltage - - 0.1* VDDM<	VIL _M	Low level input voltage	-	-0.4	-		V
CI Input capacitance - 1 10 pF VPOR Power-On-Reset voltage Cf. Figure 7 0.7 - 0.9 V VDROPH High brown-out voltage Cf. Figure 7 - VDDN-1 V VEROPH High brown-out voltage Cf. Figure 7 - 0.2 - V VEROPH High brown-out voltage Cf. Figure 7 - - 7 ms trause Reset time Cf. Figure 7 - - 7 ms VH _{MA} High level input voltage - - 0.7* VDDM V VH _{MA} Low level input voltage - - 0.4* - 0.3* V VH _{MA} Hysteresis of Schmitt trigger - - - 1.0 pF Cl Input capacitance - - 1.0 pF ScL (nput capacitance) - - 1.0 pF ScL (nput capacitance) -<			-	-		-	V
VPCR Power-On-Reset voltage Cf. Figure 7 0.7 - 0.9 V VDROPH High brown-out voltage Cf. Figure 7 - VDDM1 - V VDROPL Low brown-out voltage Cf. Figure 7 - 0.2 - V VBROPL Low brown-out voltage Cf. Figure 7 - - 7 ms VIMA High level input voltage Cf. Figure 7 - - 7 ms VIH _{MA} High level input voltage - 0.7' - VDDM +0.3 V VIL _{MA} Low level input voltage - - 0.1'' - VDDM +0.3 V VHYSM Hysteresis of Schmitt trigger - - - 0.1'' V VDDM - VDDM +0.3 V SCL Input capacitance - - 1.0 p F SC - 1.0 p SC SCL Input adapcitance -			-	-1.5	-		
VDROPH High brown-out voltage Cf. Figure 7 - VDDM-1 - V VDROPL Low brown-out voltage Cf. Figure 7 - 0.2 - V Vesser Reset time Cf. Figure 7 - 0.2 - V Vulese Reset time Cf. Figure 7 - - 7 ms ADDR (input) - - 0.7" - 0.4 - 0.3" V VIH _{MA} High level input voltage - - - 0.4 - 0.3" V VHYS _M Hysteresis of Schmitt trigger - - - 0.1" V VDDM - VDDM - VDDM - VDDM - 1.5 µA - 1.5 µA - 1.0 pF SCI (input) and SDA (input/Output) (40 - - - 1.0 pF Sci (input/Output) (40 - - - 1.0 pF Sci (input/Output) (40 - - </td <td></td> <td></td> <td>-</td> <td>-</td> <td>-</td> <td></td> <td></td>			-	-	-		
VDROPL Low brown-out voltage Cf. Figure 7 - 0.2 - V typuse Reset time Cf. Figure 7 - - 7 ms ADDR (Input) VILMM High level input voltage - - 7 ms VILMM Low level input voltage - - 0.7" VDDM - 0.3" V VILM Low level input voltage - - 0.4 - 0.3" V VHYSM Hysteresis of Schmitt trigger - - - 1.5 µA Cl Input leakage current - - - 1.5 µA Cl Input dapaditance - - - 10 pF SCL (Input) and SDA (Input/Output) f0 Therace as described by Philips I'C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I'C specifications. VOL Low level output voltage - - 0.3 V VILM Low level output voltage - - 0.3 V VILM Low level input voltage - <td>VPOR</td> <td>Power-On-Reset voltage</td> <td>Cf. Figure 7</td> <td>0.7</td> <td>-</td> <td>0.9</td> <td></td>	VPOR	Power-On-Reset voltage	Cf. Figure 7	0.7	-	0.9	
Itesser Reset time Cf. Figure 7 - 7 ms teuser Reset pulse from host uC Cf. Figure 7 300 - - ns ADDR (input) - 0.7* VDDM - - ns VIH _{MA} High level input voltage - - 0.7* VDDM +0.3 V VIH _{MA} High level input voltage - - 0.4 - 0.3* V VHYS _M Hysteresis of Schmitt trigger - - 0.4 - 0.3* V ULEAK Input teakage current - - 1.5 µ A CI Input teakage current - - 10 pF SCL (input) and SDA (input/Output) rd - 10 pF ScL Input teakage current - - 0.3 V VOL Low level output voltage - - 0.3 V VOL Low level output voltage -	VDROPH	High brown-out voltage	Cf. Figure 7	-	VDDM-1	-	
toulse Reset pulse from host uC Cf. Figure 7 300 - - ns ADDR (Input) - - 0.7* VDDM - - ns VIH_M High level input voltage - - 0.7* VDDM - +0.3 V VIL_M Low level input voltage - - - 0.4 - 0.3* V VHYS_M Hysteresis of Schmitt trigger - - - 0.1* - VDDM - V ILEAK Input capacitance - - - 10 pF SCL (input) and SDA (input/Output) ⁽⁴⁾ - - - 10 pF SCL (input) and SDA (input/Output) ⁽⁴⁾ - - - 0.3 V VOL Low level output voltage - - - 0.3 V VDL Low level input voltage - - - 12 mA VIH_MR High level input voltage	VDROPL	Low brown-out voltage	Cf. Figure 7	-	0.2	-	V
tpuse Reset pulse from host uC Cf. Figure 7 300 - - ns ADDR (Input) - - 0.7* VDDM - - ns VIH _{MA} High level input voltage - - 0.4 - 0.3* V VIL _{MA} Low level input voltage - - - 0.4 - 0.7* VDDM V VHYS _{MA} Hysteresis of Schmitt trigger - - - 0.1* V V VILEAK Input capacitance - - 1.5 - 1.5 - 1.5 µ V CI Input capacitance - - 10 pF SCL (input) - 10 pF SCL (input) - - 10 pF - - -	t _{RESET}	Reset time	Cf. Figure 7	-	-	7	ms
ADDR (Input) ····································				300	-	-	ns
VIH _{MA} High level input voltage - 0.7* VDDM · 0.3* V VIL _M Low level input voltage - 0.4 - 0.3* V VHYSM Hysteresis of Schmitt trigger - - 0.4 - 0.3* V VHYSM Hysteresis of Schmitt trigger - - - 0.0* VDDM - V ILEAK Input leakage current - - - 10 pF SCL (Input) and SDA (Input/Output) ¹⁰⁹ - - - 10 pF SCL Jule Call allave F/S mode 1/C interface as described by Philips 1/C specifications. - - 10 SCL Jule Call allave F/S mode 1/C interface as described by Philips 1/C specifications. - - 0.3 V VOL Low level output voltage - - 0.3 V - VOL Low level output sink current - - 12 mA VIL _{MR} High level input voltage -	ADDR (In						
VIHMA High level input voltage - VDDM - +0.3 V VILM Low level input voltage - -0.4 - 0.3" V VHYSM Hysteresis of Schmitt trigger - -0.4 - 0.1" VDDM V ILEAK Input leakage current - - 1.5 µA CI Input capacitance - - 10 pF SCL (input) and SDA (input/output) Ci - - 10 pF SCL (input, 2000. Please refer to that document for more detailed 1°C specifications. - - 0.3 V VOL Low level output voltage - - 0.3 V VOL Low level output voltage - - 0.3 V VOL Low level output voltage - - 0.3 V VILM Low level output voltage - - 12 mA VILM Low level output voltage - - 12 mA VILM Low level input voltage - - 0.3"				0.7*		VDDM	
VIL _M Low level input voltage - -0.4 - 0.3* VDDM V VHYS _M Hysteresis of Schmitt trigger - - 0.1* VDDM V V ILEAK Input leakage current - -1.5 - 1.5 µA CI Input capacitance - - 1.0 pF SCL (Input) and SDA (Input/Output) ''' - 1.0 pF SCL (Input) and SDA (Input/Output) ''' - 1.0 pF SCL (Input) and SDA (Input/Output) ''' - - 1.0 pF SCL (Input) and SDA (Input/Output) ''' - - 0.7 C Sci VOL Low level output solate F/S mode 12C interface as described by Philips 12C specification. - - - 0.3 V VOL Low level output voltage - - 0.3 V VIL _M Low level output voltage - - 0.3 V VIL _M Low level input voltage -		High level input voltage	-		-		V
VILM Low level input voltage - -0.4 - VDM V VHYSM Hysteresis of Schmitt trigger - - 0.1* - V ILEAK Input capacitance - - 1.5 - 1.5 µA CI Input capacitance - - 10 pF SCL (input) and SDA (input/Output) ⁽²⁾ Interface complies with slave F/S mode I'C interface as described by Philips I'C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I'C specifications. SOL VOL Low level output voltage - - O. VILM VILM Low							
VHYSM Hysteresis of Schmitt frigger - - VDDM - V ILLAK Input leakage current - -1.5 - 1.5 µA CI Input capacitance - - 10 pF SCL (Input) and SDA (Input/Output) ⁽²⁾ Interface complies with slave F/S mode I'C interface as described by Philips I'C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I'C specifications. - 0.1 - 10 pF ScL	VIL _M	Low level input voltage	-	-0.4	-		V
Cl Input capacitance - - 10 pF SCL (Input) and SDA (Input/Output) ⁽²⁾ - - 10 pF Interface complies with slave F/S mode I/C interface as described by Philips I/C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I/C specifications. - - 10 pF SDA Implementation of the second sec			-	-		-	V
SCL (input) and SDA (input/Output) Interface complies with slave F/S mode l ² C interface as described by Philips l ² C specification version 2.1 dated January, 2000. Please refer to that document for more detailed l ² C specifications. SDA Image: specification version 2.1 dated January, 2000. Please refer to that document for more detailed l ² C specifications. SDA Image: specification version 2.1 vit Image: specification version 2.1 VOL Low level output since version 2.1 VOL Low level output voltage VOL Low level output sink current IOL _M Low level input voltage VIH _{MR} High level input voltage VIL _M Low level input voltage VIL _M Low level of the SCL clock VIL _M Low level of the SCL clock thod time (repeated) START 0.6 condition 0.6 t _{LOW} LOW period of the SCL clock t _{LOW} Data set-up time t _{LOW} Targe repeated t _{LOW} Targe repeated t _{LOW} Targe repeated t _{LOW} Low level of the SCL clock t _{LOW} Low period of the SCL clock <td>ILEAK</td> <td>Input leakage current</td> <td>-</td> <td>-1.5</td> <td>-</td> <td>1.5</td> <td>μA</td>	ILEAK	Input leakage current	-	-1.5	-	1.5	μA
SCL (input) and SDA (input/Output) ^{1/2} Interface complies with slave F/S mode l ² C interface as described by Philips l ² C specification version 2.1 dated January, 2000. Please refer to that document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. SDA Implement to the document for more detailed l ² C specifications. Volt to the velop of the document for more detailed l ² C specifications. VOL Low level output voltage - - VOL Low level output voltage - - VIL _M Low level output voltage - - VIL _M Low level	CI	Input capacitance	-	-	-	10	pF
Interface complies with slave F/S mode I ² C interface as described by Philips I ² C specification version 2.1 dated January, 2000. Please refer to that document for more detailed I ² C specifications.	SCL (Inpu	ut) and SDA (Input/Output) ⁽²⁾					
dated January, 2000. Please refer to that document for more detailed I ² C specifications. SDA t t t t t t t t t t t t t	Interface	complies with slave F/S mode	I ² C interface as described by	Philips I ² C	specificati	on version	2.1
VOLLow level output voltage0.3VVOLLow level output voltage0.3VVILMLow level output voltage12mAVIHMRHigh level input voltage0.3*VVILMLow level output voltage12mAVIHMRHigh level input voltage0.7*VDDMVILMLow level output voltage0.40.3*VILMLow level input voltage0.6-thip:staHigh level input voltage-0.6-µsthup:staScL clock frequency-0.6-µsthup:staSet-up time for a repeated-0.6-µsthup:taSet-up time for a repeated-0.6-µsthup:taData hold time-0(3)-0.9(4)thup:taData set-up time-100(5)trRise time of both SDA and SCL signals-20+0.1Cb(6)-300nstFall time of both SDA and SCL signals-20+0.1Cb(6)-300nstureSet-up time for STOP-0.6100	dated Jan	uary, 2000. Please refer to that o	document for more detailed I ² C	specificatio	ons.		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							-
$\begin{array}{c c c c c c c c c c c c c c c c c c c $						L!	-
M_{MR} High level input voltage- 0.7^* VDDM- 5.5 VVIL _M Low level input voltage0.4- 0.3^* VDDMV f_{SCL} SCL clock frequency-0-400kHz $t_{HD;STA}$ Hold time (repeated) START condition-0.6 μs t_{LOW} LOW period of the SCL clock-1.3 μs t_{LOW} LOW period of the SCL clock-0.6 μs $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 μs t_{HIGH} HIGH period of the SCL clock-0.6 μs $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 μs $t_{HD;DAT}$ Data hold time-0.6 μs $t_{HD;DAT}$ Data set-up time-100 ⁽⁵⁾ t_r Rise time of both SDA and SCL signals-20+0.1C _b ⁽⁶⁾ -300ns t_f Fall time of both SDA and SCL signals-20+0.1C _b ⁽⁶⁾ -300ns			-	-	-		
VIHMRHigh level input voltage-VDDM-5.5VVILMLow level input voltage0.4- 0.3^* VDDMV f_{SCL} SCL clock frequency-0-400kHz $t_{HD;STA}$ Hold time (repeated) START condition-0.6 μs t_{LOW} LOW period of the SCL clock-1.3 μs t_{HIGH} HIGH period of the SCL clock-0.6 μs $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 μs $t_{HD;DAT}$ Data hold time-0.6 μs t_r Rise time of both SDA and SCL signals-20+0.1C_b^{(6)}-300ns t_f Fall time of both SDA and SCL signals-20+0.1C_b^{(6)}-300ns	IOLM	Low level output sink current	-	-	-	12	mΑ
VILMLow level input voltage0.4-VDDMV f_{SCL} SCL clock frequency-0-400kHz $t_{HD;STA}$ Hold time (repeated) START condition0.6 μ_S t_{LOW} LOW period of the SCL clock-1.3 μ_S t_{HGH} HIGH period of the SCL clock-0.6 μ_S t_{HIGH} HIGH period of the SCL clock-0.6 μ_S t_{HIGH} Set-up time for a repeated START condition-0.6 μ_S $t_{SU;STA}$ Set-up time for a repeated START condition-0.6 μ_S $t_{HD;DAT}$ Data hold time-0.6 μ_S $t_{HD;DAT}$ Data set-up time-100 ⁽⁵⁾ t_r Rise time of both SDA and SCL signals-20+0.1C_b^{(6)}-300ns t_r Set-up time for STOP-0.6400 μ_S	VIH _{MR}	High level input voltage	-		-		V
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	VIL_M	Low level input voltage	-	-0.4	-		V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	f _{SCL}		-	0	-	400	kHz
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	t _{HD;STA}		-	0.6	-	-	μs
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	ti ow		_	1.3	-	-	μs
$t_{SU;STA}$ Set-up time for a repeated START condition- 0.6 - μs $t_{HD:DAT}$ Data hold time- 0.6 - μs $t_{HD:DAT}$ Data set-up time- $100^{(3)}$ - $0.9^{(4)}$ μs t_{r} Rise time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_{f} Fall time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_{f} Set-up time for STOP- 0.6 - 0.6 - 0.6			-		-	-	
$t_{HD:DAT}$ Data hold time- $0^{(3)}$ - $0.9^{(4)}$ μs $t_{SU:DAT}$ Data set-up time- $100^{(5)}$ t_r Rise time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_f Fall time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_f Set-up time for STOP- 0.6 - 0.6 - 0.6		Set-up time for a repeated	-		-	-	
$t_{SU;DAT}$ Data set-up time- $100^{(5)}$ t_r Rise time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_f Fall time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 ns t_f Set-up time for STOP- 0.6 - 0.6 - 0.6			_	0 ⁽³⁾	-	0 Q ⁽⁴⁾	110
trRise time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 nstrFall time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 nstrSet-up time for STOP- 0.6 - 0.6 - 0.6				•	_	0.0	μο
t_r SCL signals-20+0.1C_b-300Ns t_f Fall time of both SDA and SCL signals- $20+0.1C_b^{(6)}$ - 300 nstargetSet-up time for STOP- 0.6 - 0.6 - 0.6	SU;DAT		-		-	-	+
t _f SCL signals - 20+0.1Cb ^o - 300 ns turned Set-up time for STOP 0.6 - us	t _r	SCL signals	-	20+0.1C _b ⁽⁶⁾	-	300	ns
	t _f	SCL signals	-	20+0.1C _b ⁽⁶⁾	-	300	ns
	t _{su;sto}		-	0.6	-	-	μs



Symbol	Description	Conditions	Min	Тур	Max	Unit
t _{BUF}	Bus free time between a STOP and START condition	-	1.3	-	-	μs
C _b	Capacitive load for each bus line	-	-	-	400	pF
V _{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	-	0.1*VDDM	-	-	V
V _{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	-	0.2*VDDM	-	-	V
Miscellar	neous					
RPULL	Programmable pull-up/down resistors for IO[0-7]	-	-	60	-	kΩ
t _{PLD}	PLD propagation delay	VCC1,2 & VDDM = 5V	-	-	25	ns

(1) Assuming no load connected to outputs and inputs fixed to VCC1,2 or GND.

(2) All values referred to VIH_{MR min} and VIL_{M max} levels.

(3) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to VIH_{MR min}) to bridge the undefined region of the falling edge of SCL.

(4) The maximum t_{HD:DAT} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(5) A Fast-mode l^2 C-bus device can be used in a Standard-mode l^2 C-bus system, but the requirement $t_{SU;DAT} \ge 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal.

If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r max}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released.

(6) C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall-times are allowed.

Table 5 – Electrical Specifications



3 TYPICAL OPERATING CHARACTERISTICS

Figures below apply to default registers values, Tamb, unless otherwise specified.

3.1 IDDM vs. VDDM



3.2 VOL vs. IOL





3.3 VOH vs. IOH





4 **BLOCK DETAILED DESCRIPTION**

SX1504 4-channel GPIO



Figure 4 – SX1504 Block Diagram





4.1



4.3 SX1506 16-channel GPIO



Figure 6 – SX1506 Block Diagram

4.4 Reset (NRESET)

The SX1504, SX1505 and SX1506 generate their own power on reset signal after a power supply is connected to the VDDM pin. The reset signal is made available for the user at the pin NRESET. The rising edge of the NRESET indicates that the startup sequence of the SX1504, SX1505 or SX1506 has finished. NRESET must be connected to VDDM (or greater) either directly, or via a resistor.



Figure 7 – Power-On / Brown-out Reset Conditions

- 1. Device behavior is undefined until VDDM rises above VPOR, at which point NRESET is driven to GND by the SX1504, SX1505 or SX1506.
- 2. After t_{RESET}, NRESET is released (high-impedance) by the SX1504, SX1505 or SX1506 to allow it to be pulled high by an external resistor.
- 3. In operation, the SX1504, SX1505 and SX1506 may be reset at anytime by an external device driving NRESET low during t_{PULSE}. Chip can be accessed normally again after NRESET rising edge.



- 4. During a brown-out event, if VDDM drops above VDROPH a reset will not occur.
- 5. During a brown-out event, if VDDM drops between VDROPH and VDROPL a reset may occur.
- 6. During a brown-out event, if VDDM drops below VDROPL a reset will occur next time VPOR is crossed.

Please note that a brown-out event is defined as a transient event on VDDM. If VDDM is attached to a battery, then the gradual decay of the battery voltage will not be interpreted as a brown-out event. Please also note that a sharp rise in VDDM (> 1V/us) may induce a circuit reset.

4.5 2-Wire Interface (I²C)

The SX1504, SX1505 and SX1506 2-wire interface (I²C compliant) operates only in slave mode. In this configuration, the device has one or two device addresses defined by ADDR pin.

Device	ADDR Pin	I ² C Address	Description
SX1504 & 0		0x2 0 (010000 0)	First address of the 2-wire interface
SX1505	1	0x21 (0100001)	Second address of the 2-wire interface
SX1506		0x20 (0100000)	Fixed address of the 2-wire interface
	1	- (/	Fixed address of the 2-wire interfac

Table 6 - 2-Wire Interface Address

2 lines are used to exchange data between an external master host and the slave device:

- SCL : Serial CLock
- SDA : Serial DAta

The SX1504, SX1505 and SX1506 are read-write slave-mode I^2C devices and comply with the Philips I^2C standard Version 2.1 dated January, 2000. The SX1504, SX1505 and SX1506 have respectively 12, 16, and 31 user-accessible internal 8-bit registers. The I^2C interface has been designed for program flexibility, in that once the slave address has been sent to the SX1504, SX1505 or SX1506 enabling it to be a slave transmitter/receiver, any register can be written or read independently of each other. While there is no auto increment/decrement capability in the SX1504 and SX1505 I^2C logic, a tight software loop can be designed to access the next register independent of which register you begin accessing. SX1506 implements auto increment capability. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

Seven bit addressing is used and ten bit addressing is not allowed. Any general call address will be ignored by the SX1504, SX1505 and SX1506. The SX1504, SX1505 and SX1506 are not CBUS compatible and can operate in standard mode (100kbit/s) or fast mode (400kbit/s).

<u>4.5.1</u> WRITE

The simplest format for an I^2C write is given below. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The I^2C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].



Master operations

SX1504, SX1505 or SX1506 operations (Slave)

S: Start Condition

W: Write = '0' A: Acknowledge (sent by slave)

P: Stop condition

Slave Address: 7 bit Register Address: 8 bit Data: 8 bit

Figure 8 - 2-Wire Serial Interface, Write Register Operation





Figure 9 - Write RegData Register

Please note that SX1506 implements register address auto-increment i.e. after the Data ACK from Slave the master can write further bytes and the interface will handle the register address increment automatically. Finally the master terminates the transfer normally the stop condition [P].

4.5.2 READ

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The l^2C then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8 bit data byte; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

S Slave Address	WA	Register Address	A Sr	Slave Address	RA	Data	NACK P		
Master operations									
SX1504, SX1505 o	r SX1506	operations (Slave)							
S: Start Condition Slave Address: 7 bit W: Write = '0' Register Address: 8 bit R: Read = '1' Data: 8 bit A: Acknowledge (sent by slave) NACK: Non-Acknowledge (sent by master) Sr: Repeated Start Condition P: Stop condition Figure 10 - 2-Wire Serial Interface, Read Register Operation									
Please note that SX1506 implements register address auto-increment i.e. after the Data byte from Slave the master can acknowledge (ACK) to indicate that it wants to read the next byte and the interface will handle the register address increment automatically. Finally the master terminates the transfer normally with a NACK									

4.5.3 READ - STOP separated format (SX1504 and SX1505 only)

When operating SX1504 or SX1505, stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The slave then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a Stop or Restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the slave with a read command. The slave acknowledges this request and returns the data from the register location that had previously been set up.

followed by the stop condition [P].





Sr: Repeated Start Condition

P: Stop condition

Figure 11 - 2-Wire Serial Interface, Read – Stop Separated Mode Operation

4.6 Interrupt (NINT)

At start-up, the transition detection logic is reset, and NINT is released to a high-impedance state. The interrupt mask register is set to 0xFF, disabling the interrupt output for transitions on all I/O ports. The transition flags are cleared to indicate no data changes.

An interrupt NINT can be generated on any programmed combination of I/Os rising and/or falling edges through the RegInterruptMask and RegSense registers.

If needed, the I/Os which triggered the interrupt can then be identified by reading RegInterruptSource register.

When NINT is low (i.e. interrupt occurred), it can be reset back high (i.e. cleared) by writing 0xFF in RegInterruptSource (this will also clear corresponding bits in RegEventStatus register). SX1506 also allows the interrupt to be cleared automatically when reading RegData register (Cf. RegAdvanced)

Every level went to detect vising edge of 1/0[4] on SV4505 (NINT will go leve)

Example: We want to detect rising edge of I/O[1] on SX1505 (NINT will go low). 1. We enable interrupt on I/O[1] in RegInterruptMask

- \Rightarrow RegInterruptMask ="XXXXXX**0**X"
- 2. We set edge sense for I/O[1] in RegSense
- ⇒ RegSenseLow ="XXXX01XX"

4.7 **Programmable Logic Functions (PLD)**

The SX1504, SX1505 and SX1506 offer a unique fully programmable logic functions like a PLD to give more flexibility and reduce external logic gates used for standard applications.

Since the whole truth table is fully programmable, the SX1504, SX1505, and SX1506 can implement combinatory functions ranging from the basic AND/OR gates to the most complicated ones with up to four 3-to1 PLDs or two 3-to-2 PLDs which can also be externally cascaded if needed.

In all cases, any IO not configured for PLD functionality retains its GPIO functionality while I/Os used by the PLD have their direction automatically set accordingly.

Please note that while RegDir corresponding bits are ignored for PLD operation they may still be set to input to access unused PLD inputs as normal GPI (PLD truth table can define some inputs to have no effect on PLD output) and/or generate interrupt based on any of the PLD inputs or outputs bits.

<u>4.7.1</u> SX1504

The SX1504 I/Os can be configured to provide any combinational 2-to-1 logic function using I/O[0-2] whilst retaining GPIO capability on I/O[3] OR provide a combinational 3-to-1 decode function using all 4 I/O ports.

RegPLDMode	SX1504 I/Os								
1:0	3	2	1	0					
00	GPIO	GPIO	GPIO	GPIO					
01	GPIO	PLD OUT	PLD IN	PLD IN					
10	PLD OUT	PLD IN	PLD IN	PLD IN					

Table 7 – SX1504 PLD Modes Settings



<u>4.7.2</u> SX1505

The SX1505 I/Os can be configured as per the SX1504, and can additionally be configured to provide a 2-to-1 logic function on I/O[4-6], 3-to-1 logic function on I/O[4-7], or 3-to-2 logic decode on I/O[0-4].

RegPL	DMode	SX1505 I/Os								
5:4	1:0	7	6	5	4	3	2	1	0	
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN	
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	

Table 8 – SX1505 PLD Modes Settings

4.7.3 SX1506

Each of the two I/O banks of the SX1506 I/Os can be configured as per the SX1505.

RegPLD	ModeB	SX1506 I/Os								
5:4	1:0	15	14	13	12	11	10	9	8	
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN	
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	

Table 9 – SX1506 PLD Modes Settings (Bank B)

RegPLD	OModeA	SX1506 I/Os								
5:4	1:0	7	6	5	4	3	2	1	0	
00	00	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	
00	01	GPIO	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	
00	10	GPIO	GPIO	GPIO	GPIO	PLD OUT	PLD IN	PLD IN	PLD IN	
00	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
01	00	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
01	01	GPIO	PLD OUT	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
01	10	GPIO	PLD OUT	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
01	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	
10	00	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	GPIO	GPIO	GPIO	
10	01	PLD OUT	PLD IN	PLD IN	PLD IN	GPIO	PLD OUT	PLD IN	PLD IN	
10	10	PLD OUT	PLD IN	PLD IN	PLD IN	PLD OUT	PLD IN	PLD IN	PLD IN	
10	11	GPIO	GPIO	GPIO	PLD OUT	PLD OUT	PLD IN	PLD IN	PLD IN	

Table 10 – SX1506 PLD Modes Settings (Bank B)



4.7.4 Tutorial

The generic method described in this paragraph can be applied to any of the SX1504, SX1505 or SX1506. *Example: We want to implement an AND gate between I/O[0] and IO[1] on SX1505*

- 1. Identify in the tables above the RegPLDMode setting to be programmed.
- What we need corresponds to the second line of the SX1505 PLD Table => RegPLDMode = "xx00xx01" 2. Fill corresponding RegPLDTableX with the wanted truth table.
- As mentioned in RegPLDMode description, using PLD 2-to-1 mode on I/0[0-2] implies to fill the truth table located in RegPLDTable0(3:0)

I/O[1]	I/O[0]	I/O[2]
0	0	(0)
0	1	0
1	0	0
1	1	1/

=> RegPLDTable0 = "xxxx**1000**"



5 CONFIGURATION REGISTERS

5.1 SX1504 4-channel GPIO

Address	Name	Description	Default
0x00	RegData	Data register	1111 1111
0x01	RegDir	Direction register	1111 1111
0x02	RegPullUp	Pull-up register	0000 0000
0x03	RegPullDown	Pull-down register	0000 0000
0x04	Reserved	Unused	XXXX XXXX
0x05	RegInterruptMask	Interrupt mask register	1111 1111
0x06	RegSenseHigh	Unused	XXXX XXXX
0x07	RegSenseLow	Sense register	0000 0000
0x08	RegInterruptSource	Interrupt source register	0000 0000
0x09	RegEventStatus	Event status register	0000 0000
0x10	RegPLDMode	PLD mode register	0000 0000
0x11	RegPLDTable0	PLD truth table 0	0000 0000
0x12	RegPLDTable1	Unused	XXXX XXXX
0x13	RegPLDTable2	PLD truth table 2	0000 0000
0x14	RegPLDTable3	Unused	XXXX XXXX
0x15	RegPLDTable4	Unused	XXXX XXXX

Table 11 – SX1504 Configuration Registers Overview

Addr	Name	Default	Bits	Description			
			7:4	Reserved. Must be set to 1 (default value)			
0x00	RegData	0xFF	3:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.			
			7:4	Reserved. Must be set to 1 (default value)			
0x01	RegDir	0xFF	3:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input			
			7:4	Reserved. Must be set to 0 (default value)			
0x02	RegPullUp	0x00	3:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled			
			7:4	Reserved. Must be set to 0 (default value)			
0x03	RegPullDown	0x00	3:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled			
0x04	Reserved	0xXX	7:0	Unused			
			7:4	Reserved. Must be set to 1 (default value)			
0x05	RegInterruptMask	0xFF	3:0	Configures which [input-configured] IO will trigger an ir 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	terrupt on NINT pin		
0x06	RegSenseHigh	0xXX	7:0	Unused			
			7:6	Edge sensitivity of I/O[3]	00 : None		
0x07	RegSenseLow	0x00	5:4	Edge sensitivity of I/O[2]	01 : Rising		
0,01	Regornselow	0,000	3:2	Edge sensitivity of I/O[1]	10 : Falling		
			1:0	Edge sensitivity of I/O[0]	11 : Both		
			7:4	Reserved. Must be set to 0 (default value)			
0x08	RegInterruptSource	0x00	3:0	Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured).			
				Writing '1' clears the bit in RegInterruptSource and in RegEventStatus. When all bits are cleared, NINT signal goes back high.			
0x09		0x00	7:4	Reserved. Must be set to 0 (default value)			



Addr	Name	Default	Bits	Description	
	RegEventStatus		3:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as config register occured). Writing '1' clears the bit in RegEventStatus and in RegI If the edge sensitivity of the IO is changed, the bit(s) wi	nterruptSource if relevant.
			7:2	Reserved. Must be set to 0 (default value)	· · · · ·
0x10	RegPLDMode	0x00	1:0	PLDMode 00 : PLD disabled – Normal GPIO mode for I/O[3:0] 01 : PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] as 10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as 11 : Not used	s defined in RegPLDTable0 s defined in RegPLDTable2
			7:4	Reserved. Must be set to 0 (default value)	
			3	Value to be output on I/O[2] when I/O[1:0] = 11	
0x11	RegPLDTable0	0x00	2	Value to be output on I/O[2] when I/O[1:0] = 10	Applies only when PLDMode is
			1	Value to be output on I/O[2] when I/O[1:0] = 01	set to PLD 2-to-1 mode
			0	Value to be output on I/O[2] when I/O[1:0] = 00	
0x12	RegPLDTable1	0xXX	7:0	Unused	
			7	Value to be output on I/O[3] when I/O[2:0] = 111	
			6	Value to be output on I/O[3] when I/O[2:0] = 110	_
			5	Value to be output on I/O[3] when I/O[2:0] = 101	_
0x13	RegPLDTable2	0x00	4	Value to be output on $I/O[3]$ when $I/O[2:0] = 100$	Applies only when PLDMode is
	U U		3	Value to be output on I/O[3] when I/O[2:0] = 011	set to PLD 3-to-1 mode
			2	Value to be output on $I/O[3]$ when $I/O[2:0] = 010$	-
			1	Value to be output on $I/O[3]$ when $I/O[2:0] = 001$	4
			0	Value to be output on I/O[3] when I/O[2:0] = 000	
0x14	RegPLDTable3	0xXX	7:0	Unused	
0x15	RegPLDTable4	0xXX	7:0	Unused	

Table 12 – SX1504 Configuration Registers Description

5.2 SX1505 8-channel GPIO

Address	Name	Description	Default
0x00	RegData	Data register	1111 1111
0x01	RegDir	Direction register	1111 1111
0x02	RegPullUp	Pull-up register	0000 0000
0x03	RegPullDown	Pull-down register	0000 0000
0x04	Reserved	Unused	XXXX XXXX
0x05	RegInterruptMask	Interrupt mask register	1111 1111
0x06	RegSenseHigh	Sense register for I/O[7:4]	0000 0000
0x07	RegSenseLow	Sense register for I/O[3:0]	0000 0000
0x08	RegInterruptSource	Interrupt source register	0000 0000
0x09	RegEventStatus	Event status register	0000 0000
0x10	RegPLDMode	PLD mode register	0000 0000
0x11	RegPLDTable0	PLD truth table 0	0000 0000
0x12	RegPLDTable1	PLD truth table 1	0000 0000
0x13	RegPLDTable2	PLD truth table 2	0000 0000
0x14	RegPLDTable3	PLD truth table 3	0000 0000
0x15	RegPLDTable4	PLD truth table 4	0000 0000

Table 13 – SX1505 Configuration Registers Overview

Addr	Name	Default	Bits	Description
0x00	RegData	0xFF 7:0 Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.		
0x01	RegDir	0xFF	Configures direction for each IO. 7:0 0 : IO is configured as an output 1 : IO is configured as an input	
0x02	RegPullUp	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled
0x03	RegPullDown	0x00	7:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled



Addr	Name	Default	Bits	Description		
0x04	Reserved	0xXX	7:0	Unused		
0.05	DealateausatMeels		7.0	Configures which [input-configured] IO will trigger an in	terrupt on NINT pin	
0x05	RegInterruptMask	0xFF	7:0	0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt		
			7:6	Edge sensitivity of I/O[7]	00 : None	
			5:4	Edge sensitivity of I/O[6]	01 : Rising	
0x06	RegSenseHigh	0x00	3:2	Edge sensitivity of I/O[5]	10 : Falling	
			1:0	Edge sensitivity of I/O[4]	11 : Both	
			7:6	Edge sensitivity of I/O[3]	00 : None	
0x07	RegSenseLow	0x00	5:4	Edge sensitivity of I/O[2]	01 : Rising	
0,01	Regornacion	0,00	3:2	Edge sensitivity of I/O[1]	10 : Falling 11 : Both	
			1:0	Edge sensitivity of I/O[0]		
0x08	RegInterruptSource	0x00	7:0	Interrupt source (from IOs set in RegInterruptMask) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event RegSense register occured). Writing '1' clears the bit in RegInterruptSource and in F When all bits are cleared, NINT signal goes back high.	RegEventStatus	
0x09	RegEventStatus	0x00	7:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as config register occured). Writing '1' clears the bit in RegEventStatus and in Reg If the edge sensitivity of the IO is changed, the bit(s) w	ured in relevant RegSense InterruptSource if relevant.	
			7:6	Reserved. Must be set to 0 (default value)	•	
0.10		0.00	5:4	PLDModeHigh (applies to I/O[7:4]) 00 : PLD disabled – Normal GPIO mode for I/O[7:4] 01 : PLD 2-to-1 mode – I/O[6] is a decode of I/O[5:4] a 10 : PLD 3-to-1 mode – I/O[7] is a decode of I/O[6:4] a 11 : Reserved		
0x10	RegPLDMode	0x00	3:2	Reserved. Must be set to 0 (default value) PLDModeLow (applies to I/O[3:0])		
			1:0	00: PLD disabled – Normal GPIO mode for I/O[3:0] 01: PLD 2-to-1 mode – I/O[2] is a decode of I/O[1:0] a 10: PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] a 11: PLD 3-to-2 mode – I/O[4:3] are decodes of I/O[2:0] and RegPLDTable4	s defined in RegPLDTable2	
			7	Value to be output on I/O[6] when I/O[5:4] = 11		
			6	Value to be output on I/O[6] when I/O[5:4] = 10	 Applies only when PLDModeHigh is set to PLD 2- 	
			5	Value to be output on I/O[6] when I/O[5:4] = 01	to-1 mode	
0x11	RegPLDTable0	0x00	4	Value to be output on I/O[6] when I/O[5:4] = 00		
	Ū		3	Value to be output on $I/O[2]$ when $I/O[1:0] = 11$	Applies only when	
			2	Value to be output on $I/O[2]$ when $I/O[1:0] = 10$ Value to be output on $I/O[2]$ when $I/O[1:0] = 01$	PLDModeLow is set to PLD 2-	
			0	Value to be output on $I/O[2]$ when $I/O[1:0] = 01$ Value to be output on $I/O[2]$ when $I/O[1:0] = 00$	_ to-1 mode	
			7	Value to be output on $I/O[7]$ when $I/O[6:4] = 111$	1	
			6	Value to be output on $I/O[7]$ when $I/O[6:4] = 110$	1	
			5	Value to be output on I/O[7] when I/O[6:4] = 101		
0x12	RegPLDTable1	0x00	4	Value to be output on I/O[7] when I/O[6:4] = 100	 Applies only when PLDModeHigh is set to PLD 3- 	
			3	Value to be output on $I/O[7]$ when $I/O[6:4] = 011$	to-1 mode	
			2	Value to be output on $I/O[7]$ when $I/O[6:4] = 010$	4	
			<u>1</u> 0	Value to be output on $I/O[7]$ when $I/O[6:4] = 001$ Value to be output on $I/O[7]$ when $I/O[6:4] = 000$	-	
			7	Value to be output on $I/O[7]$ when $I/O[6:4] = 000$ Value to be output on $I/O[3]$ when $I/O[2:0] = 111$		
			6	Value to be output on $I/O[3]$ when $I/O[2:0] = 110$	1	
			5	Value to be output on $I/O[3]$ when $I/O[2:0] = 101$	1	
0.40	RegPLDTable2 0x00		4	Value to be output on I/O[3] when I/O[2:0] = 100	 Applies only when PLDModeLow is set to PLD 3- 	
			3	Value to be output on I/O[3] when I/O[2:0] = 011	to-1 mode	
0x13	Regi LD Tablez					
0x13	Regi Lo tablez		2	Value to be output on $I/O[3]$ when $I/O[2:0] = 010$		
UX13			2 1	Value to be output on I/O[3] when I/O[2:0] = 001		
			2 1 0	Value to be output on I/O[3] when I/O[2:0] = 001 Value to be output on I/O[3] when I/O[2:0] = 000		
0x13 0x14	RegPLDTable3	0x00	2 1	Value to be output on I/O[3] when I/O[2:0] = 001	Applies only when PLDModeLow is set to PLD 3-	



SX1504/SX1505/SX1506 4/8/16 Channel GPIO

WIRELESS & SENSING

Addr	Name	Default	Bits	Description	
			4	Value to be output on I/O[4] when I/O[2:0] = 100	
			3	Value to be output on I/O[4] when I/O[2:0] = 011	
			2	Value to be output on I/O[4] when I/O[2:0] = 010	
			1	Value to be output on I/O[4] when I/O[2:0] = 001	
			0	Value to be output on I/O[4] when I/O[2:0] = 000	
			7	Value to be output on I/O[3] when I/O[2:0] = 111	
			6	Value to be output on I/O[3] when I/O[2:0] = 110	
			5	Value to be output on I/O[3] when I/O[2:0] = 101	Angling and such as
0x15	RegPLDTable4	0x00	4	Value to be output on I/O[3] when I/O[2:0] = 100	Applies only when PLDModeLow is set to PLD 3-
0.15	Keyr LD Table4 0,000	0,000	3	Value to be output on I/O[3] when I/O[2:0] = 011	to-2 mode
		2	2	Value to be output on I/O[3] when I/O[2:0] = 010	
		1	Value to be output on I/O[3] when I/O[2:0] = 001]	
		0	Value to be output on I/O[3] when I/O[2:0] = 000		

Table 14 – SX1505 Configuration Registers Description

5.3 SX1506 16-channel GPIO

Address	Name	Description	Default
0x00	RegDataB	Data register for Bank B I/O[15:8]	1111 1111
0x01	RegDataA	Data register for Bank A I/O[7:0]	1111 1111
0x02	RegDirB	Direction register for Bank B I/O[15:8]	1111 1111
0x03	RegDirA	Direction register for Bank A I/O[7:0]	1111 1111
0x04	RegPullUpB	Pull-up register for Bank B I/O[15:8]	0000 0000
0x05	RegPullUpA	Pull-up register for Bank A I/O[7:0]	0000 0000
0x06	RegPullDownB	Pull-down register for Bank B I/O[15:8]	0000 0000
0x07	RegPullDownA	Pull-down register for Bank A I/O[7:0]	0000 0000
0x08	RegInterruptMaskB	Interrupt mask register for Bank B I/O[15:8]	1111 1111
0x09	RegInterruptMaskA	Interrupt mask register for Bank A I/O[7:0]	1111 1111
0x0A	RegSenseHighB	Sense register for I/O[15:12]	0000 0000
0x0B	RegSenseHighA	Sense register for I/O[7:4]	0000 0000
0x0C	RegSenseLowB	Sense register for I/O[11:8]	0000 0000
0x0D	RegSenseLowA	Sense register for I/O[3:0]	0000 0000
0x0E	RegInterruptSourceB	Interrupt source register for Bank B I/O[15:8]	0000 0000
0x0F	RegInterruptSourceA	Interrupt source register for Bank A I/O[7:0]	0000 0000
0x10	RegEventStatusB	Event status register for Bank B I/O[15:8]	0000 0000
0x11	RegEventStatusA	Event status register for Bank A I/O[7:0]	0000 0000
0x20	RegPLDModeB	PLD mode register for Bank B I/O[15:8]	0000 0000
0x21	RegPLDModeA	PLD mode register for Bank A I/O[7:0]	0000 0000
0x22	RegPLDTable0B	PLD truth table 0 for Bank B I/O[15:8]	0000 0000
0x23	RegPLDTable0A	PLD truth table 0 for Bank A I/O[7:0]	0000 0000
0x24	RegPLDTable1B	PLD truth table 1 for Bank B I/O[15:8]	0000 0000
0x25	RegPLDTable1A	PLD truth table 1 for Bank A I/O[7:0]	0000 0000
0x26	RegPLDTable2B	PLD truth table 2 for Bank B I/O[15:8]	0000 0000
0x27	RegPLDTable2A	PLD truth table 2 for Bank A I/O[7:0]	0000 0000
0x28	RegPLDTable3B	PLD truth table 3 for Bank B I/O[15:8]	0000 0000
0x29	RegPLDTable3A	PLD truth table 3 for Bank A I/O[7:0]	0000 0000
0x2A	RegPLDTable4B	PLD truth table 4 for Bank B I/O[15:8]	0000 0000
0x2B	RegPLDTable4A	PLD truth table 4 for Bank A I/O[7:0]	0000 0000
0xAD	RegAdvanced	Advanced settings register	0000 0000

Table 15 – SX1506 Configuration Registers Overview

Addr Name Default Bits Description		Description			
0x00			7:0	Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.	
0x01 RegDataA 0xFF 7:0 Write: Data to be output to the output-configured IOs Read: Data seen at the IOs, independent of the direction configured.					
0x02	0x02 RegDirB 0xFF 7:0		7:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input	



Addr	Name	Default	Bits	Description		
0x03	RegDirA	0xFF	7:0	Configures direction for each IO. 0 : IO is configured as an output 1 : IO is configured as an input		
0x04	RegPullUpB	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled		
0x05	RegPullUpA	0x00	7:0	Enables the pull-up for each IO 0 : Pull-up is disabled 1 : Pull-up is enabled		
0x06	RegPullDownB	0x00	7:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled		
0x07	RegPullDownA	0x00	7:0	Enables the pull-down for each IO 0 : Pull-down is disabled 1 : Pull-down is enabled		
0x08	RegInterruptMaskB	0xFF	7:0	Configures which [input-configured] IO will trigger an inte 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt		
0x09	RegInterruptMaskA	0xFF	7:0	Configures which [input-configured] IO will trigger an inte 0 : An event on this IO will trigger an interrupt 1 : An event on this IO will NOT trigger an interrupt	errupt on NINT pin	
			7:6	Edge sensitivity of I/O[15]	00 : None	
0x0A	RegSenseHighB	0x00	5:4	Edge sensitivity of I/O[14]	01 : Rising 10 : Falling	
			3:2 1:0	Edge sensitivity of I/O[13] Edge sensitivity of I/O[12]	11 : Both	
			7:6	Edge sensitivity of I/O[7]	00 - Nana	
0.00		000	5:4	Edge sensitivity of I/O[6]	00 : None 01 : Rising	
0x0B	RegSenseHighA	0x00	3:2	Edge sensitivity of I/O[5]	10 : Falling	
			1:0	Edge sensitivity of I/O[4]	11 : Both	
	RegSenseLowB		7:6	Edge sensitivity of I/O[11]	00 : None	
0x0C		0x00	5:4	Edge sensitivity of I/O[10]	01 : Rising 10 : Falling	
			3:2 1:0	Edge sensitivity of I/O[9] Edge sensitivity of I/O[8]	11 : Both	
		0x00	7:6	Edge sensitivity of I/O[3]	00 : None	
0x0D	RegSenseLowA		5:4	Edge sensitivity of I/O[2]	01 : Rising	
UNUE	RegoenselowA		3:2	Edge sensitivity of I/O[1]	10 : Falling	
0x0E	RegInterruptSourceB	0x00	1:0 7:0	Edge sensitivity of I/O[0] 11 : Both Interrupt source (from IOs set in RegInterruptMaskB) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured). Writing '1' clears the bit in RegInterruptSourceB and in RegEventStatusB When all bits of both RegInterruptSourceA/B are cleared, NINT signal goes back high.		
0x0F	RegInterruptSourceA	0x00	7:0	Interrupt source (from IOs set in RegInterruptMaskA) 0 : No interrupt has been triggered by this IO 1 : An interrupt has been triggered by this IO (an event as configured in relevant RegSense register occured). Writing '1' clears the bit in RegInterruptSourceA and in RegEventStatusA When all bits of both RegInterruptSourceA/B are cleared, NINT signal goes back high.		
0x10	RegEventStatusB	0x00	7:0	 Which all bits of both recementarios observed are cleared, with signal goes back high. Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as configured in relevant RegSense register occured). Writing '1' clears the bit in RegEventStatusB and in RegInterruptSourceB if relevant. If the edge sensitivity of the IO is changed, the bit(s) will be cleared automatically 		
0x11	RegEventStatusA	0x00	7:0	Event status of all IOs. 0 : No event has occured on this IO 1 : An event has occured on this IO (an edge as configured in relevant RegSense		
				If the edge sensitivity of the IO is changed, the bit(s) will	be cleared automatically	
0x20		0x00	7:6	Reserved. Must be set to 0 (default value)		



SX1504/SX1505/SX1506 4/8/16 Channel GPIO

WIRELESS & SENSING

Addr	Name	Default	Bits	Description			
	RegPLDModeB			PLDModeHighB (applies to I/O[15:12])			
			E.A	00 : PLD disabled – Normal GPIO mode for I/O[15:12]	an defined in DearDI DT-blach		
			5:4	01 : PLD 2-to-1 mode – I/O[14] is a decode of I/O[13:12] as defined in RegPLDTable0B 10 : PLD 3-to-1 mode – I/O[15] is a decode of I/O[14:12] as defined in RegPLDTable1B			
				11 : Reserved			
			3:2	Reserved. Must be set to 0 (default value)			
				PLDModeLowB (applies to I/O[11:8])			
				00 : PLD disabled – Normal GPIO mode for I/O[11:8]			
			1:0	01 : PLD 2-to-1 mode – I/O[10] is a decode of I/O[9:8] as defined in RegPLDTable0B			
			1.0	10 : PLD 3-to-1 mode – I/O[11] is a decode of I/O[10:8]			
				11 : PLD 3-to-2 mode – I/O[12:11] are decodes of I/O[1 RegPLDTable3B and RegPLDTable4B	0:8] as defined in		
			7:6	Reserved. Must be set to 0 (default value)			
			1.0	PLDModeHighA (applies to I/O[7:4])			
				00 : PLD disabled – Normal GPIO mode for I/O[7:4]			
			5:4	01 : PLD 2-to-1 mode - I/O[6] is a decode of I/O[5:4] as			
				10 : PLD 3-to-1 mode – I/O[7] is a decode of I/O[6:4] as	s defined in RegPLDTable1A		
0x21		0x00		11 : Reserved			
0721	RegPLDModeA	0,000	3:2	Reserved. Must be set to 0 (default value)			
				PLDModeLowA (applies to I/O[3:0]) 00 : PLD disabled – Normal GPIO mode for I/O[3:0]			
				01 : PLD disabled - Normal GF10 mode for $1/O[3.0]01 : PLD 2-to-1 mode - 1/O[2] is a decode of 1/O[1:0] as$	s defined in RegPI DTable0A		
			1:0	10 : PLD 3-to-1 mode – I/O[3] is a decode of I/O[2:0] as	s defined in RegPLDTable2A		
				11 : PLD 3-to-2 mode – I/O[4:3] are decodes of I/O[2:0]	as defined in RegPLDTable3A		
				and RegPLDTable4A			
			7	Value to be output on $I/O[14]$ when $I/O[13:12] = 11$	Applies only when		
			6	Value to be output on $I/O[14]$ when $I/O[13:12] = 10$	PLDModeHighB is set to PLD		
	RegPLDTable0B 0x00		5	Value to be output on $I/O[14]$ when $I/O[13:12] = 01$	2-to-1 mode		
0x22		RegPLDTable0B 0x00	4	Value to be output on $I/O[14]$ when $I/O[13:12] = 00$			
			3	Value to be output on $I/O[10]$ when $I/O[9:8] = 11$	Applies only when		
			2	Value to be output on $I/O[10]$ when $I/O[9:8] = 10$	PLDModeLowB is set to PLD		
			1 0	Value to be output on $I/O[10]$ when $I/O[9:8] = 01$ Value to be output on $I/O[10]$ when $I/O[9:8] = 00$	2-to-1 mode		
			7	Value to be output on $I/O[6]$ when $I/O[5:4] = 11$			
			6	Value to be output on $I/O[6]$ when $I/O[5:4] = 10$	Applies only when		
			5	Value to be output on $I/O[6]$ when $I/O[5:4] = 01$	PLDModeHighA is set to PLD		
			4	Value to be output on $I/O[6]$ when $I/O[5:4] = 00$	2-to-1 mode		
0x23	0x23 RegPLDTable0A	RegPLDTable0A	RegPLDTable0A 0x00	0x00	3	Value to be output on $I/O[2]$ when $I/O[1:0] = 11$	
			2	Value to be output on $I/O[2]$ when $I/O[1:0] = 10$	Applies only when		
			1	Value to be output on I/O[2] when I/O[1:0] = 01	PLDModeLowA is set to PLD 2-to-1 mode		
			0	Value to be output on I/O[2] when I/O[1:0] = 00	2-10-1 11000		
			7	Value to be output on I/O[15] when I/O[14:12] = 111			
			6	Value to be output on I/O[15] when I/O[14:12] = 110			
			5	Value to be output on I/O[15] when I/O[14:12] = 101			
0x24	RegPLDTable1B	0x00	4	Value to be output on I/O[15] when I/O[14:12] = 100	Applies only when PLDModeHighB is set to PLD		
0724	Regi ED labie ID	0,00	3	Value to be output on I/O[15] when I/O[14:12] = 011	3-to-1 mode		
			2	Value to be output on I/O[15] when I/O[14:12] = 010			
			1	Value to be output on I/O[15] when I/O[14:12] = 001			
			0	Value to be output on I/O[15] when I/O[14:12] = 000			
			7	Value to be output on $I/O[7]$ when $I/O[6:4] = 111$	4		
			6	Value to be output on $I/O[7]$ when $I/O[6:4] = 110$	4		
			5	Value to be output on $I/O[7]$ when $I/O[6:4] = 101$	Applies only when		
0x25	RegPLDTable1A	0x00	4	Value to be output on $I/O[7]$ when $I/O[6:4] = 100$	PLDModeHighA is set to PLD		
			3	Value to be output on $I/O[7]$ when $I/O[6:4] = 011$	3-to-1 mode		
			2	Value to be output on $I/O[7]$ when $I/O[6:4] = 010$	4		
			1	Value to be output on $I/O[7]$ when $I/O[6:4] = 001$	4		
			0 7	Value to be output on $I/O[7]$ when $I/O[6:4] = 000$			
			6	Value to be output on $I/O[11]$ when $I/O[10:8] = 111$	-		
			<u>6</u> 5	Value to be output on $I/O[11]$ when $I/O[10:8] = 110$ Value to be output on $I/O[11]$ when $I/O[10:8] = 101$	-		
	RegPLDTable2B				Applies only when		
0x26		le2B $0x00 \qquad 4 \qquad Value to be output on I/O[11] when I/O[10:8] = 100 PLC$	PLDModeLowB is set to PLD				
			2	Value to be output on $I/O[11]$ when $I/O[10:8] = 010$	3-to-1 mode		
			1	Value to be output on $I/O[11]$ when $I/O[10:8] = 001$	1		
			0	Value to be output on $I/O[11]$ when $I/O[10:8] = 001$	1		
0x27		0x00	7	Value to be output on $I/O[3]$ when $I/O[2:0] = 111$	Applies only when		
		57.00					



SX1504/SX1505/SX1506 4/8/16 Channel GPIO

WIRELESS & SENSING

Addr	Name	Default	Bits	Description	
	RegPLDTable2A		6	Value to be output on I/O[3] when I/O[2:0] = 110	PLDModeLowA is set to PLD
			5	Value to be output on I/O[3] when I/O[2:0] = 101	3-to-1 mode
			4	Value to be output on I/O[3] when I/O[2:0] = 100	
			3	Value to be output on I/O[3] when I/O[2:0] = 011	
			2	Value to be output on I/O[3] when I/O[2:0] = 010	
			1	Value to be output on I/O[3] when I/O[2:0] = 001	
			0	Value to be output on I/O[3] when I/O[2:0] = 000	
			7	Value to be output on I/O[11] when I/O[10:8] = 111	
			6	Value to be output on I/O[11] when I/O[10:8] = 110	
			5	Value to be output on I/O[11] when I/O[10:8] = 101	
0x28	RegPLDTable3B	0x00	4	Value to be output on I/O[11] when I/O[10:8] = 100	 Applies only when PLDModeLowB is set to PLD
0/20	Regi ED Tubleob	0,00	3	Value to be output on I/O[11] when I/O[10:8] = 011	3-to-2 mode
			2	Value to be output on I/O[11] when I/O[10:8] = 010	
			1	Value to be output on I/O[11] when I/O[10:8] = 001	
			0	Value to be output on I/O[11] when I/O[10:8] = 000	
			7	Value to be output on I/O[3] when I/O[2:0] = 111	
			6	Value to be output on I/O[3] when I/O[2:0] = 110	
			5	Value to be output on I/O[3] when I/O[2:0] = 101	Applies only when
0x29	RegPLDTable3A	0x00	4	Value to be output on I/O[3] when I/O[2:0] = 100	PLDModeLowA is set to PLD
0/20			3	Value to be output on I/O[3] when I/O[2:0] = 011	3-to-2 mode
			2	Value to be output on I/O[3] when I/O[2:0] = 010	
			1	Value to be output on I/O[3] when I/O[2:0] = 001	
			0	Value to be output on I/O[3] when I/O[2:0] = 000	
			7	Value to be output on I/O[12] when I/O[10:8] = 111	
		0x00	6	Value to be output on I/O[12] when I/O[10:8] = 110	
			5	Value to be output on I/O[12] when I/O[10:8] = 101	Applies only when
0x2A	RegPLDTable4B		4	Value to be output on I/O[12] when I/O[10:8] = 100	- PLDModeLowB is set to PLD
0/12/1			3	Value to be output on I/O[12] when I/O[10:8] = 011	3-to-2 mode
			2	Value to be output on I/O[12] when I/O[10:8] = 010	
			1	Value to be output on I/O[12] when I/O[10:8] = 001	
			0	Value to be output on I/O[12] when I/O[10:8] = 000	
			7	Value to be output on I/O[4] when I/O[2:0] = 111	_
			6	Value to be output on I/O[4] when I/O[2:0] = 110	
			5	Value to be output on I/O[4] when I/O[2:0] = 101	Applies only when
0x2B	RegPLDTable4A	0x00	4	Value to be output on I/O[4] when I/O[2:0] = 100	 PLDModeLowA is set to PLD
			3	Value to be output on I/O[4] when I/O[2:0] = 011	3-to-2 mode
			2	Value to be output on I/O[4] when I/O[2:0] = 010	
			1	Value to be output on I/O[4] when I/O[2:0] = 001	_
			0	Value to be output on I/O[4] when I/O[2:0] = 000	
			7:3	Reserved. Must be set to 0 (default value)	
0xAD	RegAdvanced	0x00	2	Autoclear NINT on RegData read (Cf. §4.6) 0: OFF.RegInterruptSource must be manually cleared 1: ON.RegInterruptSource is automatically cleared wh	directly or via RegEventStatus en RegDataB or RegDataA is read
			1:0	Reserved. Must be set to 0 (default value)	

Table 16 – SX1506 Configuration Registers Description



6 APPLICATION INFORMATION

6.1 Typical Application Circuit



Figure 12 - Typical Application Schematic

6.2 Typical LED Operation

Typical LED operation is described below. The LED is usually connected to a high voltage (VBAT) to take advantage of the high sink current of the I/O and to accommodate high LED threshold voltages (VLED).



LED colour/technology dependent

Figure 13 – Typical LED Operation

Important:

- VCCx must exceed VBAT-VLED (VCCx = VBAT is recommended) else the LED will never be completely OFF
- R must be calculated for IOL not to exceed its max spec (Cf. Table 5)

6.2.1 LED ON/OFF Control

	RegDir[x]	RegData[x]
LED ON	"0" (Output)	" O "
LED OFF		"1"

Table 17 – LED ON/OFF Control



6.2.2 LED Intensity Control

When the max IOL spec is not enough it is possible to drive simultaneously multiple I/Os connected together hence increasing the total sink capability.

Example: on an SX1505, by driving an LED with both IO[2] and IO[3] one can sink up to 24+24 =48mA.

Driving an LED with multiple I/Os can also be used to implement more intensity steps for the LED. Example: with two I/Os capable of sinking each 24mA the LED can sink a total of 0mA (no I/O set to "0"), 24mA (one I/O set to "0") or 48mA (both I/Os set to "0") => 3 LED intensity steps (4 steps with 3 I/Os, 5 steps with 4 I/Os, etc)

6.3 Keypad Implementation

SX1504, SX1505, and SX1506 can be used to implement keypad applications up to 8x8 matrix (i.e. 64 keys)

Example: We want to implement a 4x4matrix keypad on SX1505



Figure 14 – 4x4 keypad connection to SX1505

- 1. Set all I/Os as inputs with internal pull-up (RegDir = 0xFF, RegPullUp = 0xFF)
- 2. Set NINT to be triggered on any IO's falling edge (RegInterruptMask = 0x00, RegSenseHigh = 0xAA, RegSenseLow = 0xAA)
- 3. When NINT goes low read RegData (or RegInterruptSource) to know the X:Y coordinates of the button which has been pressed.
- 4. Clear NINT (RegInterruptSource = 0xFF, can be done automatically on SX1506 depending on RegAdvanced setting)
- 5. Restart from point 3

6.4 Level Shifter Implementation Hints

Because of their I/O banks with independent supply voltages between 2.5V and 5.5V, the SX1505 and SX1506 can be used to perform level shifting of signals from one I/O bank to an other (uC reads I/O from one I/O bank and sends it back to the other I/O bank)

This can save significant BOM cost in a final application where only a few slow signals need to be level-shifted.



7 PACKAGING INFORMATION

7.1 QFN-UT 20-pin Outline Drawing





DIMENSIONS								
	11	NCHE	S	MILLIMETERS				
DIM	MN	NOM	MAX	MIN	NOM	MAX		
Α	.020	-	.024	0.50	-	0.60		
A1	.000	-	.002	0.00	-	0.05		
A2		(.006)			(0.152)			
b	.006	.008	.010	0.15	0.20	0.25		
D	.114	.118	.122	2.90	3.00	3.10		
D1	.061	.067	.071	1.55	1.70	1.80		
Е	.114	.118	.122	2.90	3.00	3.10		
E1	.061	.067	.071	1.55	1.70	1.80		
е		016 BS	С	0	.40 BS	C		
Γ	.012	.016	.020	0.30	0.40	0.50		
Ν		20			20			
aaa	.003				0.08			
bbb		.004			0.10			

NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
- 3. DAP IS 1.90 x 1.90mm.

Figure 15 - Packaging Information – QFN-UT 20-pin Outline Drawing

7.2 QFN-UT 20-pin Land Pattern



	DIMENSIONS					
DIM	INCHES	MILLIMETERS				
С	(.114)	(2.90)				
G	.083	2.10				
Н	.067	1.70				
К	.067	1.70				
Р	.016	0.40				
R	.004	0.10				
Х	.008	0.20				
Ý	.031	0.80				
Ζ	.146	3.70				

NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
- 3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

Figure 16 - Packaging Information – QFN-UT 20-pin Land Pattern



0.60

0.02

2,75

28

0.08

0.10

WIRELESS & SENSING

7.3 **QFN-UT 28-pin Outline Drawing**

QFN-UT 28-pin, 4 x 4 mm, 0.4 mm pitch



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 17 - Packaging Information – QFN-UT 28-pin Outline Drawing

7.4 **QFN-UT 28-pin Land Pattern**



NOTES:

- 1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
- 3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
- 4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

Figure 18 - Packaging Information – QFN-UT 28-pin Land Pattern



8 SOLDERING PROFILE

The soldering reflow profile for the SX1504, SX1505 and SX1506 is described in the standard IPC/JEDEC J-STD-020C. For detailed information please go to <u>http://www.jedec.org/download/search/jstd020c.pdf</u>

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly	
Average Ramp-Up Rate (Ts _{max} to Tp)	3 °C/second max.	3° C/second max.	
Preheat – Temperature Min (Ts _{min}) – Temperature Max (Ts _{max}) – Time (ts _{min} to ts _{max})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-180 seconds	
Time maintained above: – Temperature (T _L) – Time (t _L)	183 °C 60-150 seconds	217 °C 60-150 seconds	
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2	
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds	
Ramp-Down Rate	6 °C/second max.	6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.	

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



Figure 19 - Classification Reflow Profile (IPC/JEDEC J-STD-020C)



© Semtech 2012

All rights reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights. Semtech assumes no responsibility or liability whatsoever for any failure or unexpected operation resulting from misuse, neglect improper installation, repair or improper handling or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified range.

SEMTECH PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF SEMTECH PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK. Should a customer purchase or use Semtech products for any such unauthorized application, the customer shall indemnify and hold Semtech and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs damages and attorney fees which could arise.

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contact Information			
Taiwan	Tel: 886-2-2748-3380	Switzerland	Tel: 41-32-729-4000
	Fax: 886-2-2748-3390		Fax: 41-32-729-4001
Korea	Tel: 82-2-527-4377	United Kingdom	Tel: 44-1794-527-600
	Fax: 82-2-527-4376		Fax: 44-1794-527-60
Shanghai	Tel: 86-21-6391-0830	France	Tel: 33-(0)169-28-22-00
	Fax: 86-21-6391-0831		Fax: 33-(0)169-28-12-98
Japan	Tel: 81-3-6408-0950	Germany	Tel: 49-(0)8161-140-123
	Fax: 81-3-6408-0951		Fax: 49-(0)8161-140-124

Semtech International AG is a wholly-owned subsidiary of Semtech Corporation, which has its headquarters in the U.S.A