Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

FEDL620Q504H-02
Issue Date: May. 20, 2020

# ML620Q503H/Q504H

**Ultra Low Power 16-bit Microcontroller**

## GENERAL DESCRIPTION

This LSI family is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, $I^2C$ bus interface (master), supply voltage level detect circuit, RC oscillation type A/D converter, and successive approximation type A/D converter are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM* that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications. And, this LSI has a data flash-memory* fill area by a software which can be written in.
The on-chip debug function that is installed enables program debugging and programming.

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc. SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

## FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Build-in On-Chip debug function
  - Minimum instruction execution time
    30.5 µs (@32.768 kHz system clock)
    62.5ns (@16 MHz system clock)

- Built-in coprocessor for multiplication, division, and multiply-accumulate operations
  - Signed or unsigned operation setting
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Internal memory
  - Supports ISP function (re-writing the program memory area by software)
  - Number of segments

| Product name | Flash memory | | SRAM |
|---|---|---|---|
| | Program area** | Data area | |
| ML620Q503H | 32KB (16K × 16bit) | 2KB (1K × 16bit) | 2KB (1K × 16bit) |
| ML620Q504H | 64KB (32K × 16bit) | 2KB (1K × 16bit) | 6KB (3K × 16bit) |

**: including 1KB of unusable test area

- Interrupt controller (INTC)
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 37 maskable interrupt sources (Internal sources: 29, External sources: 8)
  - Software interrupt (SWI): maximum 64 sources
  - External interrupts and comparator allow edge selection and sampling selection
  - Priority level (4-level) can be set for each interrupt

- Time base counter (TBC)
  - Low-speed time base counter ×1 channel
- Timers (TMR)
  - 8 bits × 8 channels
    (Timer0-7: 16-bit × 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  - Selection of one shot timer mode is possible
  - External clock can be selected as timer clock.

- Function Timers (FTM)
  - 16-bit × 4 channels
  - Equipped with the timer/capture/PWM functions using a 16-bit counter
  - Timer start/stop function by software/event trriger(external pin or other timer)
  - External pin can be selected as counter clock
  - Capture function (the measurement such as the pulse width is possible using external trigger input)
  - Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Watchdog timer (WDT)
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/SSIO)
  - without FIFOs (SSIO) : 1 channel
  - with 4-byte transmits and receives FIFOs (SSIOF) : 1 channel
  - Master/slave are selectable
  - LSB first/MSB first are selectable
  - 8-bit length/16-bit length are selectable
  - Phase/Polarity of clock are selectable
  - supports slave-select signal (only SSIOF)

- UART (UARTF/UART)
  - without FIFOs (UART) : 1ch
  - with 4-byte transmits and receives FIFOs (UARTF) : 1ch
  - Full duplex buffer system
  - Communication speed: Settable within the range of 2400bps to 115200bps.
  - Programmable interface (data length, parity, stop bits selectable)

- $I^2C$ bus interface ($I^2C$)
  - Master function × 2 channel
  - Fast mode (400 kbps), standard mode (100 kbps)

- General-purpose ports (PORT)
  - Input port × 2, Input/output port × 36 channels

- Melody driver (MELODY)
  - Tempo: 15 types
  - Scale: 29 types (Melody sound frequency: 508 Hz to 10.922 kHz)
  - Tone length: 63 types
  - Buzzer output mode (4 output modes, 8 buzzer frequencies, 7duty levels at 4.096kHz /15 duty levels at other buzzer frequencies)

- RC oscillation type A/D converter (RC-ADC)
  - Time division × 2 channels
  - 24-bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12-bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2ch
  - Common mode input voltage: 0.2V to $V_{DD}$－0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages:  selectable from 13 levels
  - interrupt or reset generate are selectable

- Low Level Detector(LLD)
  - Judgement Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by Voltage Leve Supervisor(VLS)
  - Reset by Low Level Detector(LLD)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    - Crystal oscillation (32.768 kHz)
    - External clock input (30kHz to 36kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - Crystal/Ceramic oscillation (16 MHz)
    - External clock input (300kHz to 16 MHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTB, etc.) can keep in operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Die * Please contact our responsible sales person for the pad layout information.
  - 48-pin plastic TQFP Tray/Tape and Reel
    ML620Q503H-xxxTB
    ML620Q504H-xxxTB

- Guaranteed operating range
  - Operating temperature (ambient) : –40°C to +85°C
  - Operating voltage: $V_{DD}$ = 1.8V to 5.5V

## BLOCK DIAGRAM

### Block Diagram of ML620Q503H/Q504H

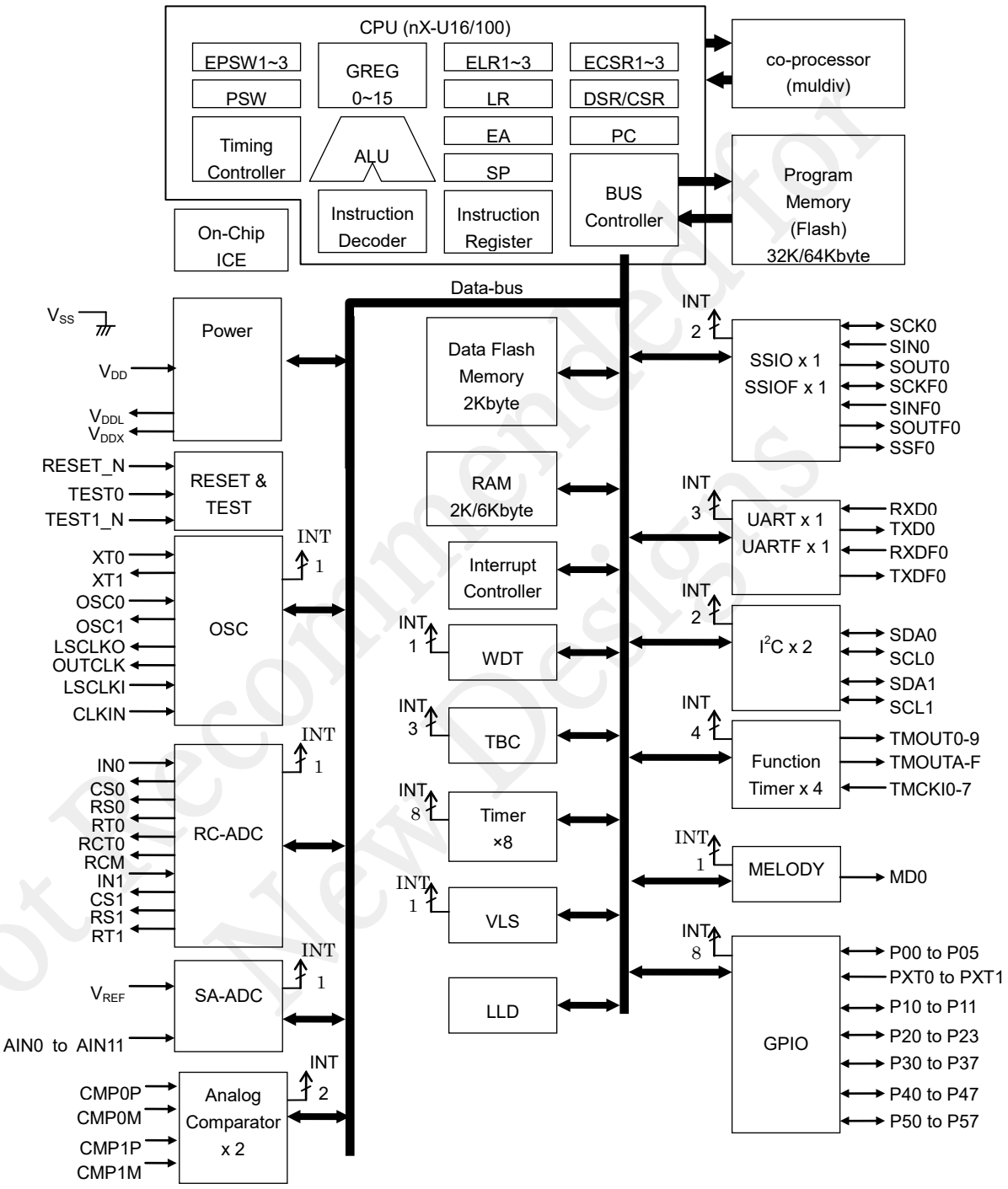
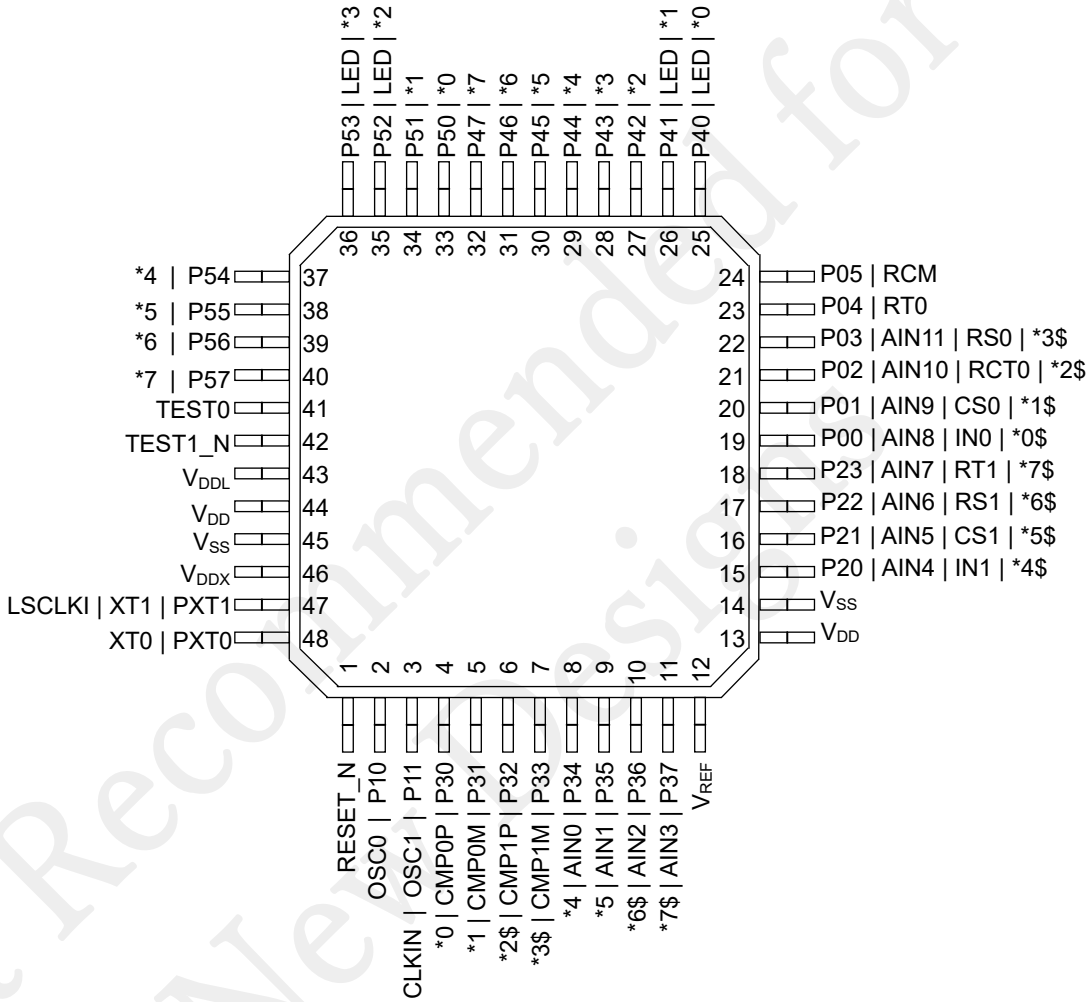



**Figure 1. Block Diagram of ML620Q503H/Q504H**

## PIN CONFIGURATION

### Pin Layout of ML620Q503H/Q504H TQFP Package




External intteruput inputpin(EXI) can be assigned to P00-P05, PXT0-1, P20-P57.
*0 to *7 and *0$ to *7$ has following functions. But 0$-7$ has limited function. Please refer to the pin list.

| | |
|---|---|
| *0 : SDA0, SOUT0, RXD0 | *4 : SDA1, SOUTF0, RXDF0 |
| *1 : SCL0, SIN0 , TXD0 | *5 : SCL1, SINF0, TXDF0 |
| *2 : SCK0, TMOUT ,TMCKI | *6 : LSCLKO,SCKF0, TMOUT, TMCKI |
| *3 : MD0, TMOUT , TMCKI | *7 : OUTCLK,SSF0, TMOUT, TMCKI |
| *0$ : SOUT0, RXD0 | *4$ : SOUTF0, RXDF0 |
| *1$ : SIN0 , TXD0 | *5$ : SIN F0, TXDF0 |
| *2$ : SCK0, TMOUT | *6$ : SCKF0, TMOUT |
| *3$ : MD0(P33 only), TMOUT | *7$ : SSF0, TMOUT |

**Figure 2. Pin Layout of ML620Q503H/Q504H TQFP Package**

## PIN LIST

| PKG Pin No. | 1st Function | | | | 2nd/3rd/4th Function | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin name | I/O | Reset State | Function | pin name | I/O | function | pin name | I/O | function | pin name | I/O | function |
| 14, 45 | $V_{SS}$ | – | – | Negative power supply pin | – | – | – | – | – | – | – | – | – |
| 13, 44 | $V_{DD}$ | – | – | Positive power supply pin | – | – | – | – | – | – | – | – | – |
| 43 | $V_{DDL}$ | – | – | Power supply pin for internal circuit (internally generated) | – | – | – | – | – | – | – | – | – |
| 46 | $V_{DDX}$ | – | – | Power supply pin for internal circuit (internall generated) | – | – | – | – | – | – | – | – | – |
| 12 | $V_{REF}$ | I | – | Reference voltage input pin of SA-ADC | – | – | – | – | – | – | – | – | – |
| 1 | RESET_N | I | Pull-up Input | Reset input pin | – | – | – | – | – | – | – | – | – |
| 42 | TEST1_N | I | Pull-up Input | Input pin for testing | – | – | – | – | – | – | – | – | – |
| 41 | TEST0 | I/O | Pull-down Input | Input/output pin for testing | – | – | – | – | – | – | – | – | – |
| 48 | PXT0/ EXII0/ XT0 | I | Input disable | Input port/ External interrupt/ Low-speed oscillation port | – | – | – | – | – | – | – | – | – |
| 47 | PXT1/ EXI1/ XT1/ LSCLKI | I/O | Hi-Z output | Input-Output port/ External interrupt/ Low-speed oscillation port Low-speed external clock input | – | – | – | – | – | – | – | – | – |
| 19 | P00/ EXI00/ AIN8 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | IN0 | I | RC-ADC oscillation input | SOUT0 | O | SSIO data output | RXD0 | I | UART data input |
| 20 | P01/ EXI01/ AIN9 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | CS0 | O | RC-ADC reference capacitance connection pin | SIN0 | I | SSIO data input | TXD0 | O | UART data output |
| 21 | P02/ EXI02/ AIN10 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | RCT0 | O | RCADC resistor/capacitor sensor connection pin | SCK0 | I/O | SSIO clock input/output | TMOUT0 | O | FTM output |
| 22 | P03/ EXI03/ AIN11 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | RS0 | O | RC-ADC reference resistor connection pin | – | – | – | TMOUT1 | O | FTM output |
| 23 | P04/ EXI04 | I/O | Hi-Z output | Input-Output port/ External interrupt | RT0 | O | RC-ADC measurement resistor sensor connection pin | – | – | – | – | – | – |
| 24 | P05/ EXI05 | I/O | Hi-Z output | Input-Output port/ External interrupt | RCM | O | RC-ADC oscillation monitor | – | – | – | – | – | – |
| 2 | P10/ OSC0 | I/O | Hi-Z output | Input-Output port/ High-speed oscillation port | – | – | – | – | – | – | – | – | – |
| 3 | P11/ OSC1/ CLKIN | I/O | Hi-Z output | Input-Output port/ High-speed oscillation port High-speed external clock input | – | – | – | – | – | – | – | – | – |
| 15 | P20/ EXI20/ AIN4 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | IN1 | I | RC-ADC oscillation input | SOUTF0 | O | SSIOF data output | RXDF0 | I | UARTF data input |
| 16 | P21/ EXI21/ AIN5 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | CS1 | O | RC-ADC reference capacitance connection pin | SINF0 | I | SSIOF data input | TXDF0 | O | UARTF data output |
| 17 | P22/ EXI22/ AIN6 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | RS1 | O | RC-ADC reference resistor connection pin | SCKF0 | I/O | SSIOF clock input/output | TMOUT2 | O | FTM output |

| PKG Pin No. | 1st Function | | | | 2nd/3rd/4th Function | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin name | I/O | Reset State | Function | pin name | I/O | function | pin name | I/O | function | pin name | I/O | function |
| 18 | P23/ EXI23/ AIN7 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | RT1 | O | RC-ADC measurement resistor sensor connection pin | SSF0 | I/O | SSIOF select input/output | TMOUT3 | O | FTM output |
| 4 | P30/ EXI30/ CMP0P | I/O | Hi-Z output | Input-Output port/ External interrupt/ Comparator plus input | SDA0 | I/O | $I^2C$ data input/output | SOUT0 | O | SSIO data output | RXD0 | I | UART data input |
| 5 | P31/ EXI31/ CMP0M | I/O | Hi-Z output | Input-Output port/ External interrupt/ Comparator minus input | SCL0 | O | $I^2C$ clock output | SIN0 | I | SSIO data input | TXD0 | O | UART data output |
| 6 | P32/ EXI32/ CMP1P | I/O | Hi-Z output | Input-Output port/ External interrupt/ Comparator plus input | – | – | – | SCK0 | I/O | SSIO clock input/output | TMOUT4 | O | FTM output |
| 7 | P33/ EXI33/ CMP1M | I/O | Hi-Z output | Input-Output port/ External interrupt/ Comparator minus input | MD0 | O | Melody/Buzzer output | – | – | – | TMOUT5 | O | FTM output |
| 8 | P34/ EXI34/ AIN0 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | SDA1 | I/O | $I^2C$ data input/output | SOUTF0 | O | SSIOF data output | RXDF0 | I | UARTF data input |
| 9 | P35/ EXI35/ AIN1 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | SCL1 | O | $I^2C$ clock output | SINF0 | I | SSIOF data input | TXDF0 | O | UARTF data output |
| 10 | P36/ EXI36/ AIN2 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | – | – | – | SCKF0 | I/O | SSIOF clock input/output | TMOUT6 | O | FTM output |
| 11 | P37/ EXI37/ AIN3 | I/O | Hi-Z output | Input-Output port/ External interrupt/ SA-ADC input | – | – | – | SSF0 | I/O | SSIOF select input/output | TMOUT7 | O | FTM output |
| 25 | P40/ EXI40/ LED | I/O | Hi-Z output | Input-Output port/ External interrupt/ LED output | SDA0 | I/O | $I^2C$ data input/output | SOUT0 | O | SSIO data output | RXD0 | I | UART data input |
| 26 | P41/ EXI41/ LED | I/O | Hi-Z output | Input-Output port/ External interrupt/ LED output | SCL0 | O | $I^2C$ clock output | SIN0 | I | SSIO data input | TXD0 | O | UART data output |
| 27 | P42/ EXI42/ TMCKI0 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | – | – | – | SCK0 | I/O | SSIO clock input/output | TMOUT8 | O | FTM output |
| 28 | P43/ EXI43/ TMCKI1 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | MD0 | O | Melody/Buzzer output | – | – | – | TMOUT9 | O | FTM output |
| 29 | P44/ EXI44 | I/O | Hi-Z output | Input-Output port/ External interrupt | SDA1 | I/O | $I^2C$ data input/output | SOUTF0 | O | SSIOF data output | RXDF0 | I | UARTF data input |
| 30 | P45/ EXI45 | I/O | Hi-Z output | Input-Output port/ External interrupt | SCL1 | O | $I^2C$ clock output | SINF0 | I | SSIOF data input | TXDF0 | O | UARTF data output |
| 31 | P46/ EXI46/ TMCKI2 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | LSCLKO | O | Low-speed clock output | SCKF0 | I/O | SSIOF clock input/output | TMOUTA | O | FTM output |
| 32 | P47/ EXI47/ TMCKI3 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | OUTCLK | O | High-speed clock output | SSF0 | I/O | SSIOF select input/output | TMOUTB | O | FTM output |
| 33 | P50/ EXI50 | I/O | Hi-Z output | Input-Output port/ External interrupt | SDA0 | I/O | $I^2C$ data input/output | SOUT0 | O | SSIO data output | RXD0 | I | UART data input |
| 34 | P51/ EXI51 | I/O | Hi-Z output | Input-Output port/ External interrupt | SCL0 | O | $I^2C$ clock output | SIN0 | I | SSIO data input | TXD0 | O | UART data output |
| 35 | P52/ EXI52/ TMCKI4/ LED | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input/ LED output | – | – | – | SCK0 | I/O | SSIO clock input/output | TMOUTC | O | FTM output |
| 36 | P53/ EXI53/ TMCKI5/ LED | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input/ LED output | MD0 | O | Melody/Buzzer output | – | – | – | TMOUTD | O | FTM output |

| PKG Pin No. | 1st Function | | | | 2nd/3rd/4th Function | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Pin name | I/O | Reset State | Function | pin name | I/O | function | pin name | I/O | function | pin name | I/O | function |
| 37 | P54/ EXI54 | I/O | Hi-Z output | Input-Output port/ External interrupt | SDA1 | I/O | $I^2C$ data input/output | SOUTF0 | O | SSIOF data output | RXDF0 | I | UARTF data input |
| 38 | P55/ EXI55 | I/O | Hi-Z output | Input-Output port/ External interrupt | SCL1 | O | $I^2C$ clock output | SINF0 | I | SSIOF data input | TXDF0 | O | UARTF data output |
| 39 | P56/ EXI56/ TMCKI6 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | LSCLKO | O | Low-speed clock output | SCKF0 | I/O | SSIOF clock input/output | TMOUTE | O | FTM output |
| 40 | P57/ EXI57/ TMCKI7 | I/O | Hi-Z output | Input-Output port/ External interrupt/ Timer clock input | OUTCLK | O | High-speed clock output | SSF0 | I/O | SSIOF select input/output | TMOUTF | O | FTM output |

## PIN DESCRIPTION

The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quartic function)

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|---|---|---|---|---|---|
| System | | | | | |
| RESET_N | I | Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected. | RESET_N | — | L |
| XT0 | I | Crystal connection pin for low-speed clock. Capacitors $C_{DL}$ and $C_{GL}$ are connected across this pin and $V_{SS}$ as required. | PXT0 | 1st | — |
| XT1 | O | | PXT1 | 1st | — |
| LSCLKI | I | External clock input for Low-speed clock. | PXT1 | 1st | — |
| OSC0 | I | Crystal/ceramic connection pin for high-speed clock (16 MHz max.). Capacitors $C_{DH}$ and $C_{GH}$ are connected across this pin and $V_{ss}$. | P10 | 1st | — |
| OSC1 | O | | P11 | 1st | — |
| CLKIN | I | External clock input for High-speed clock. | P11 | 1st | — |
| LSCLKO | O | Low-speed clock output pin. | P46,P56 | 2nd | — |
| OUTCLK | O | High-speed clock output pin. | P47,P57 | 2nd | — |
| General-purpose input/output port | | | | | |
| PXT0-PXT1 | I | General-purpose input port(without pull-up/pull-down resister). | PXT0-PXT1 | 1st | — |
| P00-P05 | I/O | General-purpose input/output port. | P00-P05 | 1st | — |
| P10-P11 | I/O | General-purpose input/output port. | P10-P11 | 1st | — |
| P20-P23 | I/O | General-purpose input/output port. | P20-P23 | 1st | — |
| P30-P37 | I/O | General-purpose input/output port. | P30-P37 | 1st | — |
| P40-P47 | I/O | General-purpose input/output port. | P40-P47 | 1st | — |
| P50-P57 | I/O | General-purpose input/output port. | P50-P57 | 1st | — |
| External interrupt | | | | | |
| EXII0-EXII1<br>EXI00-05<br>EXI20-23<br>EXI30-37<br>EXI40-47<br>EXI50-57 | I | External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. | PXT0-PXT1<br>P00-P05<br>P20-P23<br>P30-P37<br>P40-P47<br>P50-P57 | 1st | H/L |
| LED | | | | | |
| LED | O | N-channel open drain output pins to drive LED. | P40,P41,P52,P53 | 1st | — |
| Melody/Buzzer | | | | | |
| MD0 | — | Melody/buzzer signal output pin. | P33,P43,P53 | 2nd | H |
| UART | | | | | |
| TXD0 | O | UART0 data output pin. | P01,P31,P41,P51 | 4th | — |
| RXD0 | I | UART0 data input pin. | P00,P30,P40,P50 | 4th | — |
| TXDF0 | O | UART with FIFO data output pin. | P21,P35,P45,P55 | 4th | — |
| RXDF0 | I | UART with FIFO data input pin. | P20,P34,P44,P54 | 4th | — |

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|---|---|---|---|---|---|
| $I^2C$ bus interface | | | | | |
| SDA0 | I/O | $I^2C$0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the $I^2C$, externally connect a pull-up resistor. | P30,P40,P50 | 2nd | — |
| SCL0 | O | $I^2C$0 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the $I^2C$, externally connect a pull-up resistor. | P31,P41,P51 | 2nd | — |
| SDA1 | I/O | $I^2C$1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the $I^2C$, externally connect a pull-up resistor. | P34,P44,P54 | 2nd | — |
| SCL1 | O | $I^2C$1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the $I^2C$, externally connect a pull-up resistor. | P35,P45,P55 | 2nd | — |
| Synchronous serial | | | | | |
| SCK0 | I/O | Synchronous serial(SSIO) clock input/output pin. | P02,P32,P42,P52 | 3rd | — |
| SIN0 | I | Synchronous serial(SSIO) data input pin. | P01,P31,P41,P51 | 3rd | — |
| SOUT0 | O | Synchronous serial(SSIO) data output pin. | P00,P30,P40,P50 | 3rd | — |
| SCKF0 | I/O | Synchronous serial with FIFO(SSIOF) clock input/output pin. | P22,P36,P46,P56 | 3rd | — |
| SINF0 | I | Synchronous serial with FIFO(SSIOF) data input pin. | P21,P35,P45,P55 | 3rd | — |
| SOUTF0 | O | Synchronous serial with FIFO(SSIOF) data output pin. | P20,P34,P44,P54 | 3rd | — |
| SSF0 | I/O | Synchronous serial with FIFO(SSIOF) select input/output pin. | P23,P37,P47,P57 | 3rd | L |
| FTM | | | | | |
| TMOUT0-9<br>TMOUTA-F | O | FTM output pin. | P02,P03,P22,P23<br>P32,P33,P36,P37,<br>P42,P43,P46,P47<br>P52,P53,P56,P57 | 4th | — |
| TMCKI0-7 | I | External clock input pin for FTM | P42,P43,P46,P47,<br>P52,P53,P56,P57 | 1st | — |
| RC oscillation type A/D converter | | | | | |
| IN0 | I | Channel 0 oscillation input pin. | P00 | 2nd | — |
| CS0 | O | Channel 0 reference capacitor connection pin. | P01 | 2nd | — |
| RS0 | O | Reference resistor connection pin of Channel 0. | P03 | 2nd | — |
| RT0 | O | Resistor sensor connection pin of Channel 0 for measurement. | P04 | 2nd | — |
| RCT0 | O | Resistor/capacitor sensor connection pin of Channel 0 for measurement. | P02 | 2nd | — |
| RCM | O | RC oscillation monitor pin. | P05 | 2nd | — |
| IN1 | I | Oscillation input pin of Channel 1. | P20 | 2nd | — |
| CS1 | O | Reference capacitor connection pin of Channel 1. | P21 | 2nd | — |
| RS1 | O | Reference resistor connection pin of Channel 1. | P22 | 2nd | — |
| RT1 | O | Resistor sensor connection pin for measurement of Channel 1. | P23 | 2nd | — |

| Pin name | I/O | Description | LSI pin name | Pin mode | Logic |
|---|---|---|---|---|---|
| Successive approximation type A/D converter | | | | | |
| $V_{REF}$ | I | Reference voltage input pin for successive approximation type A/D converter. | $V_{REF}$ | — | — |
| AIN0-11 | I | Channel 0 analog input for successive approximation type A/D converter. | P34,P35,P36,P37, P20,P21,P22,P23, P00,P01,P02,P03 | 1st | — |
| Analog comparator | | | | | |
| CMP0P | I | Comparator0 Non-inverted input pin. | P30 | 1st | — |
| CMP0M | I | Comparator0 Inverted input pin. | P31 | 1st | — |
| CMP1P | I | Comparator1 Non-inverted input pin. | P32 | 1st | — |
| CMP1M | I | Comparator1 Inverted input pin. | P33 | 1st | — |
| For testing | | | | | |
| TEST0 | I/O | Input/output pin for testing. A pull-down resistor is internally connected. | TEST0 | — | — |
| TEST1_N | I | Input pin for testing. A pull-up resistor is internally connected. | TEST1_N | — | — |
| Power supply | | | | | |
| $V_{SS}$ | — | Negative power supply pin. | $V_{SS}$ | — | — |
| $V_{DD}$ | — | Positive power supply pin. | $V_{DD}$ | — | — |
| $V_{DDL}$ | — | Positive power supply pin (internally generated) for internal logic. Capacitors $C_{L0}$ and $C_{L1}$ are connected between this pin and $V_{SS}$. | $V_{DDL}$ | — | — |
| $V_{DDX}$ | — | Positive power supply pin (internally generated) for low-speed oscillation. Capacitor $C_{X1}$ is connected between this pin and $V_{SS}$. | $V_{DDX}$ | — | — |

## TERMINATION OF UNUSED PINS

Table 1 shows methods of terminating the unused pins.

**Table 1 Termination of Unused Pins**

| Pin | Recommended pin termination |
|---|---|
| RESET_N | Connect to $V_{DD}$ |
| TEST0 | open |
| TEST1_N | Connect to $V_{DD}$ |
| $V_{REF}$ | Connect to $V_{DD}$ |
| P00 to P05 | open |
| PXT0 to PXT1 | open |
| P10 to P11 | open |
| P20 to P23 | open |
| P30 to P37 | open |
| P40 to P47 | open |
| P50 to P57 | open |

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

## ELECTRIC CHARACTERISTICS

### Absolute Maximum Ratings

($V_{SS}$=0V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage 1 | $V_{DD}$ | Ta=25°C | -0.3 to +6.0 | V |
| Power supply voltage 2 | $V_{DDL}$ | Ta=25°C | -0.3 to +2.0 | V |
| Power supply voltage 3 | $V_{DDX}$ | Ta=25°C | -0.3 to +2.0 | V |
| Input voltage | $V_{IN}$ | Ta=25°C | -0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_{OUT}$ | Ta=25°C | -0.3 to $V_{DD}$+0.3 | V |
| Output current 1 | $I_{OUT1}$ | Port 0 to 2 Ta=25°C | -12 to +11 | mA |
| Output current 2 | $I_{OUT2}$ | Port 3 to 5 Ta=25°C | -12 to +20 | mA |
| Power dissipation | PD | Ta=25°C | 0.9 | W |
| Storage temperature | $T_{STG}$ | — | -55 to +150 | °C |

**Recommended Operating Conditions**

($V_{SS}$=0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating temperature (Ambience) | $T_{OP}$ | — | -40 to +85 | °C |
| Operating voltage | $V_{DD}$ | — | 1.8 to 5.5 | V |
| Reference voltage | $V_{REF}$ | — | 1.8 to $V_{DD}$ | V |
| Operating frequency （CPU） | $f_{OP}$ | — | 30k to 16.8M | Hz |
| Low-speed external clock input | $f_{EXTL}$ | — | 30k to 36k | Hz |
| High-speed external clock input | $f_{EXTH}$ | — | 2M to 16M | Hz |
| Low speed crystal oscillation frequency | $f_{XTL}$ | — | 32.768k | Hz |
| Low speed crystal oscillation external capacitor 1 | $C_{DL}$ | Using VT-200-FL(from SII） | 6.8 to 12 | pF |
| | $C_{GL}$ | | 6.8 to 12 | |
| Low speed crystal oscillation external capacitor 2 | $C_{DL}$ | Using DT-26(from Daishinku) | 12 to 16 | pF |
| | $C_{GL}$ | | 12 to 16 | |
| Low speed crystal *1 oscillation external capacitor 3 | $C_{DL}$ | Using VT-200-F(from SII） | 12 to 22 | pF |
| | $C_{GL}$ | | 12 to 22 | |
| High speed Crystal/ Ceramic oscillation frequency | $f_{XTH}$ | — | 16M | Hz |
| High speed crystal oscillation external capacitor | $C_{DH}$ | Using NX8045GB (from Nihon Denpa Kogyo) | 12 to 20 | pF |
| | $C_{GH}$ | | 12 to 20 | |
| Ceramic oscillation External capacitor | $C_{DH}$ | Using FCSTCE16M0V53 (from Murata manufacturing) Build in CL type | 0 to 5 | pF |
| | $C_{GH}$ | | 0 to 5 | |
| $V_{DDL}$ external capacitor *2 | $C_L$ | ESR ≦ 500mΩ | 2.2 ± 30% | μF |
| $V_{DDX}$ external capacitor | $C_X$ | — | 0.33 ± 30% | μF |

*1：Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal. Please evaluate the matching when other crystal oscillator/ ceramic oscillator is used.

*2：Please evaluate on user's conditions, put on $C_{L0}$( = 0.1uF) if necessary.

See the application note; "Precautions for MCU board design" for details, when designing MCU board.

**Operating Conditions of Flash Memory**

($V_{SS}$= 0V)

| Parameter | Symbol | Condition | | Range | Unit |
|---|---|---|---|---|---|
| Operating temperature (Ambience) | $T_{OP}$ | Data area : write/erase | | -40 to +85 | °C |
| | | Program area : write/erase | | 0 to +40 | °C |
| Operating voltage Write time | $V_{DD}$ | Write/erase | | 1.8 to 5.5 | V |
| | $C_{EPD}$ | Data area (1,024B x 2) | | 10,000 | times |
| | $C_{EPP}$ | Program area | | 100 | times |
| Erase unit | — | Block erase | Program area | 8 | KB |
| | | | Data area | 2 | |
| | | Sector erase | | 1 | KB |
| Erase time(Maximum) | — | Block erase/Sector erase | | 100 | ms |
| Write unit | — | — | | 1 word (2 byte) | — |

**AC characteristics (Oscillation)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C , unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Low speed crystal oscillation start time | $T_{XTL}$ | — | — | — | 2 | s | 1 |
| High speed crystal oscillation start time | $T_{XTH}$ | — | — | — | 20 | ms | |
| Low speed built-in RC oscillation frequency*1*2 | $f_{LCR}$ | Ta=25°C | typ -1.5% | 32.768 | typ +1.5% | kHz | |
| | | Ta=-40 ~ 85°C | typ -5% | 32.768 | typ +5% | | |
| High speed build-in RC oscillation frequency*1*2 | $f_{HCR}$ | Ta=25°C | typ -1% | 16 | typ +1% | MHz | |
| | | Ta=-40 to 85°C | typ -5% | 16 | typ +5% | | |

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.

**DC Characteristics (IDD)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. (3.0V) | Rating Max. (3.6V) | Rating Max. (5.5V) | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|---|
| Power consumption 1 | IDD1 | CPU is Stopped<br>Low/High-speed oscillation is stopped | Ta=25°C | – | 0.25 | 0.8 | 1.3 | µA | 1 |
| | | | Ta=-40 to 85°C | – | – | 15 | 18 | | |
| Power consumption 2 | IDD2 | DEEP-HALT mode *2*4<br>(LBTC function)<br>Low-speed crystal oscillating (32.768kHz)<br>High-speed oscillation is stopped. | Ta=25°C | – | 0.45 | 1.3 | 1.6 | µA | |
| | | | Ta=-40 to 85°C | – | – | 15 | 18 | | |
| Power consumption 3 | IDD3 | HALT mode *2*4<br>(LTBC function)<br>Low-speed crystal oscillating (32.768kHz)<br>High speed oscillation is stopped. | Ta=25°C | – | 2 | 2.7 | 3.0 | µA | |
| | | | Ta=-40 to 85°C | – | – | 18 | 19 | | |
| Power consumption 4 | IDD4 | CPU Low-speed *1*4<br>Low-speed built-in CR oscillating<br>High speed oscillation is stopped. | Ta=25°C | – | 10 | 12 | 13 | µA | |
| | | | Ta=-40 to 85°C | – | – | 25 | 28 | | |
| Power consumption 5 | IDD5 | CPU High-speed(16MHz) *1*4<br>High-speed Built-in CR oscillating | Ta=25°C | – | 4 | 5.5 | 5.5 | mA | |
| | | | Ta=-40 to 85°C | – | – | 6 | 6 | | |
| Power consumption 6 | IDD6 | CPU High-speed(16MHz) *1*3*4<br>High speed crystal oscillating (16MHz) | Ta=25°C | – | 6 | 7.5 | 9.4 | mA | |
| | | | Ta=-40 to 85°C | – | – | 8 | 9.9 | | |

*1 : at CPU activity rate =100% （No HALT state）

*2 : using 32.768KHz crystal oscillator VT-200-FL (from SII)($C_{GL}$/$C_{DL}$＝12pF)
using 32.768KHz crystal oscillator DT-26(from Daishinku)($C_{GL}$/$C_{DL}$＝12pF）

*3 : using NX8045GB(from Nihon denpa kogyo) ($C_{GH}$/$C_{DH}$＝16pF)

*4 : BLKCON0~BLKCON5 valid bits are all “1”.

### DC Characteristics (VLS)

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating *1 | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| VLS judge voltage ($V_{DD}$=fall) | $V_{VLS}$ | vlscon = 3H | 1.798 | 1.898 | 1.998 | V | 1 |
| | | vlscon = 4H | 1.900 | 2.000 | 2.100 | | |
| | | vlscon = 5H | 1.993 | 2.093 | 2.193 | | |
| | | vlscon = 6H | 2.096 | 2.196 | 2.296 | | |
| | | vlscon = 7H | 2.209 | 2.309 | 2.409 | | |
| | | vlscon = 8H | 2.309 | 2.409 | 2.509 | | |
| | | vlscon = 9H | 2.505 | 2.605 | 2.705 | | |
| | | vlscon = AH | 2.700 | 2.800 | 2.900 | | |
| | | vlscon = BH | 2.968 | 3.068 | 3.168 | | |
| | | vlscon = CH | 3.294 | 3.394 | 3.494 | | |
| | | vlscon = DH | 3.697 | 3.797 | 3.897 | | |
| | | vlscon = EH | 4.126 | 4.226 | 4.326 | | |
| | | vlscon = FH | 4.567 | 4.667 | 4.767 | | |
| $V_{VLS}$ Hysteresis width ($V_{DD}$=rise) | $H_{VLS}$ | – | $V_{VLS}$ x 1.8% | $V_{VLS}$ x 3.8% | $V_{VLS}$ x 6.3% | V | |

### DC characteristics (LLD)

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| LLD judge Voltage | VLLR | — | 1.60 | 1.80 | 2.00 | V | 1 |

### DC characteristics (Analog comparator)

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Common input voltage range | $V_{CMPIN}$ | — | 0.2 | — | $V_{DD}$ -0.2 | V | 1 |
| Input offset voltage | $V_{CMPOF}$ | — | -30 | — | 30 | mV | |
| Comparator judge time | $T_{CMP}$ | CMPP- CMPM =40mV | — | — | 2 | µs | |

**DC characteristics (VOHL, IOHL)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Output voltage 1 ( P00-P05, P10-P11 P20-P23, P30-P37 P40-P47, P50-P57) | VOH1 | 3.6V < $V_{DD}$ ≤ 5.5V IOH=-2.5mA | $V_{DD}$ -0.6 | – | – | V | 2 |
| | | 1.8V ≤ $V_{DD}$ ≤ 3.6V IOH=-1.0mA | $V_{DD}$ -0.5 | – | – | | |
| | VOL1 | 3.6V < $V_{DD}$ ≤ 5.5V IOL=+5.0mA | – | – | 0.6 | | |
| | | 1.8V ≤ $V_{DD}$ ≤ 3.6V IOL=+0.5mA | – | – | 0.4 | | |
| Output voltage 2 (P40,P41, P52, P53) (LED mode is selected) | VOL2 | 3.6V < $V_{DD}$ ≤ 5.5V IOL=+5.0mA | – | – | 0.4 | | |
| | | 2.7V ≤ $V_{DD}$ ≤ 3.6V IOL=+5.0mA | – | – | 0.6 | | |
| | | 1.8V ≤ $V_{DD}$ < 2.7V IOL=+2.0mA | – | – | 0.4 | | |
| Output voltage 3 (P30,P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) ($I^2C$ mode is selected) | VOL3 | IOL3= +3mA ($I^2C$spec) ($V_{DD}$ ≥ 2V) | – | – | 0.4 | | |
| Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) ($I^2C$ mode is selected) | VOL4 | IOL3= +2mA($I^2C$spec) ($V_{DD}$ < 2V) | – | – | $V_{DD}$ ×0.2 | | |
| Output leak 1 (P00-P05,P20-P23, P30-P37, P40-P47, P50-P57) | IOOH1 | VOH=$V_{DD}$ (at high impedance) | – | – | +1 | μA | 3 |
| | IOOL1 | VOL=$V_{SS}$ (at high impedance) | -1 | – | – | | |
| Output leak 2 (P10-P11) | IOOH2 | VOH=$V_{DD}$ (at high impedance) | – | – | +2 | | |
| | IOOL2 | VOL=$V_{SS}$ (at high impedance) | -2 | – | – | | |

**DC characteristics (IIHL)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating*1 | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input current 1 (RESET_N, TEST1_N) | IIH1 | VIH1=$V_{DD}$ | — | — | 1 | μA | 4 |
| | IIL1 | VIL1=$V_{SS}$ | -900 | -300 | -20 | | |
| Input current 2 (TEST0) | IIH2 | VIH2=$V_{DD}$ | 20 | 300 | 900 | | |
| | IIL2 | VIL2=$V_{SS}$ | -1 | — | — | | |
| Input current 3 (PXT0-PXT1, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57) | IIH3 | VIH3=$V_{DD}$ (at pull down) | 1 | 15 | 200 | | |
| | IIL3 | VIL3=$V_{SS}$ (at pull up) | -200 | -15 | -1 | | |
| | IIH3Z | VIH3=$V_{DD}$ (at high impedance) | — | — | 1 | | |
| | IIL3Z | VIL3=$V_{SS}$ (at high impedance) | -1 | — | — | | |
| Input current 4 (P10-P11) | IIH4 | VIH4=$V_{DD}$ (at pull down) | 1 | 15 | 200 | | |
| | IIL4 | VIL4=$V_{SS}$ (at pull up) | -200 | -15 | -1 | | |
| | IIH4Z | VIH4=$V_{DD}$ (at high impedance) | — | — | 2 | | |
| | IIL4Z | VIL4=$V_{SS}$ (at high impedance) | -2 | — | — | | |

*1 : typ.rating is Ta=25°C , $V_{DD}$=3.0V

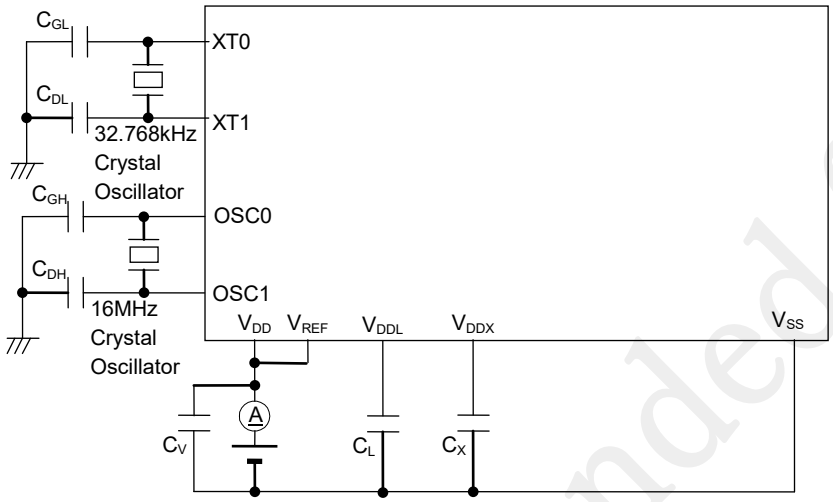
**DC characteristics (VIHL)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1 (RESET_N, TEST0, TEST1_N, PXT0-PXT1, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57) | VIH1 | — | 0.7 ×$V_{DD}$ | — | $V_{DD}$ | V | 5 |
| | VIL1 | — | 0 | — | 0.3 ×$V_{DD}$ | | |
| Input terminal capacitance (RESET_N, TEST0, TEST1_N, PXT0-PXT1,, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57) | CIN | f=10kHz $V_{rms}$=50mV Ta=25°C | — | — | 10 | pF | — |

**Measuring circuit**

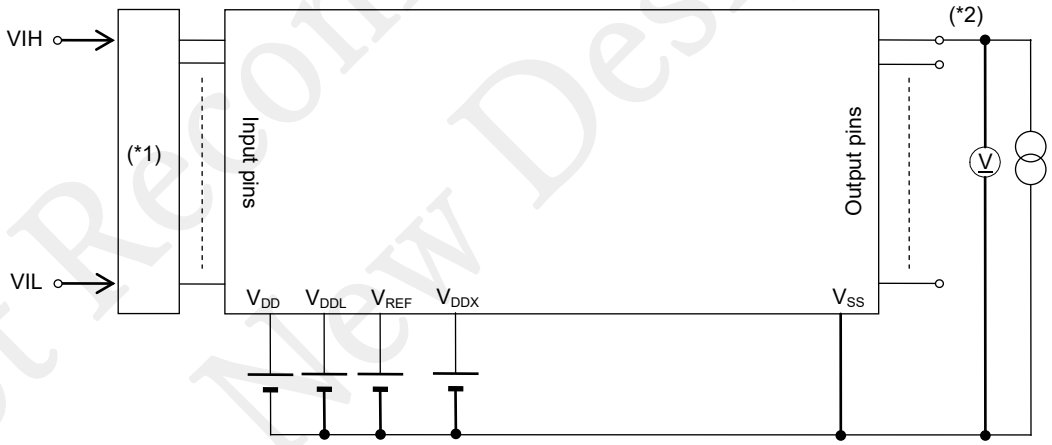
Measuring circuit 1




| | | |
|---|---|---|
| $C_V$ | : | 1.0μF |
| $C_L$ | : | 2.2μF |
| $C_X$ | : | 0.33μF |
| $C_{GL}$ | : | 12pF |
| $C_{DL}$ | : | 12pF |
| $C_{GH}$ | : | 16pF |
| $C_{DH}$ | : | 16pF |

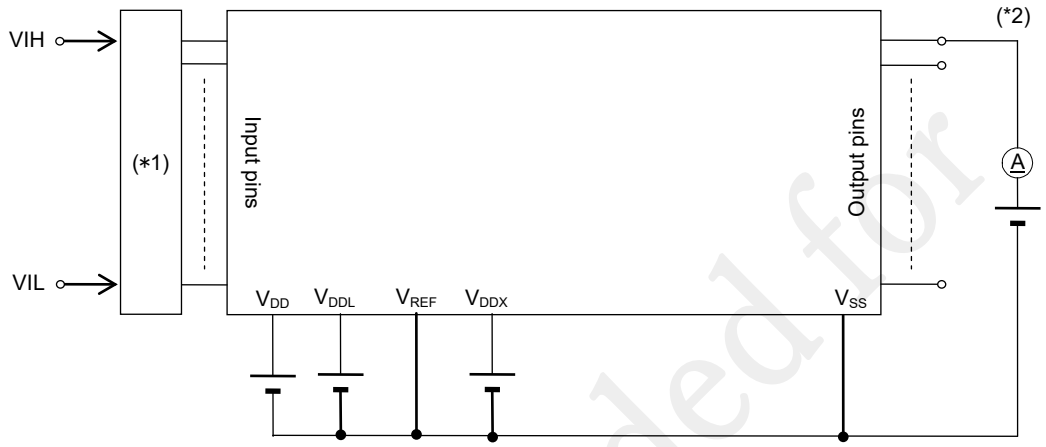
32.768kHz crystal oscillator : DT-26 (from Daishinku)
16MHz crystal oscillator : NX8045GB (from Nihon denpa kogyo)

Measuring circuit 2



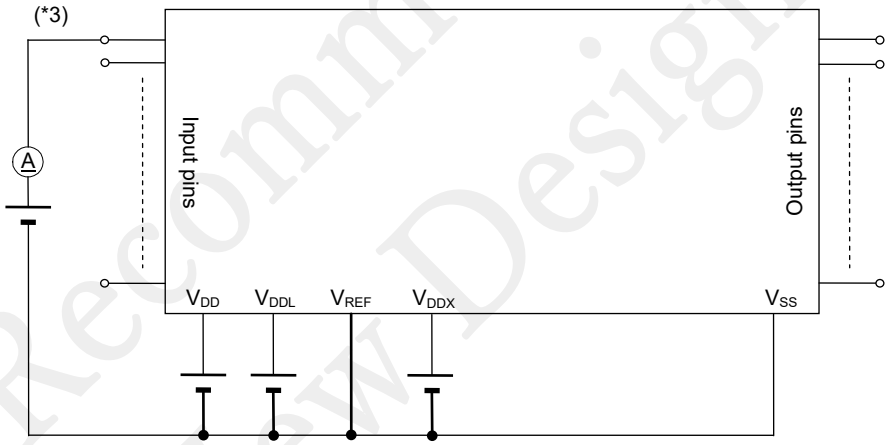

(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



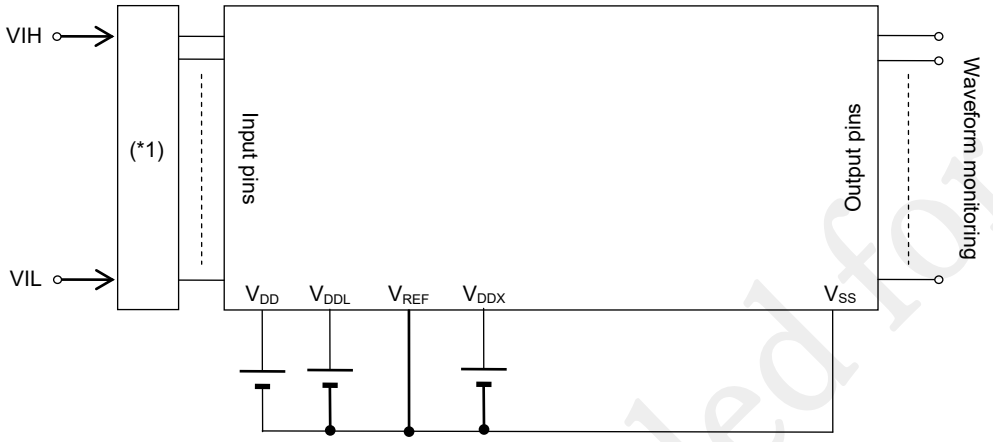

(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4




(*3) Measured at the specified output pins.

Measuring circuit 5

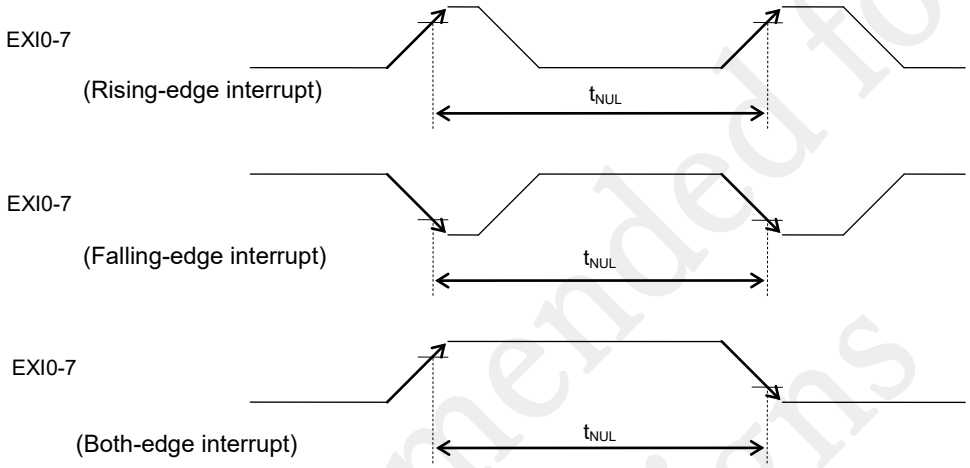



(*1) Input logic circuit to determine the specified measuring conditions.

**AC characteristics (external interrupt)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| External interrupt disable period | $t_{NUL}$ | Interruput enable (MIE=1)<br>CPU : NOP operation | 2.5 x sysclk | — | 3.5 x sysclk | φ |

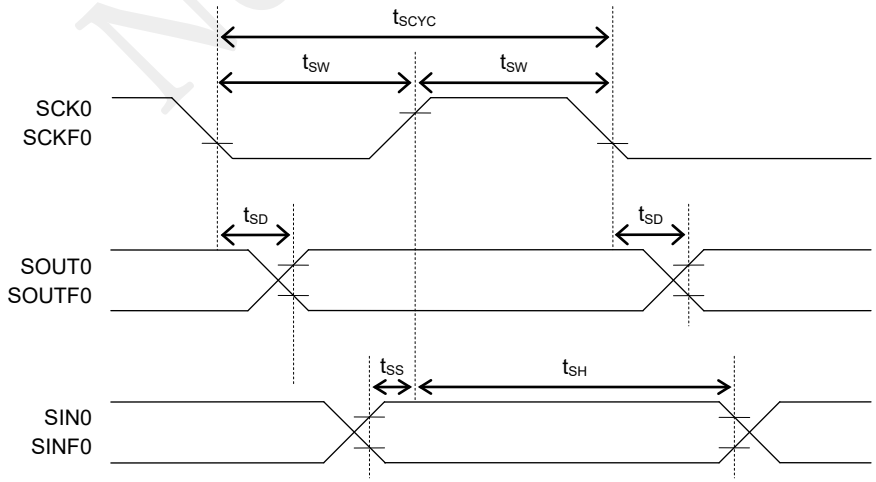


**AC characteristics (synchronous serial port)**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCK input cycle (slave mode) | $t_{SCYC}$ | High-speed oscillation is not active | 10 | — | — | µs |
| | | High speed oscillation is active | 500 | — | — | ns |
| SCK output cycle (master mode) | $t_{SCYC}$ | — | — | SCK*1 | — | s |
| SCK input pulse width (slave mode) | $t_{SW}$ | High-speed oscillation is not active | 4 | — | — | µs |
| | | High speed oscillation is active | 200 | — | — | ns |
| SCK output pulse width (master mode) | $t_{SW}$ | — | $t_{SCYC}$ ×0.4 | $t_{SCYC}$ ×0.5 | $t_{SCYC}$ ×0.6 | s |
| SOUT output delay time (slave mode) | $t_{SD}$ | — | — | — | 180 | ns |
| SOUT output delay time (master mode) | $t_{SD}$ | — | — | — | 80 | ns |
| SIN input Setup time (slave mode) | $t_{SS}$ | — | 50 | — | — | ns |
| SINinput Hold time | $t_{SH}$ | — | 50 | — | — | ns |

*1 : The clock period which is selected by the below registers(min:250ns@reguraly, min:500ns@P02, P22 is used)
In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



**AC characteristics（I²C Bus interface : Standard mode 100kHz）**

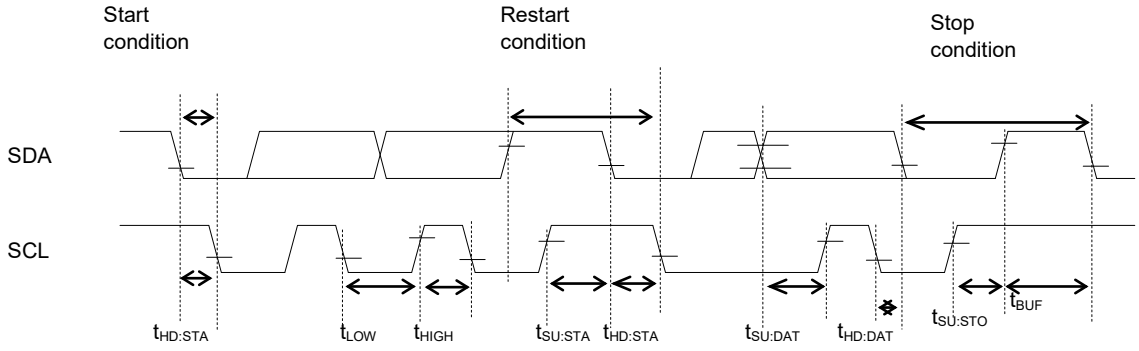
($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | $f_{SCL}$ | — | 0 | — | 100 | kHz |
| SCL hold time (Start/restart condition) | $t_{HD:STA}$ | — | 4.0 | — | — | µs |
| SCL"L" level time | $t_{LOW}$ | — | 4.7 | — | — | µs |
| SCL"H" level time | $t_{HIGH}$ | — | 4.0 | — | — | µs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 4.7 | — | — | µs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | 3.45 | µs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.25 | — | — | µs |
| SCL setup time (stop condition) | $t_{SU:STO}$ | — | 4.0 | — | — | µs |
| Bus-free time | $t_{BUF}$ | — | 4.7 | — | — | µs |

**AC characteristics（I²C bus interface : fast mode 400kHz）**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rateing | | | unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | $f_{SCL}$ | — | 0 | — | 400 | kHz |
| SCLhold time (start/restart condition) | $t_{HD:STA}$ | — | 0.6 | — | — | µs |
| SCL"L" level time | $t_{LOW}$ | — | 1.3 | — | — | µs |
| SCL"H" level time | $t_{HIGH}$ | — | 0.6 | — | — | µs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 0.6 | — | — | µs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | 0.9 | µs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | µs |
| SCLsetup time (stop condition) | $t_{SU:STO}$ | — | 0.6 | — | — | µs |
| Bus-free time | $t_{BUF}$ | — | 1.3 | — | — | µs |



**AC characteristics（RC Oscillation A/D Converter）**

($V_{DD}$=1.8~5.5V, $V_{SS}$=0V, Ta=-40~+85°C, unless otherwise specified)

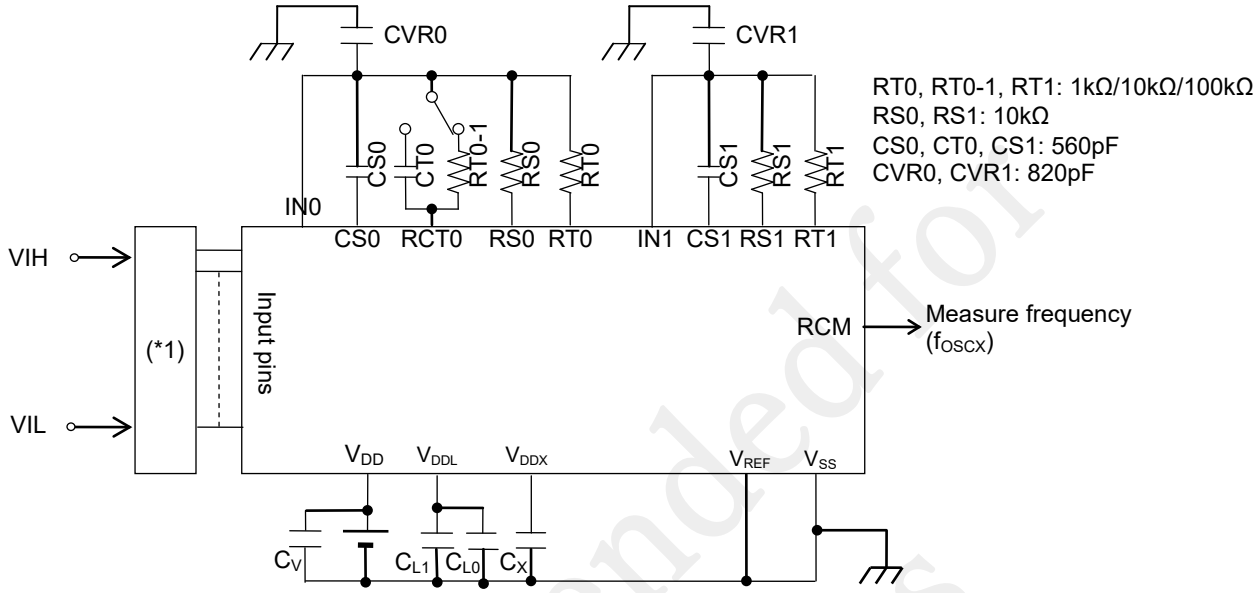
| Parameter | Symbol | Condition | Rating | | | unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Resister for oscillation | RS0,RS1,RT0,RT0-1,RT1 | – | 1 | – | 400 | kΩ |
| Oscillation frequency $V_{DD}$ = 3.0V CVR=820pF CS=560pF RAMD0=0 | $f_{OSC1\_0}$ | Resister for oscillation =1kΩ | – | 528 | – | kHz |
| | $f_{OSC2\_0}$ | Resister for oscillation =10kΩ | – | 59 | – | kHz |
| | $f_{OSC3\_0}$ | Resister for oscillation =100kΩ | – | 5.9 | – | kHz |
| RS to RT oscillation frequency ratio *1 $V_{DD}$ = 3.0V CVR=820pF CS=560pF RAMD0=0 | Kf1_0 | RT0, RT0-1, RT1=1kΩ | 8.225 | 8.94 | 9.655 | – |
| | Kf2_0 | RT0, RT0-1, RT1=10kΩ | 0.99 | 1 | 1.01 | – |
| | Kf3_0 | RT0, RT0-1, RT1=100kΩ | 0.093 | 0.101 | 0.109 | – |
| Oscillation frequency $V_{DD}$ = 5.0V CVR=820pF CS=560pF RAMD0=1 | $f_{OSC1\_0}$ | Resister for oscillation =1kΩ | – | 528 | – | kHz |
| | $f_{OSC2\_0}$ | Resister for oscillation =10kΩ | – | 59 | – | kHz |
| | $f_{OSC3\_0}$ | Resister for oscillation =100kΩ | – | 5.9 | – | kHz |
| RS to RT oscillation frequency ratio *1 $V_{DD}$ = 5.0V CVR=820pF CS=560pF RAMD0=1 | Kf1_0 | RT0, RT0-1, RT1=1kΩ | 8.225 | 8.94 | 9.655 | – |
| | Kf2_0 | RT0, RT0-1, RT1=10kΩ | 0.99 | 1 | 1.01 | – |
| | Kf3_0 | RT0, RT0-1, RT1=100kΩ | 0.093 | 0.101 | 0.109 | – |

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT0-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})} \quad (x = 1, 2, 3)$$

$$\frac{f_{OSCx}(\text{RT0-1-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})}, \quad \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})}$$

Measuring circuit




(*1) Input logic circuit to determine the specified measuring conditions.

【Note】

・Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

・When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by $V_{SS}$(GND) .

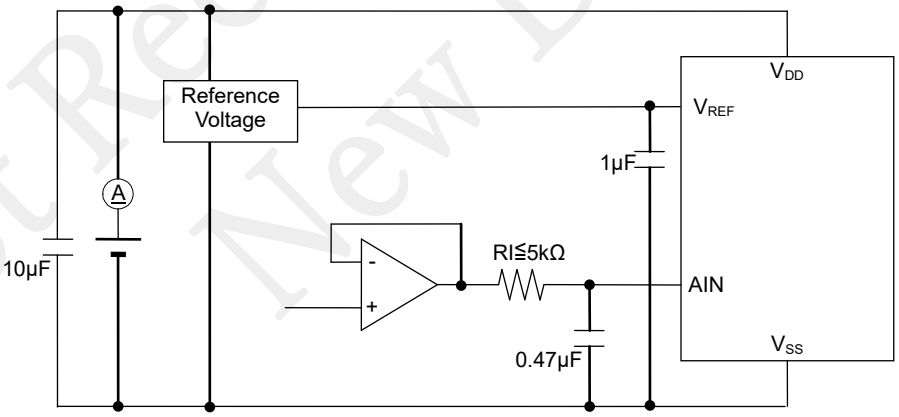
・Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

**Electrical Characteristics of Successive Approximation Type A/D Converter**

($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Resolution | n | — | — | 12 | — | bit |
| Integral non-linearity error | INL | 2.7V ≦ $V_{REF}$ ≦ 5.5V | -4 | — | +4 | LSB |
| | | 2.2V ≦ $V_{REF}$ < 2.7V | -6 | — | +6 | |
| | | 1.8V ≦ $V_{REF}$ < 2.2V (using Low-speed clock) | -10 | — | +10 | |
| Differential non-linearity error | DNL | 2.7V ≦ $V_{REF}$ ≦ 5.5V | -3 | — | +3 | |
| | | 2.2V ≦ $V_{REF}$ < 2.7V | -5 | — | +5 | |
| | | 1.8V ≦ $V_{REF}$ < 2.2V (using Low-speed clock) | -9 | — | +9 | |
| Zero-scale error | $V_{OFF}$ | 2.2V ≦ $V_{REF}$ ≦ 5.5V | -6 | — | +6 | |
| | | 1.8V ≦ $V_{REF}$ < 2.2V (using Low-speed clock) | -10 | — | +10 | |
| Full-scale error | FSE | 2.2V ≦ $V_{REF}$ ≦ 5.5V | -6 | — | +6 | |
| | | 1.8V ≦ $V_{REF}$ < 2.2V (using Low-speed clock) | -10 | — | +10 | |
| Input impidance | RI | — | — | — | 5k | Ω |
| Reference voltage | $V_{REF}$ | — | 1.8 | — | $V_{DD}$ | V |
| Conversion time | $t_{CONV}$ | Using High-speed clock(max. 4MHz) | — | 170 | — | clk |
| | | Using Low-speed clock | — | 16 | — | |

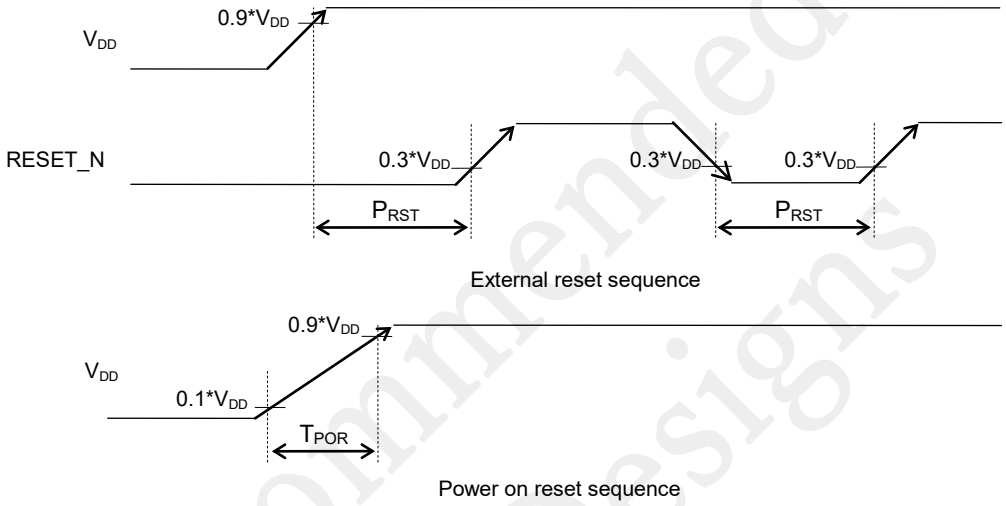
Measuring circuit



**Reset characteristics**

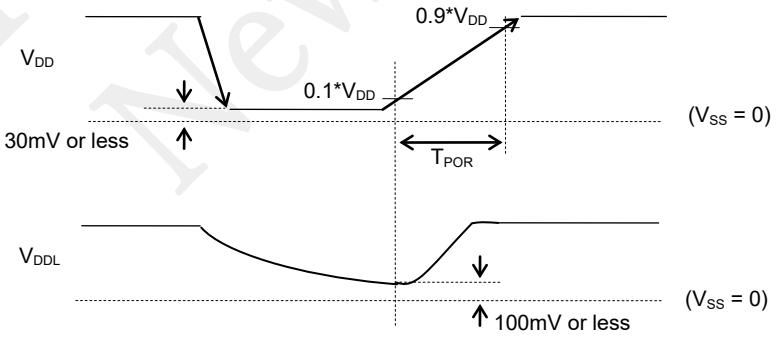
($V_{DD}$=1.8 to 5.5V, $V_{SS}$=0V, Ta=-40 to +85°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Reset pulse width | $P_{RST}$ | – | 200 | – | – | μs | 1 |
| Reset noise elimination pulse width | $P_{NRST}$ | – | – | – | 0.3 | μs | |
| Power-on reset activation power rise time | $T_{POR}$ | – | – | – | 10 | ms | |




**Power-on and shutdown Procedures**

In case of power-on or shutdown of $V_{DD}$, the procedures and constraints are shown as following.

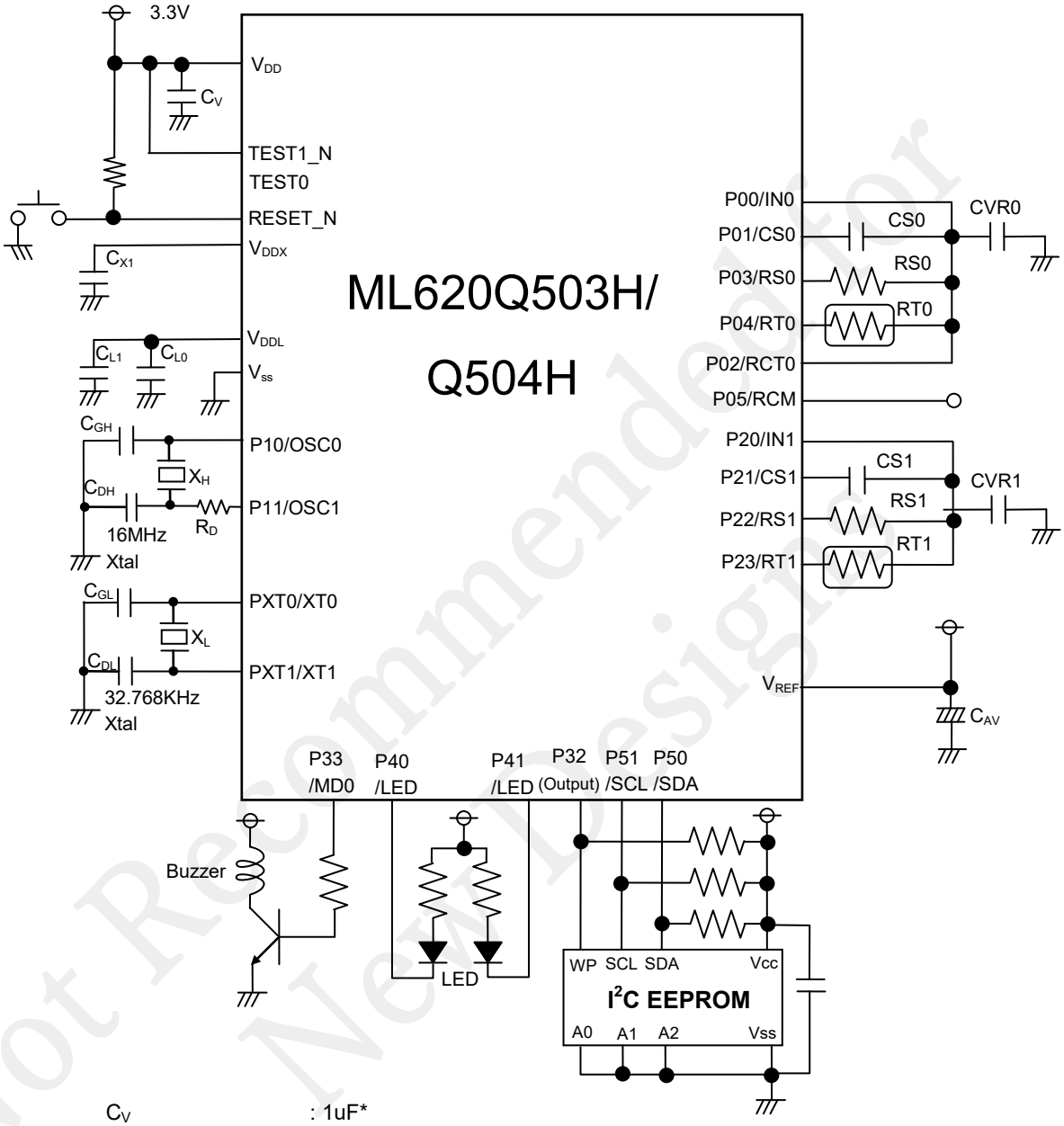



【Note】

・If $V_{DDL}$ level is 100mV or more over, reset the IC by RESET_N pin after power-on.

・$T_{POR}$ is the value when $V_{DD}$ slope is liner. If $V_{DD}$ slope is not liner in your system, use RESET_N or contact us.

## APPLICATION CIRCUIT EXAMPLE

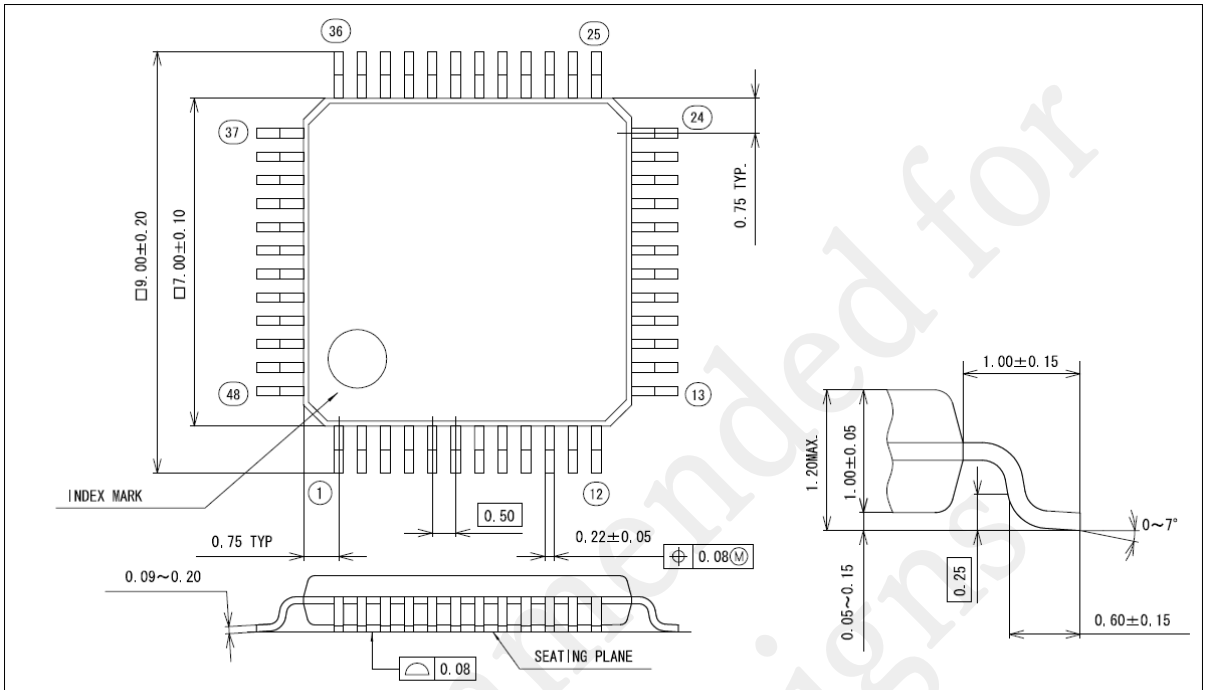



| | | | |
|---|---|---|---|
| $C_V$ | : 1uF* | | |
| $C_{L1}$ | : 2.2uF | $C_{L0}$ | : open* |
| $C_{X1}$ | : 0.33uF | | |
| $C_{GL}$ | : 12~16pF* | $C_{DL}$ | : 12~16pF* |
| $C_{GH}$ | : 12~20pF* | $C_{DH}$ | : 12~20pF* |
| $R_D$ | : 0Ω* | | |
| $C_{AV}$ | : 1uF* | RS0, RS1 | : 10 KΩ |
| CS0, CS1 | : 560 pF | CVR0, CVR1 | : 820 pF |
| RT0, RT1 | : Thermistor (103AT/Semitec) | | |
| $X_H$ | : NX8045GB/16.000MHz, Nihon Denpa Kogyo | | |
| $X_L$ | : DT-26, Daishinku | | |

*: Make a decision the parameters after evaluating on an user's conditions when designing circuits for mass production.

## PACKAGE DIMENSIONS

### ML620Q503H/Q504H Package Dimensions




NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

| LAPIS Semiconductor Co.,Ltd. | | | |
|---|---|---|---|
| PACKAGE CODE | P-TQFP48-0707-0.50-ZK6 | | |
| PACKAGE MATERIAL | EPOXY RESIN | UNIT | mm |
| LEAD FLAME MATERIAL | Cu ALLOY | DWG No. | QSL-69142 |
| LEAD FINISH | Sn 100% | REVISION | 3 |
| PLATING THICKNESS | MORE THAN 5μm | 1st ISSUE | Jul/28/2014 |
| PACKAGE MASS (g) | 0.13TYP | REVISED | Oct/14/2014 |

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions(reflow method, temperature and times).

## REVISION HISTORY

| Document No. | Date | Page | | Description |
|---|---|---|---|---|
| | | Previous Edition | Current Edition | |
| FEDL620Q504H-01 | Aug.31.2015 | – | – | Final Edition issued |
| FEDL620Q504H-02 | May.20.2020 | 4 | 4 | Updated shipment |
| | | 13,32 | 13,32 | Updated about RESET_N and TEST1_N pins |
| | | 15 | 15 | Added comment in recommended operating conditions. |
| | | 31 | 31 | Corrected “Power-on and shutdown Procedures” <published as errata> |
| | | 17,31 | 31 | Changed placement of reset characteristics.<br>Added note. |
| | | 33 | 33 | Updated package dimensions |

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