DDR SDRAM SODIMM

MT9VDDT1672H – 128MB[1]
MT9VDDT3272H – 256MB
MT9VDDT6472H – 512MB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2100, PC2700, or PC3200
- 128MB (16 Meg x 72), 256MB (32 Meg x 72), and 512MB (64 Meg x 72)
- Supports ECC error detection and correction
- $V_{DD} = V_{DDQ} = 2.5V$ (-40B: $V_{DD} = V_{DDQ} = 2.6V$)
- $V_{DDSPD} = 2.3–3.6V$
- 2.5V I/O (SSTL_2-compatible)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—that is, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Multiple internal device banks for concurrent operation
- Selectable burst lengths (BL) 2, 4, or 8
- Auto precharge option
- Auto refresh and self refresh modes: 15.625µs (128MB) and 7.8125µs (256MB, 512MB) maximum average periodic refresh interval
- Serial presence-detect (SPD) with EEPROM
- Selectable CAS latency (CL) for maximum compatibility
- Single rank
- Gold edge contacts

200-Pin SODIMM (MO-224) Figures

Figure 1: Low-Profile Layout

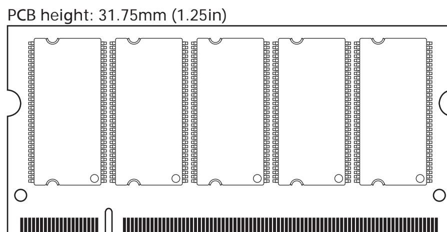
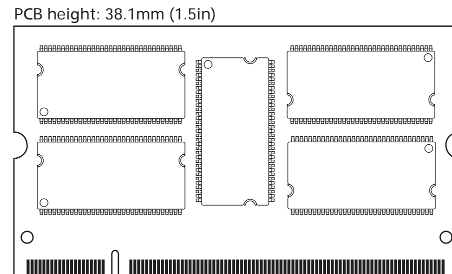


Figure 2: Standard Layout



Options / Marking

Options	Marking
• Operating temperature[2]	
– Commercial (0°C ≤ T_A ≤ +70°C)	None
– Industrial (–40°C ≤ T_A ≤ +85°C)	I
• Package	
– 200-pin DIMM (standard)	G
– 200-pin DIMM (Pb-free)	Y
• Memory clock, speed, CAS latency	
– 5.0ns (200 MHz), 400 MT/s, CL = 3.0	-40B
– 6.0ns (167 MHz), 333 MT/s, CL = 2.5	-335
– 7.5ns (133 MHz), 266 MT/s, CL = 2.0[3]	-262
– 7.5ns (133 MHz), 266 MT/s, CL = 2.0[3]	-26A
– 7.5ns (133 MHz), 266 MT/s, CL = 2.5[3]	-265

Notes: 1. End of life.
2. Contact Micron for industrial temperature module offerings.
3. Not recommended for new designs.

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Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^tRCD (ns)	^tRP (ns)	^tRC (ns)	Notes
		CL = 3	CL = 2.5	CL = 2				
-40B	PC3200	400	333	266	15	15	55	
-335	PC2700	–	333	266	18	18	60	1
-262	PC2100	–	266	266	15	15	60	
-26A	PC2100	–	266	266	20	20	65	
-265	PC2100	–	266	200	20	20	65	

Notes: 1. The values of ^tRCD and ^tRP for -335 modules show 18ns to align with industry specifications; actual DDR SDRAM device specifications are 15ns.

Table 2: Addressing

Parameter	128MB	256MB	512MB
Refresh count	4K	8K	8K
Row address	8K (A[11:0])	8K (A[12:0])	8K (A[12:0])
Device bank address	4 (BA[1:0])	4 (BA[1:0])	4 (BA[1:0])
Device configuration	128Mb (16 Meg x 8)	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)
Column address	1K (A[9:0])	1K (A[9:0])	2K (A[11, 9:0])
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 128MB Modules

Base device: MT46V16M8,[1] 128Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^tRCD-^tRP)
MT9VDDT1672HG-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-335__	128MB	16 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT1672HY-262__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT1672HG-26A__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT1672HG-265__	128MB	16 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Table 4: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT46V32M8,[1] 256Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^tRCD-^tRP)
MT9VDDT3272HG-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HY-40B__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT3272HG-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272H(I)Y-335__	256MB	32 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT3272HG-262__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-2-2
MT9VDDT3272HG-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3
MT9VDDT3272HY-265__	256MB	32 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

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Table 5: Part Numbers and Timing Parameters – 512MB Modules
Base device: MT46V64M8,[1] 512Mb DDR SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)
MT9VDDT6472HG-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HY-40B__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3
MT9VDDT6472HG-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472H(I)Y-335__	512MB	64 Meg x 72	2.7 GB/s	6.0ns/333 MT/s	2.5-3-3
MT9VDDT6472HG-26A__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2-3-3
MT9VDDT6472HG-265__	512MB	64 Meg x 72	2.1 GB/s	7.5ns/266 MT/s	2.5-3-3

Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT9VDDT6472HY-335J1.

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Pin Assignments and Descriptions

Table 6: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**	**Pin**	**Symbol**
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42	2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43	4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{DD}	6	DQ4	56	DQ28	106	A6	156	V_{DD}
7	DQ1	57	V_{DD}	107	A5	157	V_{DD}	8	DQ5	58	V_{DD}	108	A4	158	CK1#
9	V_{DD}	59	DQ25	109	A3	159	V_{SS}	10	V_{DD}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V_{SS}	12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{DD}	163	DQ48	14	DQ6	64	V_{SS}	114	V_{DD}	164	DQ52
15	V_{SS}	65	DQ26	115	A10	165	DQ49	16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{DD}	18	DQ7	68	DQ31	118	RAS#	168	V_{DD}
19	DQ8	69	V_{DD}	119	WE#	169	DQS6	20	DQ12	70	V_{DD}	120	CAS#	170	DM6
21	V_{DD}	71	CB0	121	S0#	171	DQ50	22	V_{DD}	72	CB4	122	NC	172	DQ54
23	DQ9	73	CB1	123	NC	173	V_{SS}	24	DQ13	74	CB5	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51	26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	DQS8	127	DQ32	177	DQ56	28	V_{SS}	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	V_{DD}	30	DQ14	80	CB6	130	DQ37	180	V_{DD}
31	DQ11	81	V_{DD}	131	V_{DD}	181	DQ57	32	DQ15	82	V_{DD}	132	V_{DD}	182	DQ61
33	V_{DD}	83	CB3	133	DQS4	183	DQS7	34	V_{DD}	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}	36	V_{DD}	86	NC	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58	38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	CK2	139	DQ35	189	DQ59	40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	CK2#	141	DQ40	191	V_{DD}	42	DQ20	92	V_{DD}	142	DQ44	192	V_{DD}
43	DQ17	93	V_{DD}	143	V_{DD}	193	SDA	44	DQ21	94	V_{DD}	144	V_{DD}	194	SA0
45	V_{DD}	95	NC	145	DQ41	195	SCL	46	V_{DD}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{DDSPD}	48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99[1]	NC/A12	149	V_{SS}	199	NC	50	DQ22	100	A11	150	V_{SS}	200	NC

Notes: 1. Pin 99 is NC for 128MB and A12 for 256MB and 512MB.

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Table 7: Pin Descriptions

Symbol	Type	Description
A[12:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective device bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[1:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA[1:0] define which mode register (or extended mode register) is loaded during the LOAD MODE REGISTER command. A[11:0] (128MB) and A[12:0] (256MB, 512MB).
BA[1:0]	Input	**Bank address:** BA[1:0] define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
CK[2:0], CK#[2:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
CKE0	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) the internal clock, input buffers, and output drivers.
DM[8:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#	Input	**Chip selects:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
CB[7:0]	I/O	Check bits.
DQ[63:0]	I/O	**Data input/output:** Data bus.
DQS[8:0]	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. Used to capture data.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}	Supply	**Power supply:** 2.5V ±0.2V (-40B: 2.6V ±0.1V).
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** 2.3–3.6V.
V_{REF}	Supply	SSTL_2 reference voltage (V_{DD}/2).
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

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Functional Block Diagrams

Figure 3: Functional Block Diagram – Low-Profile Layout

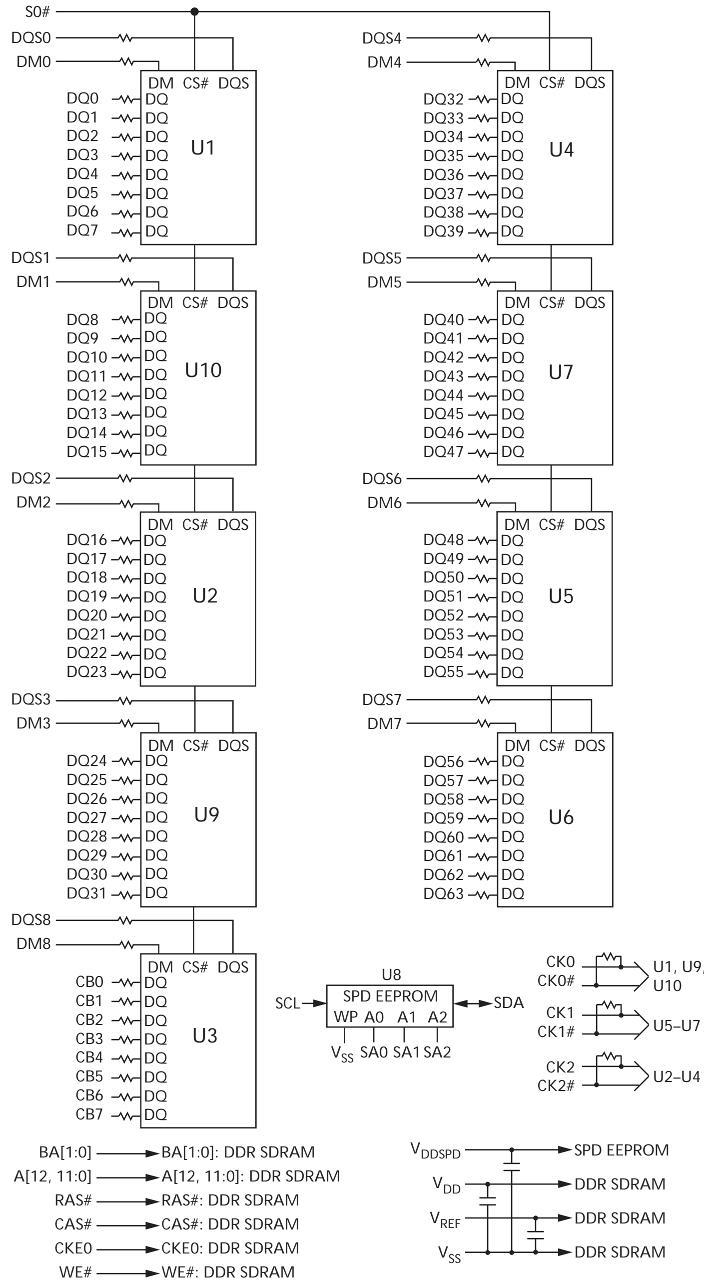

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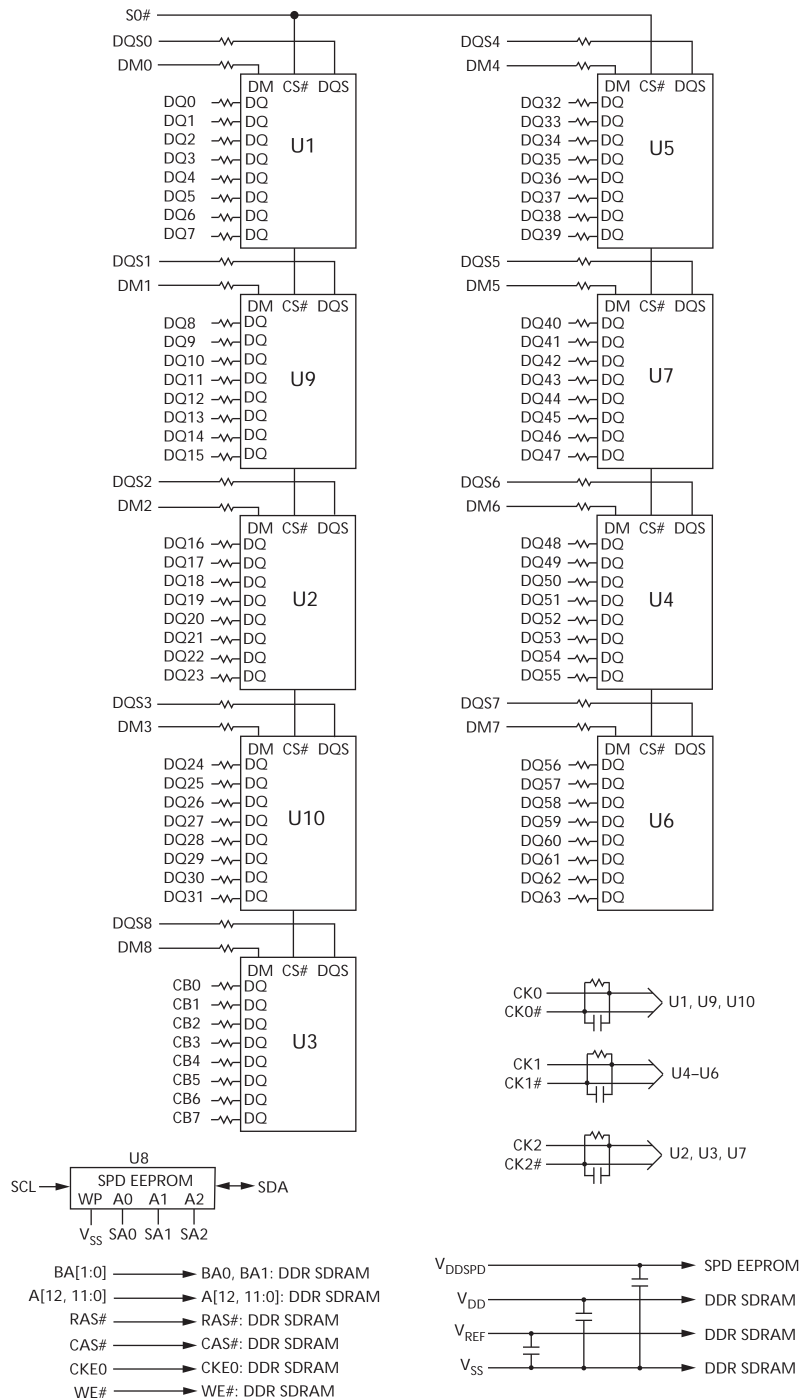
Figure 4: Functional Block Diagram – Standard Layout



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General Description

The MT9VDDT1672H, MT9VDDT3272H, and MT9VDDT6472H are high-speed, CMOS dynamic random access, 128MB, 256MB, and 512MB memory modules organized in a x72 configuration. These modules use DDR SDRAM devices with four internal banks.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR SDRAM modules incorporate serial presence-detect. The SPD function is implemented using a 2048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA[2:0], which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

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Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated on the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}		–1.0	3.6	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	3.2	V
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, BA, S#, CKE	–18	18	µA
		CK, CK#	–6	6	
		DM	–2	2	
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQ are disabled	DQ, DQS	–5	5	µA
T_A	DRAM ambient operating temperature[1]	Commercial	0	+70	°C
		Industrial	–40	+85	°C

Notes: 1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades
DDR components meet or exceed the listed module speed grades

Module Speed Grade	Component Speed Grade
-40B	-5
-335	-6
-262	-75E
-26A	-75Z
-265	-75

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I_{DD} Specifications

Table 10: I_{DD} Specifications and Conditions – 128MB (Die Revision D)

Values are shown for the MT46V16M8 DDR SDRAM only and are computed from values specified in the 128Mb (16 Meg x 8) component data sheet

Parameter/Condition		Symbol	-335	-262	-26A/ -265	Units
Operating one bank active-precharge current: $^tRC = {^tRC}$ (MIN); $^tCK = {^tCK}$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	1125	990	945	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {^tRC}$ (MIN); $^tCK = {^tCK}$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	1215	1080	1080	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {^tCK}$ (MIN); CKE = LOW		I_{DD2P}	27	27	27	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {^tCK}$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	405	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {^tCK}$ (MIN); CKE = LOW		I_{DD3P}	225	225	180	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = {^tRAS}$ (MAX); $^tCK = {^tCK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	450	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {^tCK}$ (MIN); I_{OUT} = 0mA		I_{DD4R}	1260	1170	1125	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {^tCK}$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1260	1125	1080	mA
Auto refresh current	$^tREFC = {^tRFC}$ (MIN)	I_{DD5}	2385	1980	1980	mA
	^tREFC = 15.625µs	I_{DD5A}	45	45	45	
Self refresh current: CKE ≤ 0.2V		I_{DD6}	36	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^tRC = {^tRC}$ (MIN); $^tCK = {^tCK}$ (MIN); Address and control inputs change only during active READ or WRITE commands		I_{DD7}	3195	2970	2925	mA

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Table 11: I_{DD} Specifications and Conditions – 256MB (Die Revision F)

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-262	-265	Units
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	1215	1125	1125	1080	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	1530	1530	1440	1305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD2P}	36	36	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	540	450	405	405	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD3P}	360	270	225	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	630	540	450	450	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}	1800	1575	1350	1350	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1755	1575	1350	1350	mA
Auto refresh current	$^tREFC = {}^tRFC$ (MIN)	I_{DD5}	2340	2295	2115	2205	mA
	^tREFC = 7.8125µs	I_{DD5A}	54	54	54	54	
Self refresh current: CKE ≤ 0.2V		I_{DD6}	36	36	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		I_{DD7}	4230	3690	3150	3285	mA

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Table 12: I_{DD} Specifications and Conditions – 256MB (Die Revision K)
Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	900	810	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	1080	1035	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD2P}	36	36	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	450	450	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD3P}	315	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	540	495	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}	1620	1440	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1620	1440	mA
Auto refresh current	$^tREFC = {}^tRFC$ (MIN)	I_{DD5}	1440	1440	mA
	^tREFC = 15.625µs	I_{DD5A}	54	54	
Self refresh current: CKE ≤ 0.2V		I_{DD6}	36	36	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		I_{DD7}	2610	2430	mA

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Table 13: I_{DD} Specifications and Conditions – 256MB (Die Revision M)

Values are shown for the MT46V32M8 DDR SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

<table>
<tr><th colspan="2">Parameter/Condition</th><th>Symbol</th><th>-40B</th><th>-335</th><th>Units</th></tr>
<tr><td colspan="2">Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles</td><td>I_{DD0}</td><td>630</td><td>540</td><td>mA</td></tr>
<tr><td colspan="2">Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle</td><td>I_{DD1}</td><td>765</td><td>675</td><td>mA</td></tr>
<tr><td colspan="2">Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW</td><td>I_{DD2P}</td><td>36</td><td>36</td><td>mA</td></tr>
<tr><td colspan="2">Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS</td><td>I_{DD2F}</td><td>207</td><td>207</td><td>mA</td></tr>
<tr><td colspan="2">Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW</td><td>I_{DD3P}</td><td>126</td><td>126</td><td>mA</td></tr>
<tr><td colspan="2">Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle</td><td>I_{DD3N}</td><td>270</td><td>270</td><td>mA</td></tr>
<tr><td colspan="2">Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA</td><td>I_{DD4R}</td><td>855</td><td>765</td><td>mA</td></tr>
<tr><td colspan="2">Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle</td><td>I_{DD4W}</td><td>945</td><td>855</td><td>mA</td></tr>
<tr><td rowspan="2">Auto refresh current</td><td>$^tREFC = {}^tRFC$ (MIN)</td><td>I_{DD5}</td><td>1035</td><td>945</td><td rowspan="2">mA</td></tr>
<tr><td>^tREFC = 15.625μs</td><td>I_{DD5A}</td><td>54</td><td>54</td></tr>
<tr><td colspan="2">Self refresh current: CKE ≤ 0.2V</td><td>I_{DD6}</td><td>36</td><td>36</td><td>mA</td></tr>
<tr><td colspan="2">Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands</td><td>I_{DD7}</td><td>1575</td><td>1575</td><td>mA</td></tr>
</table>

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Table 14: I_{DD} Specifications and Conditions – 512MB (Die Revision F)

Values are shown for MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	-26A/ -265	Units
Operating one bank active-precharge current: ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	1395	1170	1035	mA
Operating one bank active-read-precharge current: BL = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	1665	1440	1305	mA
Precharge power-down standby current: All device banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD2P}	45	45	45	mA
Idle standby current: CS# = HIGH; All device banks idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; V_{IN} = V_{REF} for DQ, DM, and DQS		I_{DD2F}	495	405	360	mA
Active power-down standby current: One device bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}	405	315	270	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	540	450	405	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}	1710	1485	1305	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1775	1575	1215	mA
Auto refresh current	^tREFC = ^tRFC (MIN)	I_{DD5}	3105	2610	2520	mA
	^tREFC = 7.8125µs	I_{DD5A}	99	90	90	
Self refresh current: CKE ≤ 0.2V		I_{DD6}	45	45	45	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); Address and control inputs change only during active READ or WRITE commands		I_{DD7}	4050	3645	3150	mA

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Table 15: I_{DD} Specifications and Conditions – 512MB (Die Revision J)

Values are shown for the MT46V64M8 DDR SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-40B	-335	Units
Operating one bank active-precharge current: $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	675	585	mA
Operating one bank active-read-precharge current: BL = 4; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	765	675	mA
Precharge power-down standby current: All device banks idle; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD2P}	45	45	mA
Idle standby current: CS# = HIGH; All device banks idle; $^tCK = {}^tCK$ (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DM, and DQS		I_{DD2F}	207	207	mA
Active power-down standby current: One device bank active; Power-down mode; $^tCK = {}^tCK$ (MIN); CKE = LOW		I_{DD3P}	162	126	mA
Active standby current: CS# = HIGH; CKE = HIGH; One device bank active; $^tRC = {}^tRAS$ (MAX); $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	360	342	mA
Operating burst read current: BL = 2; Continuous burst reads; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); I_{OUT} = 0mA		I_{DD4R}	1080	765	mA
Operating burst write current: BL = 2; Continuous burst writes; One device bank active; Address and control inputs changing once per clock cycle; $^tCK = {}^tCK$ (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	1080	855	mA
Auto refresh current	$^tREFC = {}^tRFC$ (MIN)	I_{DD5}	1080	945	mA
	^tREFC = 15.625µs	I_{DD5A}	72	72	
Self refresh current: CKE ≤ 0.2V		I_{DD6}	45	45	mA
Operating bank interleave read current: Four device bank interleaving reads (BL = 4) with auto precharge; $^tRC = {}^tRC$ (MIN); $^tCK = {}^tCK$ (MIN); Address and control inputs change only during active READ or WRITE commands		I_{DD7}	2070	1890	mA

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Serial Presence-Detect

Table 16: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	2.3	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	$V_{DDSPD} \times 0.7$	$V_{DDSPD} + 0.5$	V
Input low voltage: Logic 0; All inputs	V_{IL}	–1.0	$V_{DDSPD} \times 0.3$	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
Standby current: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
Power supply current: SCL clock frequency = 100 kHz	I_{CC}	–	2.0	mA

Table 17: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
Clock/data fall time	^{t}F	–	300	ns	2
Clock/data rise time	^{t}R	–	300	ns	2
Data-in hold time	$^{t}HD:DAT$	0	–	µs	
Start condition hold time	$^{t}H:STA$	0.6	–	µs	
Clock HIGH period	$^{t}HIGH$	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	$^{t}SU:DAT$	100	–	ns	
Start condition setup time	$^{t}SU:STA$	0.6	–	µs	3
Stop condition setup time	$^{t}SU:STO$	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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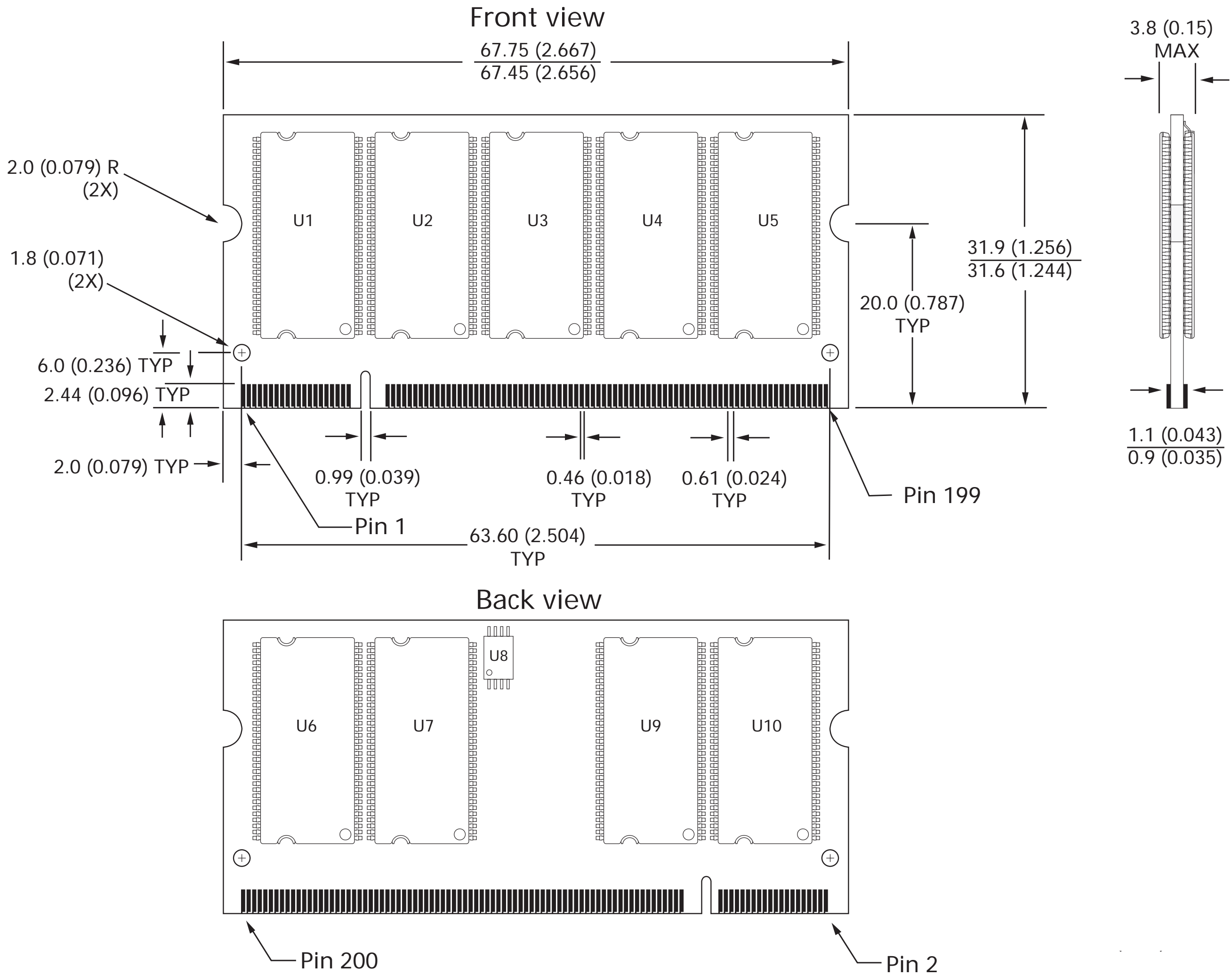
Module Dimensions

Figure 5: 200-Pin SODIMM – Low-Profile Layout



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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Figure 6: 200-Pin SODIMM – Standard Layout

Front view

67.72 (02.666)
67.45 (02.656)
3.8 (0.15) MAX
U1
U3
U4
U2
U5
2.0 (0.079) R (2X)
1.8 (0.071) (2X)
6.0 (0.236) TYP
2.44 (0.096) TYP
2.0 (0.079) TYP
35.69 (1.505)
35.43 (1.495)
20.0 (0.787) TYP
1.1 (0.043)
0.9 (0.035)
0.99 (0.039) TYP
0.46 (0.018) TYP
0.61 (0.024) TYP
Pin 1
Pin 199
63.60 (2.504) TYP

Back view

U6
U8
U9
U7
U10
Pin 200
Pin 2

Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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