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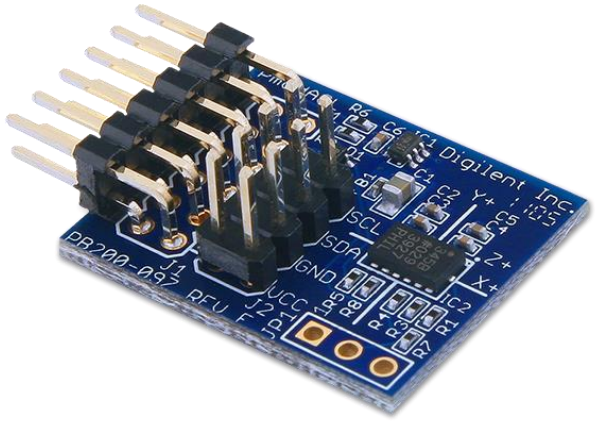
PmodACL™ Reference Manual

Revised April 15, 2016
This manual applies to the PmodACL rev. E

Overview

The Digilent PmodACL is a 3-axis digital accelerometer module powered by the Analog Devices® ADXL345.



The PmodACL.

Features include:

- 3-axis, ±2/4/8/16g accelerometer
- User-selectable resolution
- Activity/inactivity monitoring
- Single/double-tap and free-fall detection
- Small PCB size for flexible designs 1.0 in × 0.8 in (2.5 cm × 2.0 cm)
- 12-pin Pmod port with SPI interface and 2×4-pin I²C interface
- Follows Digilent Pmod Interface Specification Type 2A
- Library and example code available in resource center

1 Functional Description

The PmodACL utilizes Analog Devices ADXL345 to provide high resolution acceleration changes including inclination changes of less than 1.0°. With free fall and single/double-tap detection capabilities, the PmodACL can be configured to take measurements on the user's whim.

2 Interfacing with the Pmod

The PmodACL communicates with the host board via the SPI protocol or the I²C protocol. SPI communication is enabled when the Chip Select line is driven low; conversely, the I²C protocol is enabled when the Chip Select line is driven to a logic level high voltage. An interrupt can be triggered whenever a measured axis acceleration data is over a user-defined threshold limit. A data stream setting the threshold activity to a value of 250 mg and Interrupt 1 to be triggered whenever the X and Y axis exceeds the threshold level through SPI is provided below in Table 1.

Read/~Write	Multi-byte	6-bit Threshold Activity Address					
0	0	1	0	0	1	0	0
8 bits of Threshold Activity data (62.5 mg/LSB scale)							
0	0	0	0	0	1	0	0
Read/~Write	Multi-byte	6-bit Activity/Inactivity Control Address					
0	0	1	0	0	1	1	1
Activity/Inactivity Control Settings							
ACT ac/dc	ACT X	ACT Y	ACT Z	INACT ac/dc	INACT X	INACT Y	INACT Z
0	1	1	0	0	0	0	0
Read/~Write	Multi-byte	6-bit Interrupt Enable Address					
0	0	1	0	1	1	1	0
8 bits of Which Interrupt Sources Are Enabled							
Data Ready	Single Tap	Double Tap	Activity	Inactivity	Free Fall	Watermark	Overrun
0	0	0	1	0	0	0	0

Table 1. Data stream setting the threshold activity through SPI

Once an interrupt has been generated, users may read the data registers (0x32 - 0x37) for the 10 bits of two's complement data in the X, Y, and Z axes, respectively. The data in the two registers for each axis is right-justified with sign extensions as the leading 6 bits. Reading the Interrupt source register (0x30) clears the activity interrupt bit D4.

Users may also follow the given example code functions and demonstration to start collecting accelerometer data.

2.1 Pinout Description Table

Pin	Signal	Description
1	~CS	Chip Select
2	MOSI	Master-out-slave-in
3	MISO	Master-in-slave-out
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V)
7	INT2	Interrupt 2
8	INT1	Interrupt 1
9	NC	Not Connected
10	NC	Not Connected
11	GND	Power Supply Ground
12	VCC	Power Supply (3.3V)

Table 2. Pmod header J1.

Pin	Signal	Description
1, 5	SCL	Serial Clock
2, 6	SDA	Serial Data
3, 7	GND	Power Supply Ground
4, 8	VCC	Positive Power Supply

Table 3. Pmod header J2.

Any external power applied to the PmodACL must be within 2.0V and 3.6V; however, it is strongly recommended that the Pmod is operated at 3.3V.

3 Physical Dimensions

The pins on the pin header are spaced 100 mil apart. The PCB is 1 inch long on the sides parallel to the pins on the pin header and 0.8 inches long on the sides perpendicular to the pin header.