Logic level TOPFET
SMD version of BUK104-50L/S

BUK114-50L/S

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in a 5 pin surface mounting plastic envelope, intended as a general purpose switch for automotive systems and other applications.

APPLICATIONS

General controller for driving
- lamps
- motors
- solenoids
- heaters

FEATURES

- Vertical power DMOS output stage
- Low on-state resistance
- Logic and protection supply from separate pin
- Low operating supply current
- Overload protection against over temperature
- Overload protection against short circuit load
- Latched overload protection reset by protection supply
- Protection circuit condition indicated by flag pin
- 5 V logic compatible input level
- Separate input pin for higher frequency drive
- ESD protection on input, flag and protection supply pins
- Over voltage clamping for turn off of inductive loads
- Both linear and switching operation are possible

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Continuous drain source voltage	50	V
I_D	Continuous drain current	15	A
P_{tot}	Total power dissipation	40	W
T_j	Continuous junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance		
	V_{IS} = 5 V	125	mΩ
	V_{IS} = 7 V	100	mΩ
SYMBOL	**PARAMETER**	**NOM.**	**UNIT**
V_{PSN}	Protection supply voltage		
	BUK114-50L	5	V
	BUK114-50S	10	V

FUNCTIONAL BLOCK DIAGRAM

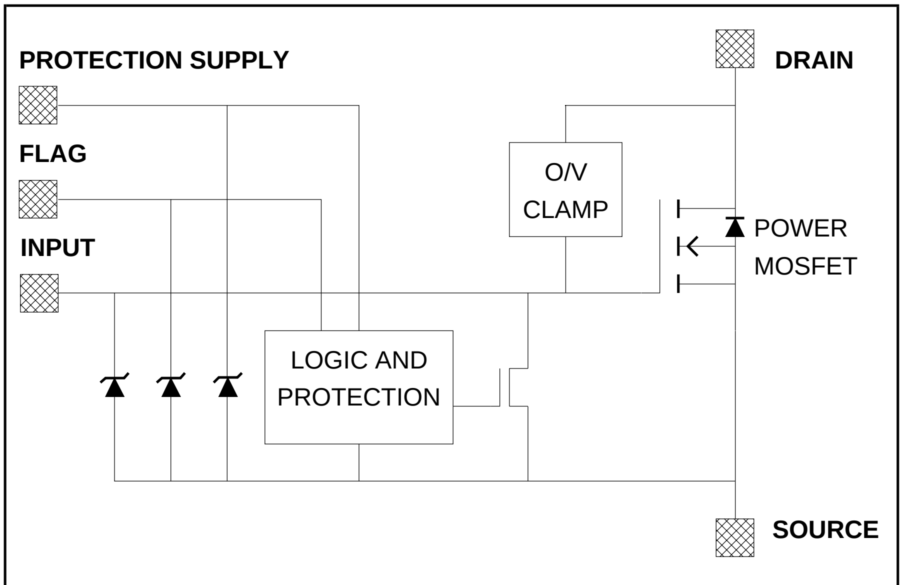

Fig.1. Elements of the TOPFET.

PINNING - SOT426

PIN	DESCRIPTION
1	input
2	flag
3	(connected to mb)
4	protection supply
5	source
mb	drain

PIN CONFIGURATION

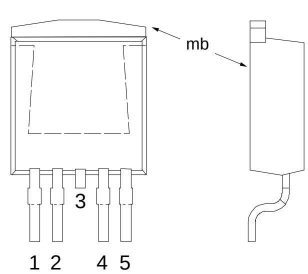

Fig. 2.

SYMBOL

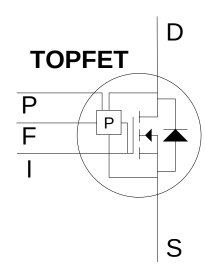

Fig. 3.

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
	Voltages					
V_{DSS}	Continuous off-state drain source voltage[1]	V_{IS} = 0 V	-	50		V
V_{IS}	Continuous input voltage	-	0	11		V
V_{FS}	Continuous flag voltage	-	0	11		V
V_{PS}	Continuous supply voltage	-	0	11		V
	Currents	V_{IS} =	-	7	5	V
I_D	Continuous drain current	$T_{mb} \leq 25$ ˚C	-	15	13	A
I_D	Continuous drain current	$T_{mb} \leq 100$ ˚C	-	9.5	8.5	A
I_{DRM}	Repetitive peak on-state drain current	$T_{mb} \leq 25$ ˚C	-	60	54	A
	Thermal					
P_{tot}	Total power dissipation	T_{mb} = 25 ˚C	-	40		W
T_{stg}	Storage temperature	-	-55	150		˚C
T_j	Junction temperature[2]	continuous	-	150		˚C
T_{sold}	Lead temperature	during soldering	-	250		˚C

OVERLOAD PROTECTION LIMITING VALUES

With the protection supply connected, TOPFET can protect itself from two types of overload - over temperature and short circuit load.

An n-MOS transistor turns on between the input and source to quickly discharge the power MOSFET gate capacitance.

For internal overload protection to remain latched while the control circuit is high, external series input resistance must be provided. Refer to INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.	UNIT
		V_{IS} =	7	5	-	V
V_{PSP}	Protection supply voltage[3]	for valid protection				
		BUK114-50L	4.4	4	-	V
		BUK114-50S	5.4	5	-	V
	Over temperature protection	$V_{PS} = V_{PSN}$				
$V_{DDP(T)}$	Protected drain source supply voltage	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		50	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		50	V
	Short circuit load protection	$V_{PS} = V_{PSN}$; $L \leq 10$ µH				
$V_{DDP(P)}$	Protected drain source supply voltage[4]	V_{IS} = 10 V; $R_I \geq 2$ kΩ	-		25	V
		V_{IS} = 5 V; $R_I \geq 1$ kΩ	-		45	V
P_{DSM}	Instantaneous overload dissipation		-		0.8	kW

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model; C = 250 pF; R = 1.5 kΩ	-	2	kV

1 Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

2 A higher T_j is allowed as an overload condition but at the threshold $T_{j(TO)}$ the over temperature trip operates to protect the switch.

3 The minimum supply voltage required for correct operation of the overload protection circuits.

4 The device is able to self-protect against a short circuit load providing the drain-source supply voltage does not exceed $V_{DDP(P)}$ maximum. For further information, refer to OVERLOAD PROTECTION CHARACTERISTICS.

OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{DRRM}	Repetitive peak clamping drain current	$R_{IS} \geq 100\ \Omega$[1]	-	15	A
E_{DSM}	Non-repetitive inductive turn-off energy[2]	I_{DM} = 15 A; $R_{IS} \geq 100\ \Omega$	-	200	mJ
E_{DRM}	Repetitive inductive turn-off energy	$R_{IS} \geq 100\ \Omega$; $T_{mb} \leq 95$ ˚C; I_{DM} = 4 A; $V_{DD} \leq 20$ V; f = 250 Hz	-	20	mJ
I_{DIRM}	Repetitive peak drain to input current[3]	$R_{IS} = 0\ \Omega$; $t_p \leq 1$ ms	-	50	mA

REVERSE DIODE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_S	Continuous forward current	T_{mb} = 25 ˚C; $V_{IS} = V_{PS} = V_{FS}$ = 0 V	-	15	A

THERMAL CHARACTERISTIC

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Thermal resistance					
$R_{th\ j-mb}$	Junction to mounting base	-	-	2.5	3.1	K/W

STATIC CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; I_D = 10 mA		50	-	65	V
$V_{(CL)DSR}$	Drain-source clamping voltage	$R_{IS} = 100\ \Omega$; I_{DM} = 1 A; $t_p \leq 300\ \mu$s; $\delta \leq 0.01$		50	-	70	V
I_{DSS}	Zero input voltage drain current	V_{DS} = 12 V; V_{IS} = 0 V		-	0.5	10	µA
I_{DSR}	Drain source leakage current	V_{DS} = 50 V; $R_{IS} = 100\ \Omega$;		-	1	20	µA
I_{DSR}	Drain source leakage current	V_{DS} = 40 V; $R_{IS} = 100\ \Omega$; T_j = 125 ˚C		-	10	100	µA
$R_{DS(ON)}$	Drain-source on-state resistance	I_{DM} = 7.5 A;	V_{IS} = 7 V	-	75	100	mΩ
		$t_p \leq 300\ \mu$s; $\delta \leq 0.01$	V_{IS} = 5 V	-	95	125	mΩ

1 The input pin must be connected to the source pin by a specified external resistance to allow the power MOSFET gate source voltage to become sufficiently positive for active clamping. Refer to INPUT CHARACTERISTICS.

2 While the protection supply voltage is connected, during overvoltage clamping it is possible that the overload protection may operate at energies close to the limiting value. Refer to OVERLOAD PROTECTION CHARACTERISTICS.

3 Shorting the input to source with low resistance inhibits the internal overvoltage protection by preventing the power MOSFET gate source voltage becoming positive.

OVERLOAD PROTECTION CHARACTERISTICS

With adequate protection supply voltage TOPFET detects when one of the overload thresholds is exceeded.

Provided there is adequate input series resistance it switches off and remains latched off until reset by the protection supply pin.

Refer also to OVERLOAD PROTECTION LIMITING VALUES and INPUT CHARACTERISTICS.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Short circuit load protection[1]	$V_{PS} = V_{PSN}$[2]; T_{mb} = 25 ˚C; L ≤ 10 µH; R_I ≥ 2 kΩ				
$E_{DS(TO)}$	Overload threshold energy	V_{DD} = 13 V; V_{IS} = 10 V	-	150	-	mJ
$t_{d\ sc}$	Response time	V_{DD} = 13 V; V_{IS} = 10 V	-	375	-	µs
	Over temperature protection	$V_{PS} = V_{PSN}$; R_I ≥ 2 kΩ				
$T_{j(TO)}$	Threshold junction temperature	from I_D ≥ 0.65 A[3]	150	-	-	˚C

TRANSFER CHARACTERISTICS

T_{mb} = 25 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 10 V; I_{DM} = 7.5 A t_p ≤ 300 µs; δ ≤ 0.01	5	9	-	S
I_D	Drain current[4]	V_{DS} = 13 V; V_{IS} = 5 V	-	25	-	A
		V_{IS} = 10 V		40	-	A

PROTECTION SUPPLY CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Protection supply					
I_{PS}, I_{PSL}	Protection supply current	normal operation or protection latched				
		BUK114-50L V_{PS} = 5 V	-	0.2	0.35	mA
		BUK114-50S V_{PS} = 10 V	-	0.4	1.0	mA
V_{PSR}	Protection reset voltage[5]		1.5	2.5	3.5	V
		T_j = 150 ˚C	1.0	-	-	V
$V_{(CL)PS}$	Protection clamp voltage	I_P = 1.35 mA	11	13	-	V

REVERSE DIODE CHARACTERISTICS

T_{mb} = 25 ˚C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{SDS}	Forward voltage	I_S = 15 A; $V_{IS} = V_{PS} = V_{FS}$ = 0 V; t_p = 300 µs	-	1.0	1.5	V
t_{rr}	Reverse recovery time	not applicable[6]	-	-	-	-

1 The short circuit load protection is able to save the device providing the instantaneous on-state dissipation is less than the limiting value for P_{DSM}, which is always the case when V_{DS} is less than V_{DSP} maximum.

2 At the appropriate nominal protection supply voltage for each type. Refer to QUICK REFERENCE DATA.

3 The over temperature protection feature requires a minimum on-state drain source voltage for correct operation. The specified minimum I_D ensures this condition.

4 During overload condition. Refer also to OVERLOAD PROTECTION LIMITING VALUES and CHARACTERISTICS.

5 The supply voltage below which the overload protection circuits will be reset.

6 The reverse diode of this type is not intended for applications requiring fast reverse recovery.

INPUT CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Normal operation					
$V_{IS(TO)}$	Input threshold voltage	V_{DS} = 5 V; I_D = 1 mA	1.0	1.5	2.0	V
		T_{mb} = 150 ˚C	0.5	-	-	V
I_{IS}	Input current	V_{IS} = 10 V	-	10	100	nA
$V_{(CL)IS}$	Input clamp voltage	I_I = 1 mA	11	13	-	V
	Overload protection latched					
R_{ISL}	Input resistance[1]	V_{PS} = 5 V; I_I = 5 mA;	-	55	-	Ω
		T_{mb} = 150 ˚C	-	95	-	Ω
		V_{PS} = 10 V; I_I = 5 mA;	-	35	-	Ω
		T_{mb} = 150 ˚C	-	60	-	Ω
	Application information					
	External input resistances for	(see figure 29)				
R_{IS}	internal overvoltage clamping[2]	R_I = ∞ Ω; V_{DS} > 30 V	100	-	-	Ω
R_I	internal overload protection[3]	R_{IS} = ∞ Ω; V_{II} = 5 V	1	-	-	kΩ
		V_{II} = 10 V	2	-	-	kΩ

SWITCHING CHARACTERISTICS

T_{mb} = 25 ˚C; R_I = 50 Ω; R_{IS} = 50 Ω (see figure 29); resistive load R_L = 10 Ω. For waveforms see figure 28.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; V_{IS}: 0 V ⇒ 10 V	-	8	-	ns
t_r	Rise time		-	13	-	ns
$t_{d\ off}$	Turn-off delay time	V_{DD} = 15 V; V_{IS}: 10 V ⇒ 0 V	-	100	-	ns
t_f	Fall time		-	45	-	ns

CAPACITANCES

T_{mb} = 25 ˚C; f = 1 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	415	600	pF
C_{oss}	Output capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	275	400	pF
C_{rss}	Reverse transfer capacitance	V_{DS} = 25 V; V_{IS} = 0 V	-	55	80	pF
C_{pso}	Protection supply pin capacitance	V_{PS} = 10 V	-	30	-	pF
C_{fso}	Flag pin capacitance	V_{FS} = 10 V; V_{PS} = 0 V	-	20	-	pF

1 The resistance of the internal transistor which discharges the power MOSFET gate capacitance when overload protection operates.

The external drive circuit should be such that the input voltage does not exceed $V_{IS(TO)}$ minimum when the overload protection has operated. Refer also to figure for latched input characteristics.

2 Applications using a lower value for R_{IS} would require external overvoltage protection.

3 For applications requiring a lower value for R_I, an external overload protection strategy is possible using the flag pin to ‘tell’ the control circuit to switch off the input.

FLAG DESCRIPTION

The flag pin provides a means to detect the presence of the protection supply and indicate the state of the overload detectors. The flag is the open drain of an n-MOS transistor and requires an external pull-up resistor[1]. It is suitable for both 5 V and 10 V logic. Flag may be used to implement an external protection strategy[2] for applications which require low input drive impedance.

TRUTH TABLE

CONDITION	DESCRIPTION	FLAG
NORMAL	Normal operation and adequate protection supply voltage	LOGIC LOW
OVER TEMP.	Over temperature detected	LOGIC HIGH
SHORT CIRCUIT	Overload condition detected	LOGIC HIGH
SUPPLY FAULT	Inadequate protection supply voltage	LOGIC HIGH

FLAG CHARACTERISTICS

T_{mb} = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Flag 'low'	normal operation				
V_{FS}	Flag voltage	I_F = 1.6 mA	-	0.15	0.4	V
I_{FSS}	Flag saturation current	V_{FS} = 10 V	-	15	-	mA
	Flag 'high'	overload or fault				
I_{FS}	Flag leakage current	V_{FS} = 10 V	-	-	10	µA
V_{PSF}	Protection supply threshold voltage	V_{FF} = 5 V; R_F = 3 kΩ;				
		BUK114-50L	2.5	3.3	4	V
		BUK114-50S	3.3	4.2	5	V
$V_{(CL)FS}$	Flag clamping voltage	I_F = 1 mA; V_{PS} = 0 V	11	13	-	V
	Application information					
R_F	Suitable external pull-up resistance	V_{FF} =5 V	1	10	50	kΩ
		V_{FF} =10 V	2	20	100	kΩ

1 Even if the flag pin is not used, it is recommended that it is connected to the protection supply via a pull-up resistor. It should not be left floating.

2 Low pass filtering of the flag signal may be advisable to prevent false tripping.

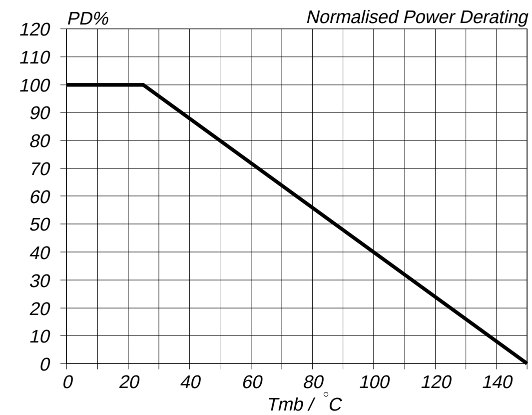

Fig.4. Normalised limiting power dissipation.
$P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$

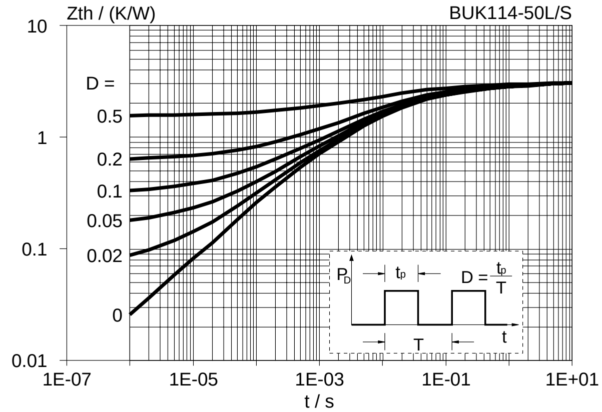

Fig.7. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

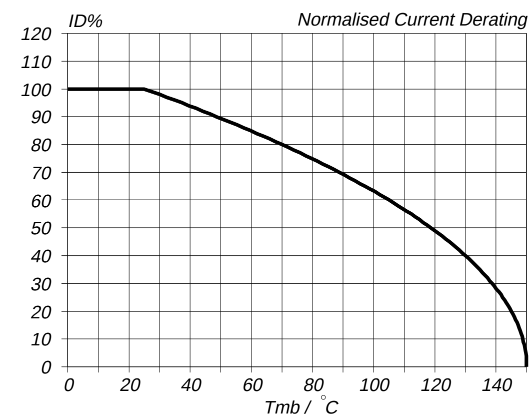

Fig.5. Normalised continuous drain current.
$I_D\% = 100 \cdot I_D/I_D(25\ ^\circ C) = f(T_{mb})$; conditions: $V_{IS} = 5$ V

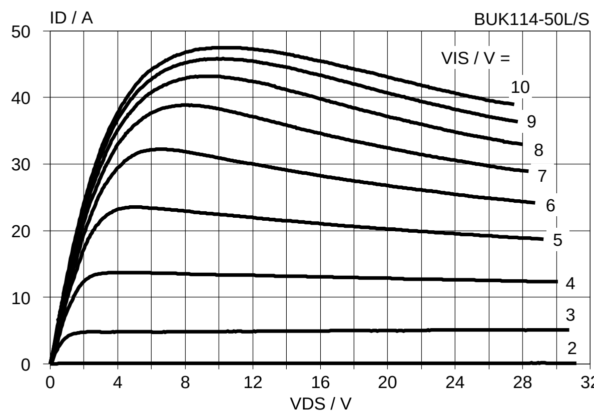

Fig.8. Typical output characteristics, $T_j = 25\ ^\circ C$.
$ID = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$ & $t_p < t_{d\ sc}$

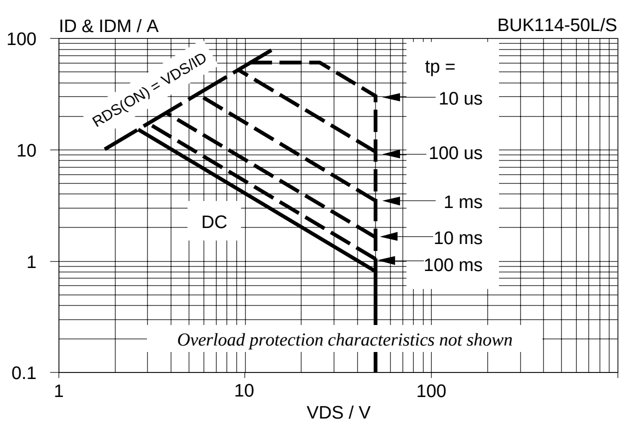

Fig.6. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

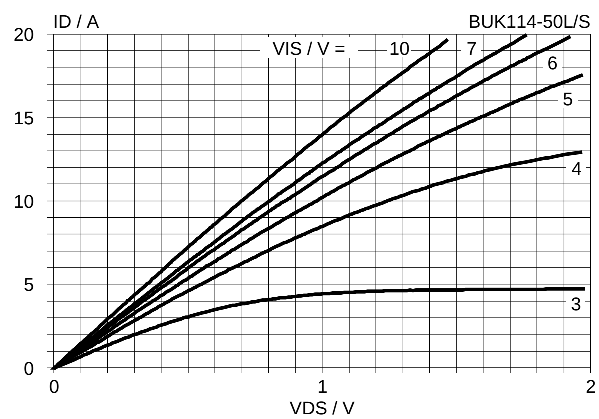

Fig.9. Typical on-state characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{IS}; $t_p = 250\ \mu s$

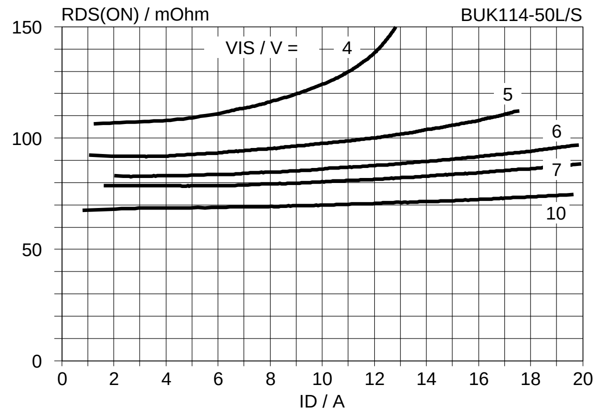

Fig.10. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{IS}; t_p = 250 µs

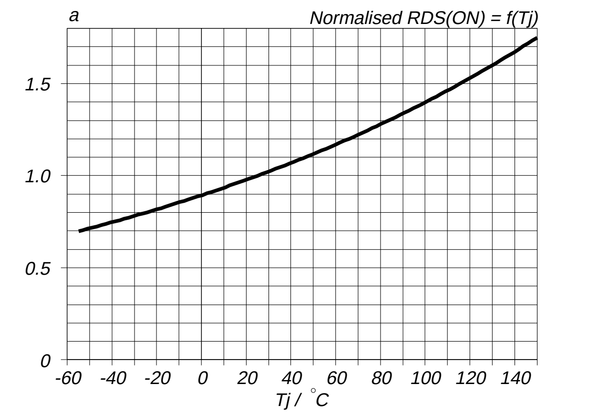

Fig.13. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)}$25 ˚C = $f(T_j)$; I_D = 7.5 A; $V_{IS} \geq 5$ V

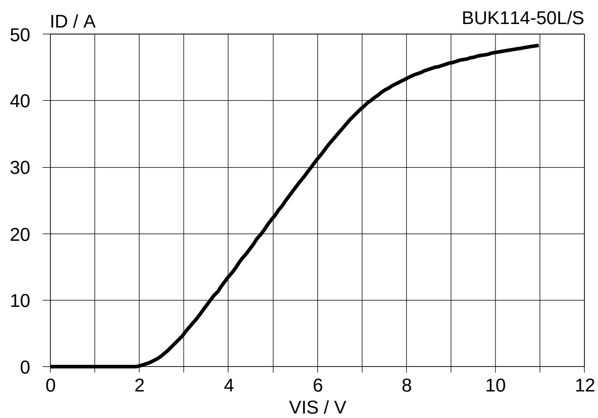

Fig.11. Typical transfer characteristics, T_j = 25 ˚C.
$I_D = f(V_{IS})$; conditions: V_{DS} = 10 V; t_p = 250 µs

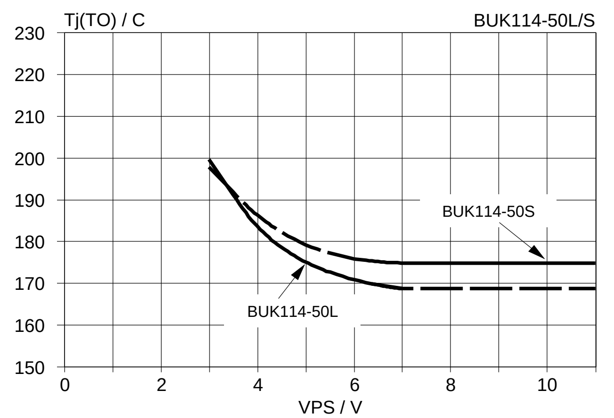

Fig.14. Typical over temperature protection threshold
$T_{j(TO)} = f(V_{PS})$; conditions: V_{DS} > 0.1 V

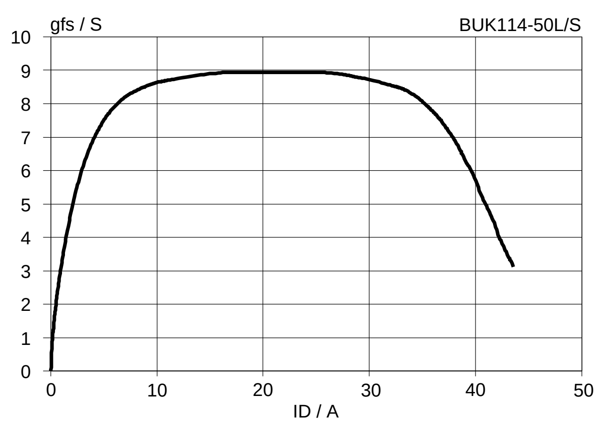

Fig.12. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 10 V; t_p = 250 µs

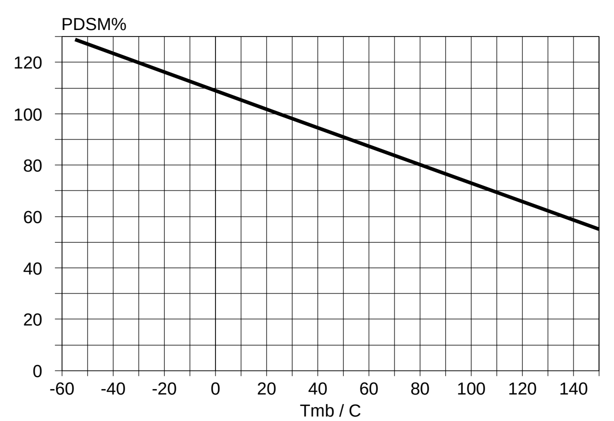

Fig.15. Normalised limiting overload dissipation.
$P_{DSM}\% = 100 \cdot P_{DSM}/P_{DSM}(25\ ˚C) = f(T_{mb})$

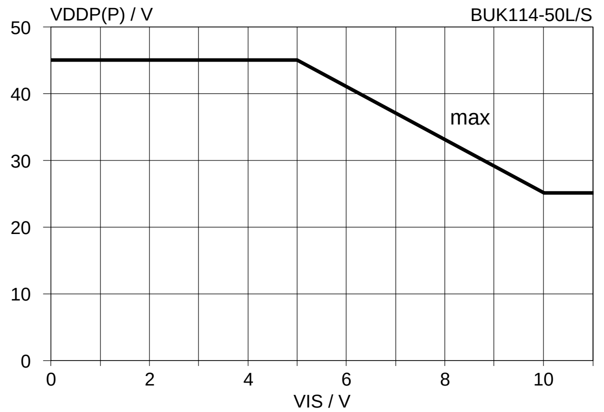

Fig.16. Maximum drain source supply voltage for SC load protection. $V_{DDP(P)} = f(V_{IS})$; $T_{mb} \leq 150$ ˚C

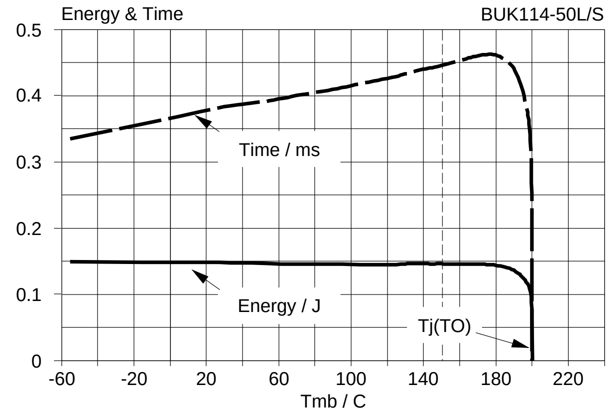

Fig.19. Typical overload protection characteristics. Conditions: V_{DD} = 13 V; $V_{PS} = V_{PSN}$, V_{IS} = 7 V; SC load

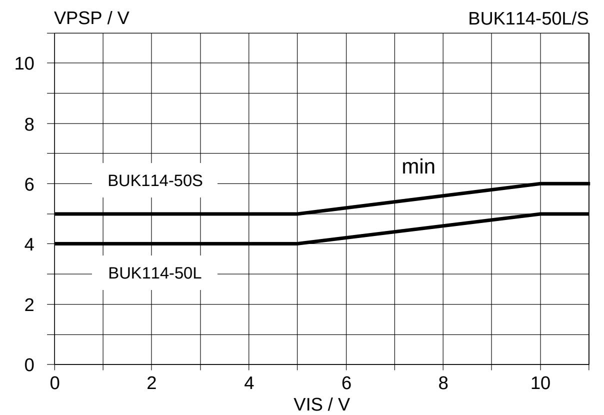

Fig.17. Minimum protection supply voltage for SC load protection. $V_{PSP} = f(V_{IS})$; $T_{mb} \geq 25$ ˚C

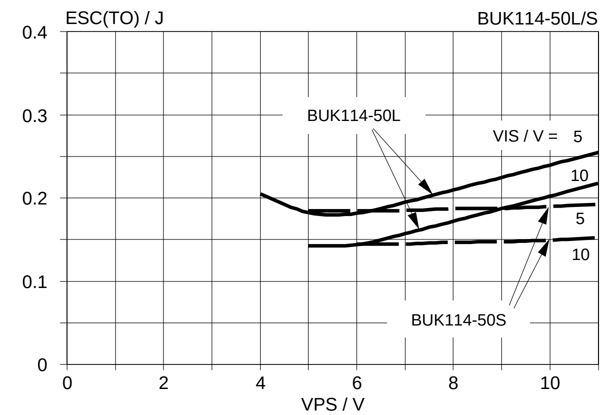

Fig.20. Typical overload protection energy, T_j = 25 ˚C $E_{SC(TO)} = f(V_{PS})$; conditions: V_{DS} = 13 V, parameter V_{IS}

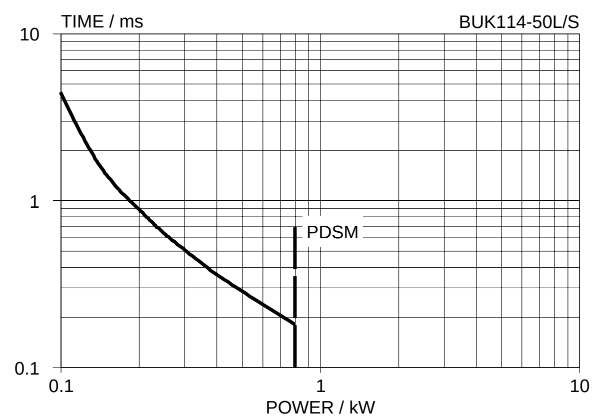

Fig.18. Typical overload protection characteristics. $t_{d\,sc} = f(P_{DS})$; conditions: $V_{PS} \geq V_{PSP}$; $V_{IS} \geq 5$ V

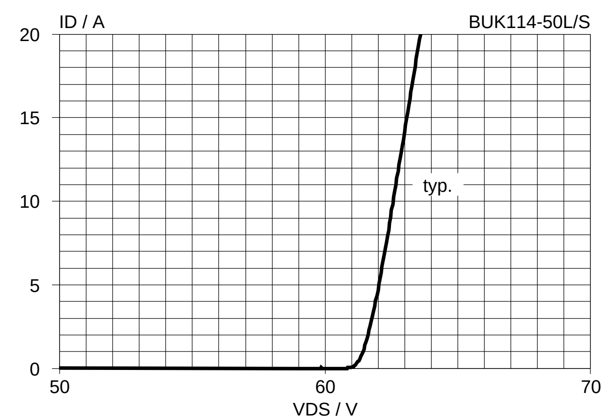

Fig.21. Typical clamping characteristics, 25 ˚C. $I_D = f(V_{DS})$; conditions: R_{IS} = 100 Ω; $t_p \leq 50$ µs

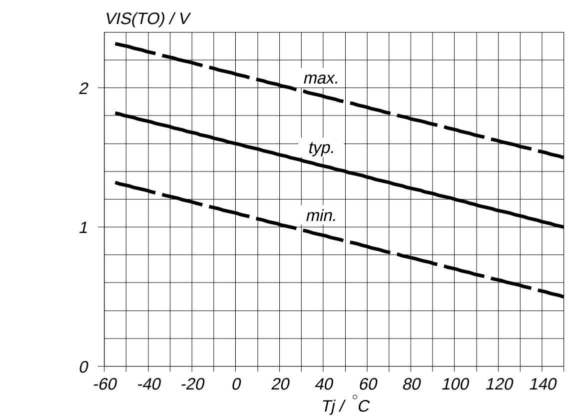

Fig.22. Input threshold voltage.
$V_{IS(TO)} = f(T_j)$; conditions: I_D = 1 mA; V_{DS} = 5 V

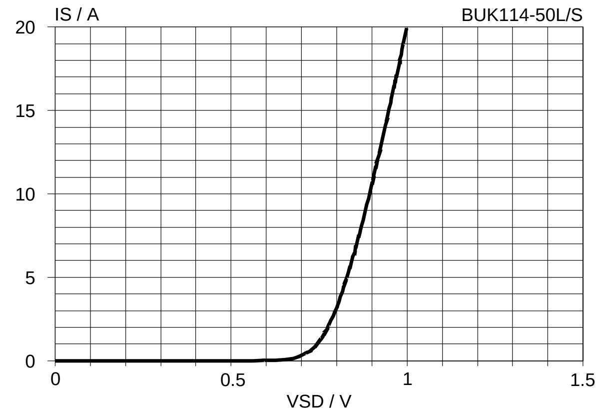

Fig.25. Typical reverse diode current, T_j = 25 ˚C.
$I_S = f(V_{SDS})$; conditions: V_{IS} = 0 V; t_p = 250 µs

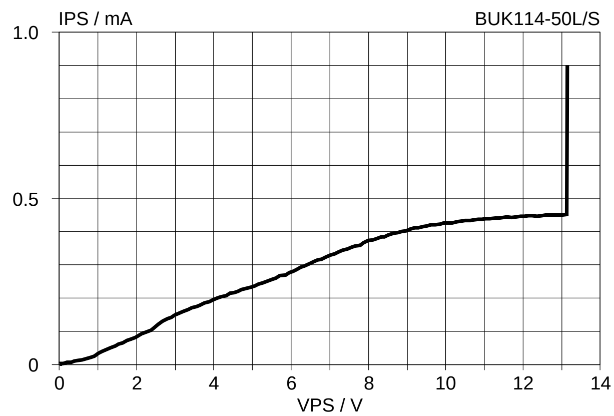

Fig.23. Typical DC protection supply characteristics.
$I_{PS} = f(V_{PS})$; normal or overload operation; T_j = 25 ˚C

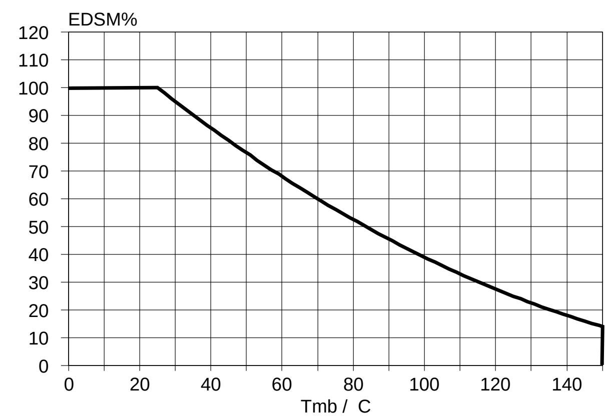

Fig.26. Normalised limiting clamping energy.
$E_{DSM}\% = f(T_{mb})$; conditions: I_D = 15 A

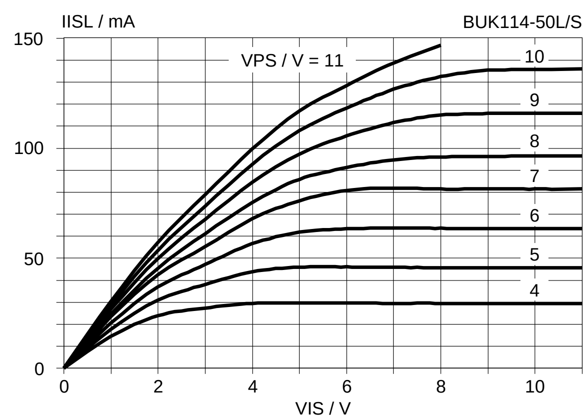

Fig.24. Typical latched input characteristics, 25 ˚C.
$I_{ISL} = f(V_{IS})$; after overload protection latched

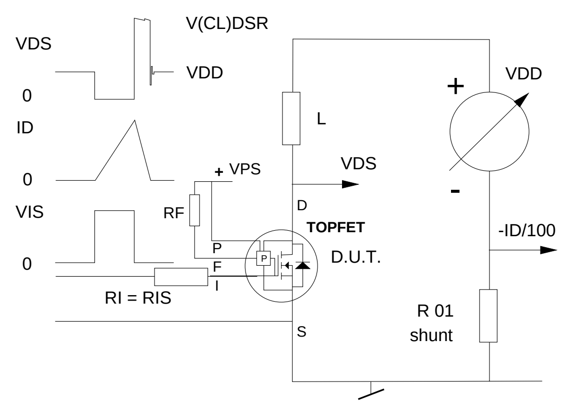

Fig.27. Clamping energy test circuit, R_{IS} = 100 Ω.
$$E_{DSM} = 0.5 \cdot LI_D^2 \cdot V_{(CL)DSR}/(V_{(CL)DSR} - V_{DD})$$

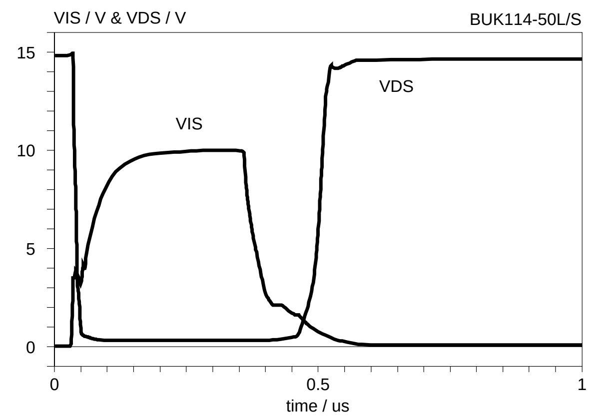

Fig.28. Typical resistive load switching waveforms
$R_I = R_{IS} = 50\ \Omega$; $R_L = 10\ \Omega$; $V_{DD} = 15$ V; $T_j = 25$ ˚C

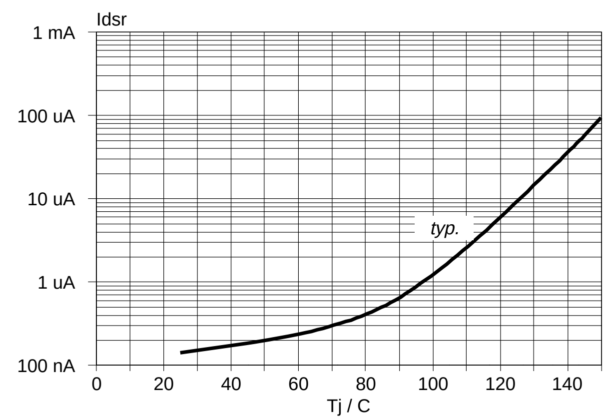

Fig.31. Typical off-state leakage current.
$I_{DSR} = f(T_j)$; Conditions: $V_{DS} = 40$ V; $R_{IS} = 100\ \Omega$.

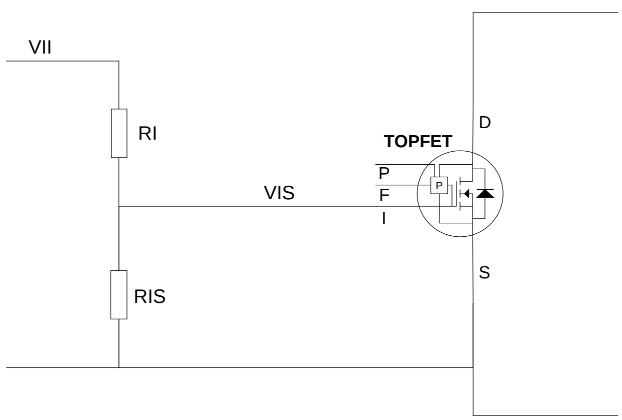

Fig.29. External input resistances R_I and R_{IS}, generator voltage V_{II} and input voltage V_{IS}.

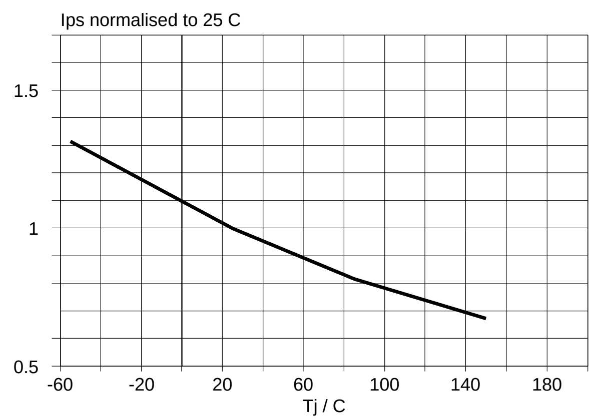

Fig.32. Normalised protection supply current.
$I_{PS}/I_{PS}25$ ˚C $= f(T_j)$; $V_{PS} = V_{PSN}$

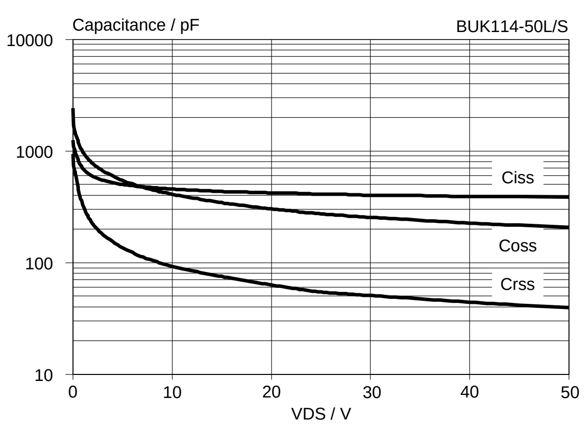

Fig.30. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{IS} = 0$ V; f = 1 MHz

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.5 g

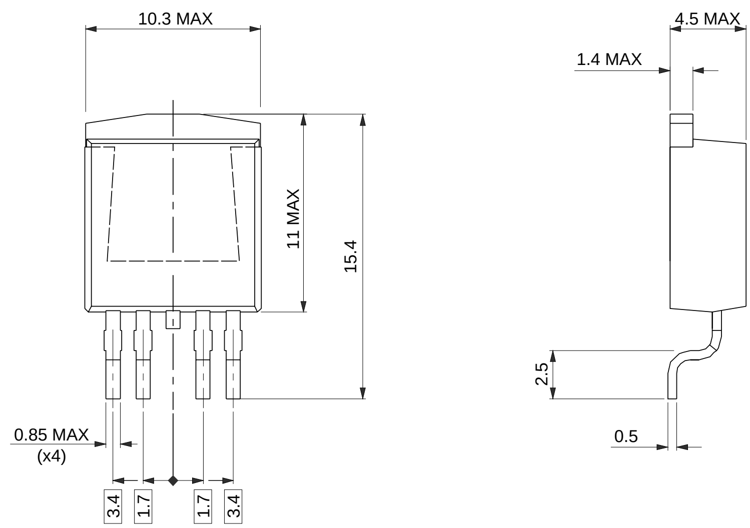

Fig.33. SOT426

mounting base connected to centre pin (cropped short)

MOUNTING INSTRUCTIONS

Dimensions in mm

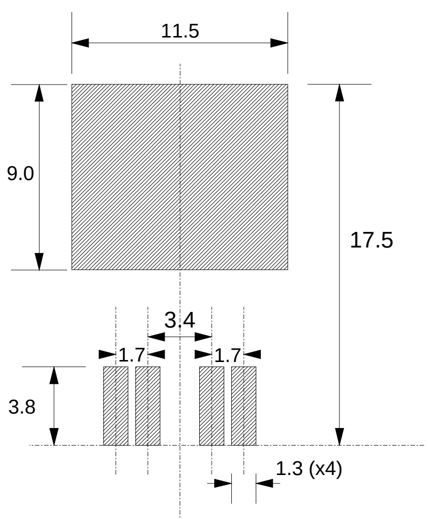

Fig.34. SOT426

soldering pattern for surface mounting.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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