INTEGRATED CIRCUITS

DATA SHEET

TEA6846H
New In Car Entertainment (NICE) car radio

Product specification
Supersedes data of 2001 Apr 12

2003 Feb 04

Philips
Semiconductors

CONTENTS

1 FEATURES

- FM mixer for conversion of FM RF from 65 to 108 MHz to IF of 10.7 MHz; the mixer provides inherent image rejection
- FM RF mixer can be set to receive weather band radio up to 162.55 MHz; weather band radio flag output
- AM mixer 1 for conversion of AM RF to AM IF1 of 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 of 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count, timing for Radio Data System (RDS) update and reference frequency for car audio signal processor ICs
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx or TEF689x)
- Digital auto alignment circuit for conversion of LC oscillator tuning voltage to controlled alignment voltage of FM antenna tank circuit
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode drive can be activated by the I^2C-bus as a local or distance function; AGC threshold is a programmable and keyed function switchable via the I^2C-bus
- FM IF linear amplifiers with high dynamic input range
- FM quadrature demodulator with automatic centre frequency adjustment and Total Harmonic Distortion (THD) compensation
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I^2C-bus
- AM RF PIN diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I^2C-bus; AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with blanking at AM IF2
- Several test modes available for fast IC and system tests.

2 GENERAL DESCRIPTION

The TEA6846H is a single IC with car radio tuner for AM and FM intended for microcontroller tuning with the I^2C-bus. It provides the following functions:

- AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6846H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDA(n)}$	analog supply voltage 1, 3, 4, 5 and 6		8	8.5	9	V
$I_{DDA(tot)}$	total analog supply current 1, 3, 4, 5 and 6	FM mode	45	56	67	mA
		AM mode	39	49	59	mA
V_{DDA2}	analog supply voltage 2		4.75	5	5.25	V
I_{DDA2}	analog supply current 2	FM mode	6.5	8.1	9.8	mA
		AM mode	4.7	5.9	7.1	mA
V_{DDD}	digital supply voltage		4.75	5	5.25	V
I_{DDD}	digital supply current	FM mode	18	23	28	mA
		AM mode	18	23	28	mA
$f_{AM(ant)}$	AM input frequency	LW	0.144	–	0.288	MHz
		MW	0.522	–	1.710	MHz
		SW	5.85	–	9.99	MHz
$f_{FM(ant)}$	FM input frequency		65	–	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	–	162.55	MHz
T_{amb}	ambient temperature		–40	–	+85	°C
AM overall system parameters (1 × SFE10.7MS3; 1 × SFR450H)						
(S+N)/N	signal plus noise-to-noise ratio	m = 0.3	–	58	–	dB
THD	total harmonic distortion	m = 0.8	–	0.3	–	%
		m = 0.9	–	0.5	–	%
FM overall system parameters (3 × SFE10.7MS3)						
(S+N)/N	signal plus noise-to-noise ratio	Δf = 22.5 kHz; de-emphasis = 50 μs	–	65	–	dB
THD	total harmonic distortion	Δf = 75 kHz	–	0.6	1	%

5 BLOCK DIAGRAM

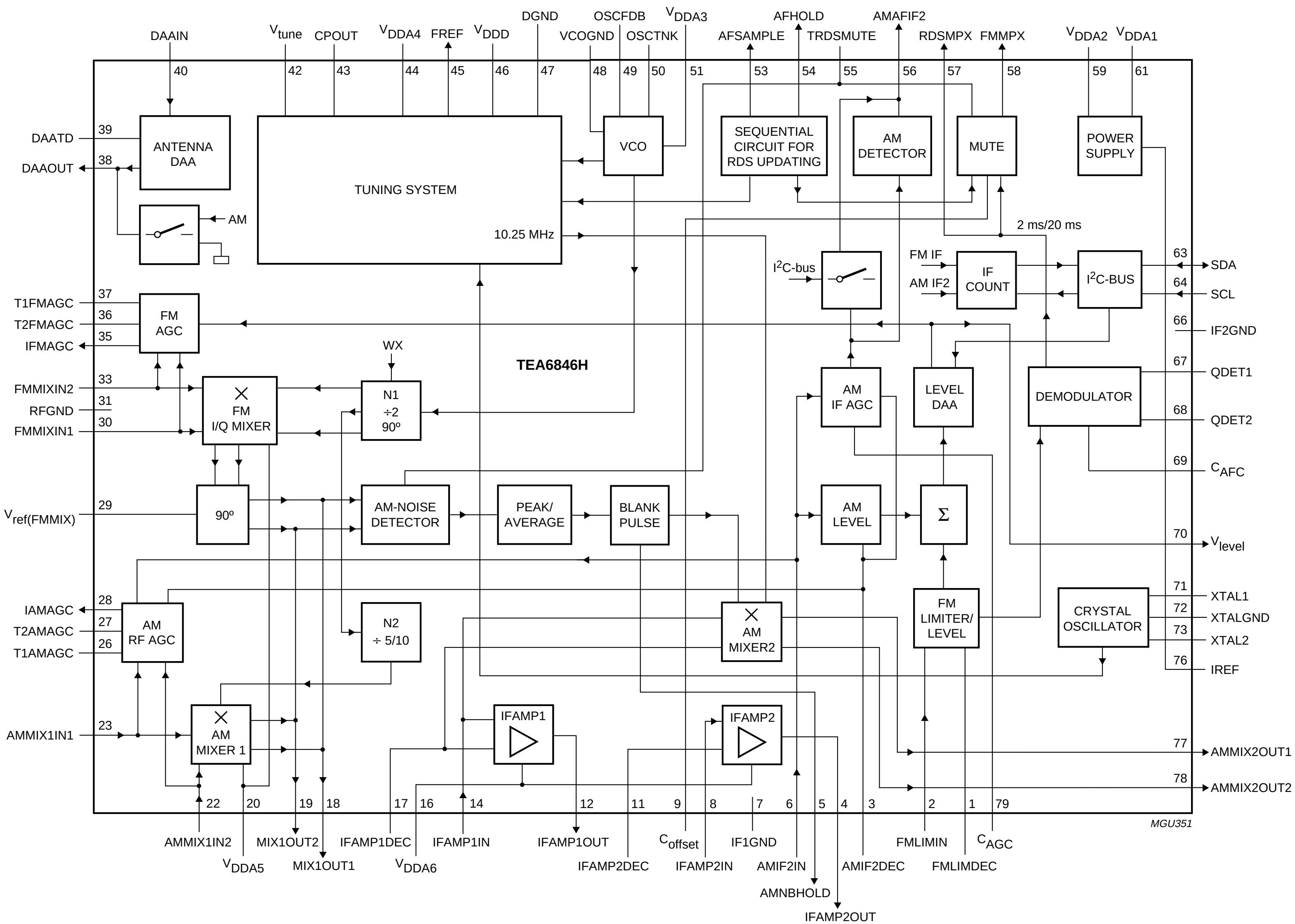


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
FMLIMDEC	1	FM limiter decoupling
FMLIMIN	2	FM limiter input (10.7 MHz)
AMIF2DEC	3	decoupling for AM IF2 input
IFAMP2OUT	4	IF amplifier 2 output (10.7 MHz)
AMNBHOLD	5	AM noise blanker threshold
AMIF2IN	6	AM IF2 input (450 kHz) for demodulator AGC and AM level detector
IF1GND	7	AM IF1 ground
IFAMP2IN	8	IF amplifier 2 input (10.7 MHz)
C_{offset}	9	DC feedback for offset compensation RDS mute
n.c.	10	not connected
IFAMP2DEC	11	IF amplifier 2 decoupling and AGC capacitor for AM noise blanker
IFAMP1OUT	12	IF amplifier 1 output (10.7 MHz)
n.c.	13	not connected
IFAMP1IN	14	IF amplifier 1 and AM mixer 2 input (10.7 MHz)
n.c.	15	not connected
V_{DDA6}	16	analog supply voltage 6 (8.5 V) for IF amplifier 1 and 2
IFAMP1DEC	17	AM mixer 2 and FM IF amplifier 1 decoupling
MIX1OUT1	18	FM mixer and AM mixer 1 IF output 1 (10.7 MHz)
MIX1OUT2	19	FM mixer and AM mixer 1 IF output 2 (10.7 MHz)
V_{DDA5}	20	analog supply voltage 5 (8.5 V) for FM mixer and AM mixer 1
n.c.	21	not connected
AMMIX1IN2	22	AM mixer 1 input 2
AMMIX1IN1	23	AM mixer 1 input 1
n.c.	24	not connected
n.c.	25	not connected
T1AMAGC	26	1st time constant of AM front-end AGC
T2AMAGC	27	2nd time constant of AM front-end AGC
IAMAGC	28	PIN diode drive current output of AM front-end AGC
$V_{ref(FMMIX)}$	29	reference voltage for FM I/Q mixer
FMMIXIN1	30	FM RF mixer input 1
RFGND	31	RF ground
n.c.	32	not connected
FMMIXIN2	33	FM RF mixer input 2
n.c.	34	not connected
IFMAGC	35	PIN diode drive current output of FM front-end AGC
T2FMAGC	36	2nd time constant of FM front-end AGC
T1FMAGC	37	1st time constant of FM front-end AGC
DAAOUT	38	output of digital auto alignment circuit for antenna tank circuit
DAATD	39	temperature compensation diode for digital auto alignment circuit for antenna tank circuit
DAAIN	40	input of digital auto alignment circuit for antenna tank circuit

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
V_{tune}	42	tuning voltage
CPOUT	43	charge pump output
V_{DDA4}	44	analog supply voltage 4 (8.5 V) for tuning PLL
FREF	45	reference frequency output for signal processor IC
V_{DDD}	46	digital supply voltage (5 V)
DGND	47	digital ground
VCOGND	48	VCO ground
OSCFDB	49	VCO feedback
OSCTNK	50	VCO tank circuit
V_{DDA3}	51	analog supply voltage 3 (8.5 V) for VCO
n.c.	52	not connected
AFSAMPLE	53	AF sample flag output for car audio signal processor IC
AFHOLD	54	AF hold flag output for car audio signal processor IC
TRDSMUTE	55	time constant for RDS update mute
AMAFIF2	56	AM demodulator AF output or IF2 output for AM stereo (multiplexed by I^2C-bus)
RDSMPX	57	MPX output for RDS decoder and signal processor (not muted)
FMMPX	58	FM demodulator MPX output
V_{DDA2}	59	analog supply voltage 2 (5 V) for on-chip power supply
n.c.	60	not connected
V_{DDA1}	61	analog supply voltage 1 (8.5 V) for on-chip power supply
n.c.	62	not connected
SDA	63	I^2C-bus data line input and output
SCL	64	I^2C-bus clock line input
n.c.	65	not connected
IF2GND	66	AM IF2 ground
QDET1	67	quadrature demodulator tank 1
QDET2	68	quadrature demodulator tank 2
C_{AFC}	69	FM demodulator AFC capacitor
V_{level}	70	level voltage output for AM and FM
XTAL1	71	crystal oscillator 1
XTALGND	72	crystal oscillator ground
XTAL2	73	crystal oscillator 2
n.c.	74	not connected
n.c.	75	not connected
IREF	76	reference current for power supply
AMMIX2OUT1	77	AM mixer 2 output 1 (450 kHz)
AMMIX2OUT2	78	AM mixer 2 output 2 (450 kHz)
C_{AGC}	79	AM IF AGC capacitor
n.c.	80	not connected

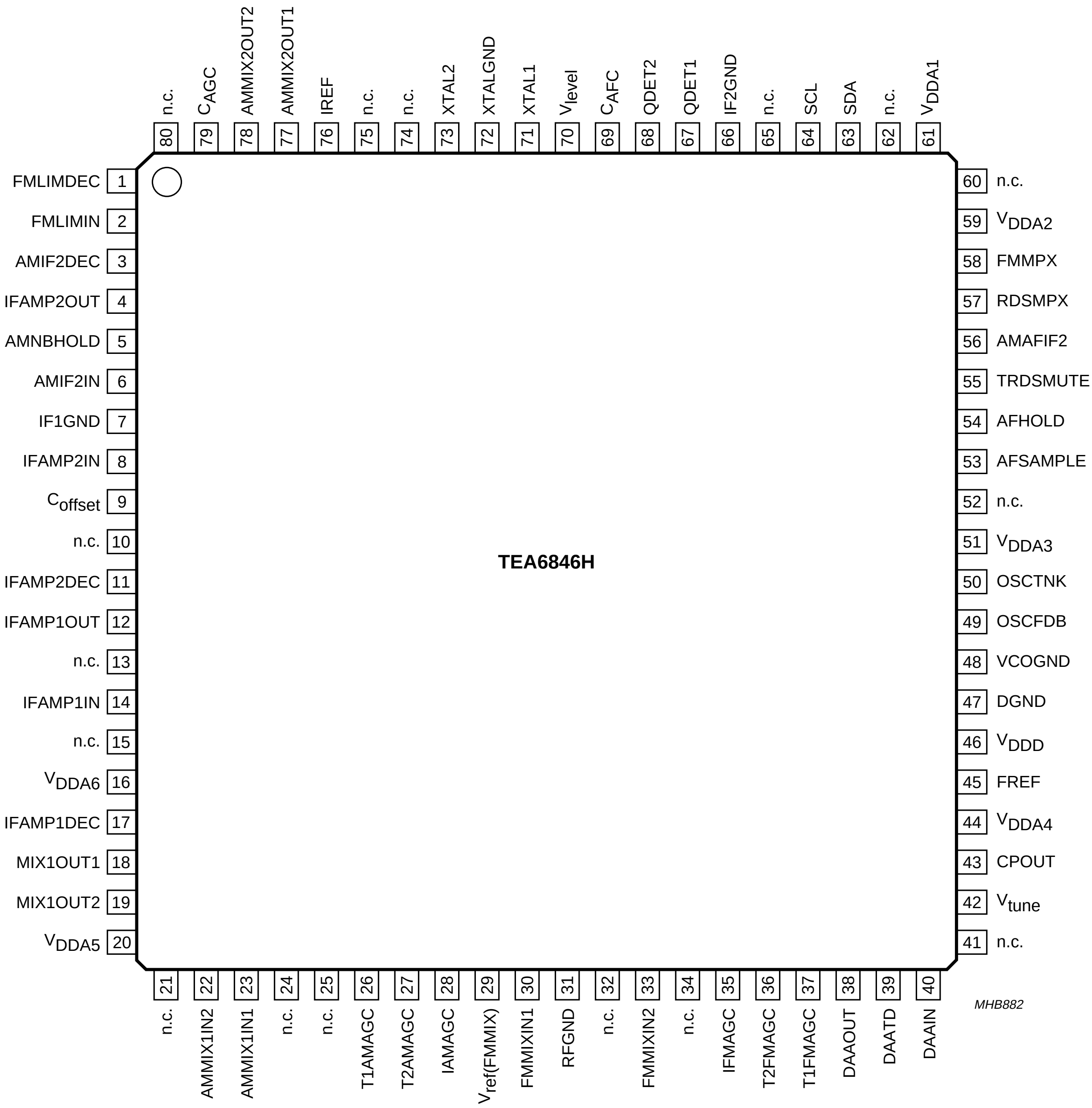


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillators

7.1.1 VCO

The L and C tuned VCO provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range of 151.2 to 248.2 MHz.

7.1.2 CRYSTAL OSCILLATOR

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.4 kHz) for the TEA688x (car audio signal processor - CASP) or TEF689x (car radio integrated signal processor - CRISP).

7.1.3 PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

7.2 FM signal channel

7.2.1 DAA

FM RF Digital Auto Alignment (DAA) circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.

7.2.2 FM I/Q MIXER

FM quadrature mixer converts FM RF (65 to 162.55 MHz) to IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands:

- US FM = 87.9 to 107.9 MHz
- US weather FM = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76.0 to 91 MHz
- East Europe FM = 65.8 to 74 MHz.

7.2.3 FM KEYED AGC

FM contains keyed wide-band RF AGC. AGC detection occurs at the FM mixer. The wide-band RF signal switches a narrow band signal (IF) from the FM IF level detector circuitry that controls the FM RF AGC block.

It includes an AGC PIN diode drive circuit for the FM RF AGC. The PIN diode drive can be activated via the I^2C-bus as a local or distance function.

The AGC threshold is programmable and the keyed AGC function is switchable via the I^2C-bus.

7.2.4 FM IF AMPLIFIERS

The two FM IF amplifiers provide 10 dB and 4 dB amplification with high linearity and dynamic range.

7.2.5 FM DEMODULATOR

The FM quadrature demodulator includes automatic centre frequency adjustment and THD compensation.

7.3 AM signal channel

7.3.1 AM TUNER INCLUDING MIXER 1 AND MIXER 2

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to IF2 of 450 kHz:

- LW = 144 to 288 kHz
- MW = 530 to 1710 kHz (US AM band)
- SW = 5.85 to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

7.3.2 AM RF AGC AND IF2 AGC

The AM RF includes a PIN diode drive circuit. The threshold detection points for AM AGC are performed at AM mixer 1 and AM IF2. AGC thresholds are programmable via the I^2C-bus.

7.3.3 AM DETECTOR

The AM detector provides AM level information and AM AF or AM IF2.

7.3.4 AM AF OR IF2 SWITCH

The AM output provides either a detected AM AF or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing.

7.3.5 AM NOISE DETECTOR AND BLANKER

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the mixer 2.

Trigger sensitivity can be modified by changing the resistor value at pin AMNBHOLD.

7.3.6 FM AND AM LEVEL DETECTOR

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I²C-bus.

7.4 Test mode

The test mode of the IC is activated by:

- Sending the test byte (byte 5) to the IC
- Connecting pin FREF through a 100 kΩ resistor to V_{DDA1}
- Applying 50 μA to pin FREF.

If the test mode is enabled by pin FREF:

- The settling time of the AM IF2 AGC is reduced to less than 100 ms in the nominal application
- The digital-to-analog converters for the antenna DAA and the level DAA can be clocked directly by the SCL line of the I²C-bus
- The output at pin FREF can be selected by the I²C-bus: TEA688x or TEF689x reference frequency, PLL reference frequency or PLL programmable divider output frequency
- The RDS update control circuit can be clocked directly via pin DAATD
- Pin T1AMAGC can be used to enable the load PLL circuit of the RDS update control circuit
- Charge pumps can be set into 3-state mode.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 for on-chip power supply		–0.3	+10	V
V_{DDA2}	analog supply voltage 2 for on-chip power supply		–0.3	+6.5	V
V_{DDA3}	analog supply voltage 3 for VCO		–0.3	+10	V
V_{DDA4}	analog supply voltage 4 for tuning PLL		–0.3	+10	V
V_{DDA5}	analog supply voltage 5 for FM and AM RF		–0.3	+10	V
V_{DDA6}	analog supply voltage 6 for IF amplifier 1 and 2		–0.3	+10	V
V_{DDD}	digital supply voltage		–0.3	+6.5	V
$\Delta V_{DD8.5\text{-}DD5}$	difference between any 8.5 V supply voltage and any 5 V supply voltage	note 1	–0.3	–	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	note 2	–200	+200	V
		note 3	–2000	+2000	V

Notes

1. To avoid damages and wrong operation it is necessary to keep all 8.5 V supply voltages at a higher level than any 5 V supply voltage. This is also necessary during power-on and power-down sequences. Precautions have to be provided in such a way that interferences can not pull down the 8.5 V supply below the 5 V supply.
2. Machine model (R = 0 Ω, C = 200 pF).
3. Human body model (R = 1.5 kΩ, C = 100 pF).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	54	K/W

10 DC CHARACTERISTICS

$V_{DDA1} = V_{DDA3} = V_{DDA4} = V_{DDA5} = V_{DDA6} = 8.5$ V; $V_{DDA2} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
$V_{DDA(n)}$	analog supply voltage 1, 3, 4, 5 and 6		8	8.5	9	V
V_{DDA2}	analog supply voltage 2		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
Supply current in FM mode						
I_{DDD}	digital supply current		18	23	28	mA
I_{DDA1}	analog supply current 1 for on-chip power supply		–	15	–	mA
I_{DDA2}	analog supply current 2 for on-chip power supply		6.5	8.1	9.8	mA
I_{DDA3}	analog supply current 3 for VCO		–	6.5	–	mA
I_{DDA4}	analog supply current 4 for tuning PLL	test mode; bit TMS3 = 1	–	2.9	–	mA
I_{DDA5}	analog supply current 5 for FM RF		–	5	–	mA
I_{DDA6}	analog supply current 6 for FM IF amplifier 1 and 2		10	12	14	mA
$I_{MIX1OUT1}$	bias current of FM mixer output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of FM mixer output 2		4.8	6	7.2	mA
Supply current in AM mode						
I_{DDD}	digital supply current		18	23	28	mA
I_{DDA1}	analog supply current 1 for on-chip power supply		–	17.5	–	mA
I_{DDA2}	analog supply current 2 for on-chip power supply		4.7	5.9	7.1	mA
I_{DDA3}	analog supply current 3 for VCO		–	6.5	–	mA
I_{DDA4}	analog supply current 4 for tuning PLL	test mode; bit TMS3 = 1	–	1.6	–	mA
I_{DDA5}	analog supply current 5 for RF		–	1.8	–	mA
$I_{MIX1OUT1}$	bias current of AM mixer 1 output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of AM mixer 1 output 2		4.8	6	7.2	mA
$I_{AMMIX2OUT1}$	bias current of AM mixer 2 output 1		3.6	4.5	5.4	mA
$I_{AMMIX2OUT2}$	bias current of AM mixer 2 output 2		3.6	4.5	5.4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
On-chip power supply reference current generator: pin IREF						
$V_{o(ref)}$	output reference voltage		4	4.25	4.5	V
R_o	output resistance		8	11	13	kΩ
$I_{o(max)}$	maximum output current		–100	–	+100	nA

11 AC CHARACTERISTICS

$V_{DDA1} = V_{DDA3} = V_{DDA4} = V_{DDA5} = V_{DDA6} = 8.5$ V; $V_{DDA2} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figs 9 and 10; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f_{osc}	oscillator frequency		151.2	–	248.2	MHz
C/N	carrier-to-noise ratio	f_{osc} = 200 MHz; Δf = 10 kHz	–	101	–	$\frac{dBc}{\sqrt{Hz}}$
RR	ripple rejection	f_{ripple} = 100 Hz; $V_{DDA3(ripple)}$ = 100 mV (RMS)				
		f_{osc} = 250 MHz	–	97	–	dB
		f_{osc} = 200 MHz	–	99	–	dB
FEEDBACK INPUT: PIN OSCFDB						
$V_{i(bias)}$	input bias voltage		2.2	2.8	3.4	V
TANK CIRCUIT OUTPUT: PIN OSCTNK						
V_O	DC output voltage		5	6.1	7.2	V
$V_{o(rms)}$	AC output voltage (RMS value)	f_{osc} = 200 MHz	–	1.5	–	V
Crystal oscillator						
f_{xtal}	crystal frequency		20.4996	20.5	20.5004	MHz
R_{xtal}	crystal motional resistance	start of operating	–	–	500	Ω
C_{xtal}	crystal shunt capacitance		–	–	18	pF
C/N	carrier-to-noise ratio	f_{xtal} = 20.5 MHz (10.25 MHz); Δf = 10 kHz	–	112	–	$\frac{dBc}{\sqrt{Hz}}$
CIRCUIT INPUTS: PINS XTAL1, XTAL2 AND XTALGND						
$V_{xtal(rms)}$	crystal voltage (RMS value)	note 1	–	350	–	mV
V_{XTAL1}, V_{XTAL2}	DC bias voltage		1.7	2.1	2.5	V
R_i	real part of input impedance	$V_{XTAL1} - V_{XTAL2}$ = 1 mV; note 1	–500	–	–	Ω
C_i	input capacitance	note 1	8	10	12	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{XTALGND}$	crystal oscillator circuit current	start-up at $V_{XTAL1} = V_{XTAL2} = 2.1$ V	–	9	–	mA
		operating at $V_{XTAL1} - V_{XTAL2} = \pm400$ mV	–	1.5	–	mA
Oscillator divider N1						
N1	oscillator divider ratio	FM mode				
		standard, Europe and local	–	2	–	
		weather band (WX)	–	1	–	
Oscillator divider N2						
N2	oscillator divider ratio	AM mode				
		LW and MW	–	10	–	
		SW	–	5	–	
Synthesizer						
PROGRAMMABLE DIVIDER						
N_{prog}	programmable divider ratio		512	–	32767	
ΔN_{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio	$f_{xtal} = 20.5$ MHz				
		$f_{ref} = 100$ kHz	–	205	–	
		$f_{ref} = 50$ kHz	–	410	–	
		$f_{ref} = 25$ kHz	–	820	–	
		$f_{ref} = 20$ kHz	–	1025	–	
		$f_{ref} = 10$ kHz	–	2050	–	
CHARGE PUMP: PIN CPOUT						
$I_{sink(cp1)l}$	low charge pump 1 peak sink current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V	200	300	400	µA
$I_{source(cp1)l}$	low charge pump 1 peak source current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V	–400	–300	–200	µA
$I_{sink(cp1)h}$	high charge pump 1 peak sink current	AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V_{CPOUT} < 7.6 V	0.7	1	1.3	mA
$I_{source(cp1)h}$	high charge pump 1 peak source current	AM stereo mode; N2 = 10 (LW and MW); 0.4 V < V_{CPOUT} < 7.6 V	–1.3	–1	–0.7	mA
$I_{sink(cp2)}$	charge pump 2 peak sink current	FM standard mode; 0.3 V < V_{CPOUT} < 7.1 V	100	130	160	µA
$I_{source(cp2)}$	charge pump 2 peak source current	FM standard mode; 0.3 V < V_{CPOUT} < 7.1 V	–160	–130	–100	µA
$I_{Z(cp1)}$, $I_{Z(cp2)}$	charge pump 1 or 2 current in 3-state	0 < V_{CPOUT} < 8.5 V	–5	–	+5	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PIN V_{tune}						
$I_{sink(cp3)}$	charge pump 3 peak sink current	FM standard mode; 0.4 V < V_{tune} < 7.6 V	2.1	3	3.9	mA
$I_{source(cp3)}$	charge pump 3 peak source current	FM standard mode; 0.4 V < V_{tune} < 7.6 V	–3.9	–3	–2.1	mA
$I_{Z(cp3)}$	charge pump 3 current in 3-state	0 < V_{tune} < 8.5 V	–5	–	+5	nA
Antenna Digital Auto Alignment (DAA)						
DAA INPUT: PIN DAAIN						
$I_{bias(cp)}$	charge pump buffer input bias current	FM mode; 0.4 V < V_{DAAIN} < 8.0 V	–10	–	+10	nA
		AM mode; 0 V < V_{DAAIN} < 8.5 V	–10	–	+10	nA
$V_{i(cp)}$	charge pump buffer input voltage		0	–	8.5	V
DAA OUTPUT: PIN DAAOUT; note 2						
$V_{o(AM)}$	DAA output voltage in AM mode		–	–	0.3	V
$V_{o(FM)}$	DAA output voltage in FM mode	V_{DAAIN} = 4.0 V; V_{DAATD} = 0.7 V				
		minimum value	–	–	0.5	V
		bits DAA[6:0] set to logic 0	1.5	1.65	1.8	V
		value: data byte 3 = 10101011	3.8	4	4.2	V
		maximum value; bits DAA[6:0] set to logic 1	8	–	8.5	V
		V_{DAAIN} = 3.0 V; V_{DAATD} = 0.7 V; bits DAA[6:0] set to logic 1	6.2	6.5	6.8	V
		V_{DAAIN} = 2 V				
		data byte 3 = 11010101	3	3.3	3.6	V
		data byte 3 = 10101010	1.8	2	2.2	V
$V_{o(n)}$	DAA output noise voltage	FM mode; V_{DAAIN} = 4 V; data byte 3: bit 6 = 1, bits 5 to 0 = 0; B = 300 Hz to 15 kHz	–	30	100	μV
$\Delta V_{o(T)}$	DAA output voltage variation with temperature	T_{amb} = –40 to +85 °C; data byte 3 = 10101011; V_{DAATD} = 0.7 V	–8	–	+8	mV
$\Delta V_{o(step)}$	DAA step accuracy	FM mode; V_{DAAOUT} < 8.0 V; n = 0 to 127	$0.5V_{LSB}$	V_{LSB}	$1.5V_{LSB}$	mV
$I_{o(sink)}$	DAA output sink current	0.2 V < V_{DAAOUT} < 8.25 V	50	–	–	μA
$I_{o(source)}$	DAA output source current		–	–	–50	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{st}	DAA output settling time	0.2 V < V_{DAAOUT} < 8.25 V; C_L = 270 pF	–	–	30	µs
RR	ripple rejection	f_{ripple} = 100 Hz; V_{DDA4} = 1 mV	–	50	–	dB
C_L	DAA output load capacitance	V_{DAAOUT} < 8.0 V; FM mode	–	–	270	pF
DAA TEMPERATURE COMPENSATION: PIN DAATD						
I_{source}	compensation diode source current	0.2 V < V_{DAATD} < 1.5 V	–50	–40	–30	µA
TC_{source}	temperature coefficient of compensation diode source current	0.2 V < V_{DAATD} < 1.5 V; T_{amb} = –40 to +85 °C	–300	–	+300	$\frac{10^{-6}}{K}$
IF counter (FM IF or AM IF2 counter)						
N_{IF}	IF counter length for AM and FM		–	8	–	bit
$T_{count(IF)}$	IF counter period	data byte 4: bit 7 = 1	–	2	–	ms
		data byte 4: bit 7 = 0	–	20	–	ms
$R_{precount}$	FM IF counter prescaler ratio	data byte 4: bit 3 = 1	–	10	–	
		data byte 4: bit 3 = 0	–	100	–	
Reference frequency for car sound processor IC; note 3						
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio		–	272	–	
f_{ref}	reference frequency	f_{xtal} = 20.5 MHz	–	75.368	–	kHz
VOLTAGE GENERATOR; PIN FREF						
$V_{o(p-p)}$	AC output voltage (peak-to-peak value)		60	100	170	mV
V_O	DC output voltage		3.2	3.4	3.9	V
R_o	output resistance		–	–	50	kΩ
$R_{L(min)}$	minimum load resistance		1	–	–	MΩ
AM signal channel						
AM RF AGC STAGE INPUTS: PINS AMMIX1IN1 AND AMMIX1IN2						
$V_{i(p)}$	RF input voltage for AGC start level (peak value)	data byte 5: bit 5 = 0, bit 6 = 0	–	150	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	275	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	400	–	mV
		data byte 5: bit 5 = 1, bit 6 = 1	–	525	–	mV
AM IF AGC STAGE INPUTS: PINS AMIF2IN AND AMIF2DEC						
$V_{i(p)}$	IF2 input voltage (peak value)	AGC start level	0.20	0.27	0.35	V
AM RF AGC CURRENT GENERATOR OUTPUT: PIN IAMAGC						
$I_{sink(max)}$	maximum AGC sink current	$V_{AMMIX1IN1}$ > 500 mV (peak value)	–	15	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_o	output resistance	I_{IAMAGC} = 1 μA	1	–	–	MΩ
C_o	output capacitance		–	5	7	pF
AM RF AGC PEAK DETECTOR: PIN T2AMAGC						
I_{att}	attack current AGC peak detector	data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input V_i = 1 V; $V_{T2AMAGC-GND}$ = 3 V; $V_{AMIF2IN-AMIF2DEC}$ = 0 V	–	–3.15	–	mA
I_{dec}	decay current AGC peak detector	data byte 5: bit 5 = 1, bit 6 = 1; AM mixer 1 input V_i = 0 V; $V_{T2AMAGC-AMMIX1IN2}$ = 0.25 V; $V_{T2AMAGC-GND}$ = 3 V; $V_{AMIF2IN-AMIF2DEC}$ = 0 V	–	2.6	–	μA
AM MIXER 1 (IF1 = 10.7 MHz)						
Mixer inputs: pins AMMIX1IN1 and AMMIX1IN2						
R_i	input resistance	note 4	50	70	100	kΩ
C_i	input capacitance	note 4	–	5	7	pF
V_I	DC input voltage		2.3	2.7	3.1	V
$V_{i(max)}$	maximum voltage on pin AMMIX1IN1	1 dB compression point of AM mixer 1 output (peak-to-peak)	500	–	–	mV
Mixer outputs: pins MIX1OUT1 and MIX1OUT2						
R_o	output resistance	note 5	100	–	–	kΩ
C_o	output capacitance	note 5	–	5	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		12	15	–	V
I_{bias}	mixer bias current	AM mode	4.8	6	7.2	mA
Mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{MIX1OUT1}}{V_{FMMIXIN1-FMMIXIN2}}$		2.0	2.55	3.2	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	-9×10^{-4}	–	K^{-1}
IP3	3rd-order intermodulation	R_L = 2.8 kΩ (AC load between output pins)	135	138	–	dBμV
IP2	2nd-order intermodulation	R_L = 2.8 kΩ (AC load between output pins)	–	170	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(n)(eq)}$	equivalent input noise voltage	band limited noise; R_{gen} = 750 Ω; R_L = 2.8 kΩ (AC load between output pins)	–	5.8	–	$\frac{nV}{\sqrt{Hz}}$
F	noise figure of AM mixer 1		–	4.5	7.1	dB
WEATHER BAND FLAG: PIN T1AMAGC						
$I_{L(max)}$	maximum load current		–5	–	+5	μA
$V_{o(max)}$	maximum output voltage for FM mode	measured with respect to pin RFGND	0	–	0.5	V
$V_{o(min)}$	minimum output voltage for WX mode	measured with respect to pin RFGND	5.1	6.0	6.9	V
AM MIXER 2 (IF2 = 450 kHz)						
Mixer inputs: pins IFAMP1IN and IFAMP1DEC						
R_i	input resistance	note 6	270	330	390	Ω
C_i	input capacitance	note 6	–	5	7	pF
V_I	DC voltage		2.4	2.7	3	V
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of AM mixer 2 output (peak-to-peak)	1.1	–	–	V
Mixer outputs: pins AMMIX2OUT1 and AMMIX2OUT2						
R_0	output resistance	note 7	100	–	–	kΩ
C_o	output capacitance	note 7	–	5	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)	V_{DDA} = 8.5 V	12	15	–	V
I_{bias}	mixer bias current	AM mode	3.6	4.5	5.4	mA
Mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{AMMIX2OUT1}}{V_{IFAMP1IN}}$		1.3	1.6	1.9	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	-9×10^{-4}	–	K^{-1}
IP3	3rd-order intermodulation	R_L = 4 kΩ (AC load between output pins)	134	137	–	dBμV
IP2	2nd-order intermodulation	R_L = 4 kΩ (AC load between output pins)	–	170	–	dBμV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 4 kΩ (AC load between output pins)	–	15	22	$\frac{nV}{\sqrt{Hz}}$
F	noise figure of AM mixer 2		–	16	19.5	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AM IF2 AGC STAGE: PINS AMIF2IN AND AMIF2DEC; note 8						
V_i	input voltage	for α = −10 dB audio attenuation				
		AM soft mute on	–	75	120	μV
		AM soft mute off	–	6	10	μV
$V_{AGC(start)}$	AGC start voltage	input carrier voltage	–	14	30	μV
$V_{AGC(stop)}$	AGC stop voltage	maximum input peak voltage	1	–	–	V
$V_{AGC(ctrl)}$	AGC control voltage	V_i = 1 mV	4.1	4.3	4.7	V
ΔAGC	AGC range	between start and stop of AGC; m = 0.8	–	89	–	dB
R_i	input resistance		1.8	2	2.2	kΩ
C_i	input capacitance		–	–	5	pF
AM DETECTOR						
$V_{sens(rms)}$	sensitivity voltage (RMS value)	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.5 kHz; R_{gen} = 2 kΩ; note 8				
		(S+N)/N = 26 dB	–	45	65	μV
		(S+N)/N = 46 dB	–	600	900	μV
(S+N)/N	maximum signal plus noise-to-noise ratio	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.5 kHz; R_{gen} = 2 kΩ	54	60	–	dB
THD	total harmonic distortion	B_{AF} = 2.5 kHz; C_{AGC} = 22 μF; AM IF2 AGC input V_i = 100 μV to 500 mV (RMS)				
		m = 0.8; f_{mod} = 400 Hz	–	0.5	1	%
		m = 0.9; f_{mod} = 400 Hz	–	1	2	%
		m = 0.8; f_{mod} = 100 Hz	–	1.25	2.5	%
		m = 0.9; f_{mod} = 100 Hz	–	1.75	3.5	%
RR	ripple rejection	$V_{DDA2(ripple)}$ = 100 mV (RMS); f_{ripple} = 100 Hz	30	40	–	dB
t_{sw}	FM to AM switching time	C_{AGC} = 22 μF	–	1000	1500	ms
t_{settle}	AM AGC settling time	C_{AGC} = 22 μF				
		normal operation	–	–	1800	ms
		test mode	–	–	180	ms
Output: pin AMAFIF2						
$V_{o(rms)}$	AM IF2 output voltage (RMS value)	AM stereo; m = 0				
		minimum at V_i = 14 μV	1.5	3	4.5	mV
		maximum at V_i = 5.0 mV	130	180	230	mV
		AM mono; m = 0.3; f_{mod} = 400 Hz; V_i = 100 μV to 500 mV (RMS)	240	290	340	mV
R_o	output resistance	AM stereo	–	–	500	Ω
		AM mono	–	–	500	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_o	output capacitance	AM mono	–	5	7	pF
AM IF2 LEVEL DETECTOR OUTPUT: PIN V_{level}; see Fig.3						
V_{level}	DC output voltage	V_i = 10 µV to 1 V	0	–	7	V
		V_i < 1 µV; standard setting of level DAA and level slope	0.1	0.5	0.9	V
		V_i = 1.4 mV; standard setting of level DAA	1.6	2.2	2.8	V
ΔV_{level}	step size for adjustment of level starting point	standard setting of level slope	30	40	50	mV
$V_{level(slope)}$	slope of level voltage	standard setting of level slope	650	800	950	$\frac{mV}{20\ dB}$
ΔV_{step}	step size for adjustment of level slope	V_i =1.4 mV	45	60	75	$\frac{mV}{20\ dB}$
B_{level}	bandwidth of level output voltage		200	300	–	kHz
R_o	output resistance		–	–	500	Ω
RR	ripple rejection	$V_{DDA1(ripple)}$ = 100 mV (RMS); f_{ripple} = 100 Hz	–	40	–	dB
AM NOISE BLANKER; see Fig.4						
Threshold: pin AMNBHOLD						
V_O	DC output voltage		4.3	4.6	5.1	V
t_{sup}	suppression time		6	7.5	10	µs
$f_{trigger}$	trigger sensitivity frequency	V_{pulse} = 200 mV (peak); V_{level} < 1.8 V	–	1000	–	Hz
		V_{pulse} = 200 mV (peak); V_{level} > 2.2 V	–	–	100	Hz
		V_{pulse} = 20 mV (peak); V_{level} < 1.8 V	–	–	100	Hz
Noise detector output: pin TRDSMUTE						
$I_{sink(AGC)}$	AM noise blanker AGC sink current	$V_{TRDSMUTE}$ = 3 V	35	50	65	µA
V_{AGC}	AM noise blanker AGC voltage	AM mixer 1 input V_i = 0 V	1.9	2.2	2.5	V
FM signal channel						
FM RF AGC						
Inputs: pins FMMIXIN1 and FMMIXIN2; note 9						
$V_{i(RF)(rms)}$	RF input voltage for start of wide-band AGC (RMS value)	data byte 5: bit 5 = 0, bit 6 = 0	–	4	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	8	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	12	–	mV
		data byte 5: bit 5 = 1, bit 6 = 1	–	16	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AGC peak detector output: pin T1FMAGC						
I_{ch}	charge current		–350	–600	–850	μA
I_{dch}	discharge current		15	25	35	μA
PIN diode drive output: pin IFMAGC						
I_{drive}	drive current	V_o = 0.5 to 4.0 V	8	11.5	15	mA
Level voltage output: pin V_{level}						
V_{th}	threshold voltage for narrow-band AGC	data byte 5: bit 7 = 1; standard setting of level DAA	500	950	1400	mV
FM RF MIXER						
Reference voltage: pin $V_{ref(FMMIX)}$						
V_{ref}	reference voltage	FM mode	6.5	7.1	7.9	V
		AM mode	2.7	3.1	3.4	V
Inputs: pins FMMIXIN1 and FMMIXIN2; note 9						
$V_{i(RF)(max)}$	maximum RF input voltage	1 dB compression point of FM mixer output voltage (peak-to-peak value)	70	100	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 600 Ω; R_L = 2.8 kΩ	–	2.6	3.1	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		–	1.4	–	kΩ
C_i	input capacitance		–	5	7	pF
Outputs: pins MIX1OUT1 and MIX1OUT2; note 5						
R_o	output resistance		100	–	–	kΩ
C_o	output capacitance		–	5	7	pF
I_{bias}	mixer bias current	FM mode	4.8	6	7.2	mA
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		3	–	–	V
FM mixer						
$g_{m(conv)}$	conversion transconductance		8.5	12.5	18	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature		–	-1×10^{-3}	–	K^{-1}
F	noise figure		–	3	4.6	dB
IP3	3rd-order intermodulation		116	119	–	dBμV
IRR	image rejection ratio		25	30	–	dB
IF AMPLIFIER 1						
G	gain	R_L = 330 Ω; V_i = 1 mV; note 10	13.5	15.5	17.5	dB
F	noise figure		–	10	13	dB
IP3	3rd-order intermodulation		117	120	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs: pins IFAMP1IN and IFAMP1DEC; note 10						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 1 output voltage (peak value)	200	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 330 Ω	–	8	10	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		–	5	7	pF
Output: pin IFAMP1OUT						
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
R_o	output resistance		270	330	390	Ω
C_o	output capacitance		–	5	7	pF
IF AMPLIFIER 2						
G	gain	R_L = 330 Ω; V_i = 1 mV; note 11	6.5	8.5	10.5	dB
F	noise figure		–	13	15	dB
IP3	3rd-order intermodulation		127	130	–	dBμV
Inputs: pins IFAMP2IN and IFAMP2DEC; note 11						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 2 output voltage (peak value)	500	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 330 Ω	–	10	13	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		–	5	7	pF
Output: pin IFAMP2OUT						
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
R_o	output resistance		270	330	390	Ω
C_o	output capacitance		–	5	7	pF
FM demodulator and level detector; see Figs 5 and 6						
FM LIMITER						
Inputs: pins FMLIMIN and FMLIMDEC; note 12						
G	gain	R_{gen} = 50 Ω	74	80	–	dB
R_i	input resistance		270	330	390	kΩ
C_i	input capacitance		–	5	7	pF
Outputs: pins QDET1 and QDET2						
$V_{o(p-p)}$	output voltage (peak-to-peak value)	measured between output pins	500	700	–	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM DEMODULATOR						
R_L	load resistance		20	–	–	kΩ
C_L	load capacitance		–	–	50	pF
FM limiter inputs: pins FMLIMIN and FMLIMDEC; note 12						
$V_{start(lim)(rms)}$	start of limiting of MPX output voltage (RMS value)	α_{AF} = –3 dB	–	10	15	μV
$V_{o(sens)(rms)}$	sensitivity for MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs				
		(S+N)/N = 26 dB	–	10	15	μV
		(S+N)/N = 46 dB	–	50	75	μV
RDS MPX output: pin RDSMPX						
$V_{o(rms)}$	RDS MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 57 kHz; V_i = 20 μV to 1 V; note 12	180	230	280	mV
$I_{o(max)}$	maximum RDS MPX output current		–	–	100	μA
R_o	output resistance		–	–	500	Ω
B	bandwidth RDS MPX output	C_L = 0; R_L > 20 kΩ	200	300	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 100 Hz to 20 kHz	–	40	–	dB
FM MPX output: pin FMMPX; note 12						
$V_{o(rms)}$	MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; V_i = 20 μV to 1 V	180	230	280	mV
α_{AM}	AM suppression of MPX output	Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; de-emphasis = 75 μs				
		V_i = 500 μV to 300 mV	50	60	–	dB
		V_i = 20 to 500 μV	–	40	–	dB
		V_i = 300 mV to 1 V	–	40	–	dB
$I_{o(max)}$	maximum MPX output current		–	–	100	μA
(S+N)/N	maximum signal plus noise-to-noise ratio of MPX output voltage	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; V_i = 10 mV	67	70	–	dB
THD	total harmonic distortion of MPX output voltage	Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; V_i = 200 μV to 800 mV	–	0.35	0.7	%
B	bandwidth MPX output	C_L = 0; R_L > 20 kΩ	200	–	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 100 Hz to 20 kHz	–	40	–	dB
$R_{L(min)}$	minimum load resistance		20	–	–	kΩ

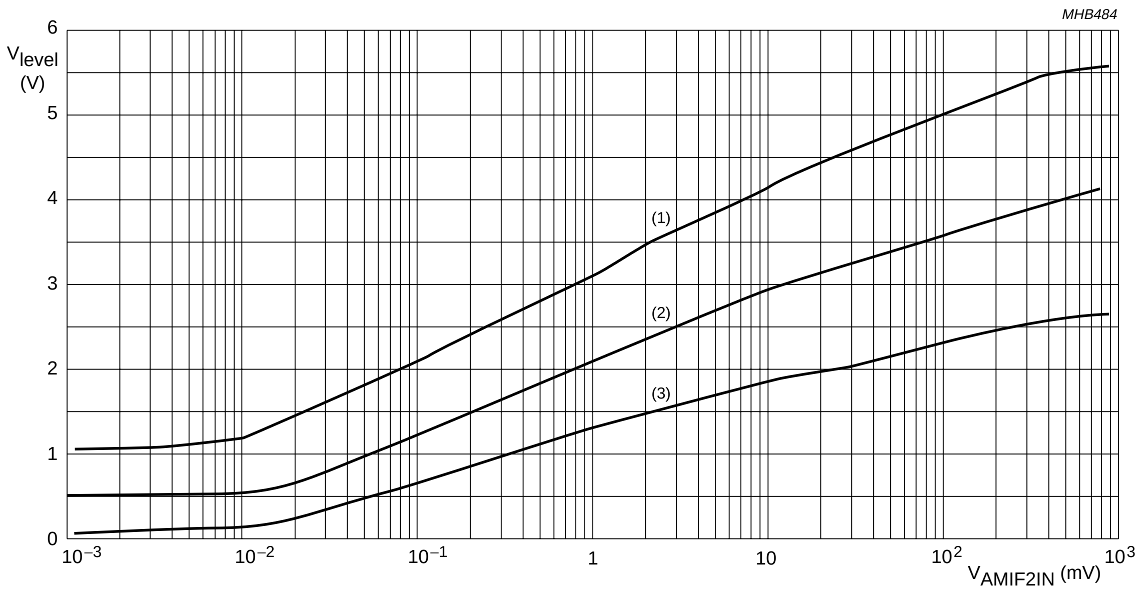
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{o(max)}$	maximum output resistance		–	–	500	Ω
$C_{L(max)}$	maximum load capacitance		–	–	50	pF
MPX MUTE						
α_{mute}	muting depth	during RDS update	60	80	–	dB
t_{att}	attack time MPX mute	$C_{TRDSMUTE}$ = 10 nF	0.75	1	1.25	ms
t_{decay}	decay time MPX mute	$C_{TRDSMUTE}$ = 10 nF	0.75	1	1.25	ms
RDS update: pin TRDSMUTE						
I_{dch}	discharge current	V_o = 3 V; audio output muted	24	32	38	μA
I_{ch}	charge current	V_o = 3 V; audio output not muted	–38	–32	–24	μA
DEMODULATOR AFC						
G_{AFC}	AFC gain	Δf = 100 kHz	28	32	–	dB
RDS MPX output: pin RDSMPX; note 12						
$V_{offset(DC)}$	residual DC offset voltage	L_{demod} = typical value				
		V_i = 10 to 80 μV	–	0.1	1	V
		V_i = 80 μV to 800 mV	–	10	30	mV
		L_{demod} = ±6%				
		V_i = 10 to 80 μV	–	0.240	1	V
		V_i = 80 μV to 800 mV	–	25	500	mV
FM IF LEVEL DETECTOR OUTPUT: PIN V_{level}; note 12						
V_{level}	DC output voltage	V_i = 10 μV to 1 V	0	–	7	V
		V_i < 1 μV; standard setting of level DAA	0.2	0.6	1.1	V
		V_i = 1 mV; standard setting of level DAA	1.4	1.9	2.5	V
ΔV_{level}	level starting point for adjustment of step size	standard setting of level slope	30	40	50	mV
$V_{level(slope)}$	slope of level voltage	standard setting of level slope	650	800	950	$\frac{mV}{20\ dB}$
ΔV_{step}	level slope adjustment of step size	V_i = 1 mV	45	50	75	$\frac{mV}{20\ dB}$
B_{level}	bandwidth of level output voltage	V_i = 10 mV; f_{mod} = 22.5 kHz; standard setting of level DAA	200	300	–	kHz
R_o	output resistance		–	–	500	Ω
RR	ripple rejection	$V_{DDA1(ripple)}$ = 100 mV (RMS); f_{ripple} = 100 Hz	–	40	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RDS update						
Output: pin AFHOLD						
$I_{sink(max)}$	maximum sink current	after first bus transmission with AF = 1 (start of RDS update); V_o = 0.5 V	1.0	1.2	1.4	mA
Output: pin AFSAMPLE						
$I_{sink(max)}$	maximum sink current	no RDS update in progress; V_o = 0.5 V	1.0	1.2	1.4	mA
Test mode; note 3						
Temperature compensation diode: pin DAATD						
$V_{i(ext)}$	external input voltage to clock state machine	$V_{DAATD(L)}$ = 2.5 V; $V_{DAATD(H)}$ = 3.5 V	2.5	–	3.5	V
Clock input: pin SCL						
$V_{i(ext)}$	external input voltage to clock DAA	$V_{SCL(L)}$ = 0 V; $V_{SCL(H)}$ = 5 V	0	–	5	V
Time constant output: pin T1AMAGC						
V_{pulse}	enabling voltage of load PLL signal	pin FREF in test mode	5.1	6	6.9	V

Notes

1. Measured between pins XTAL1 and XTAL2.
2. DAA conversion gain formula: $V_{DAAOUT} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.25\right) \times (V_{DAAIN} + V_{DAATD})\right] - V_{DAATD}$

   where n = 0 to 127.
3. Reference frequency pin FREF:
   a) R_{ext} = 68 kΩ connected to ground activates the 2nd I^2C-bus address
   b) R_{ext} = 100 kΩ connected to V_{DDA1} sets the IC into test mode.
4. Input parameters of AM mixer 1 measured between pins AMMIX1IN1 and AMMIX1IN2.
5. Output parameters of FM mixer and AM mixer 1 measured between pins MIX1OUT1 and MIX1OUT2.
6. Input parameters of AM mixer 2 measured between pins IFAMP1IN and IFAMP1DEC.
7. Output parameters of AM mixer 2 measured between pins AMMIX2OUT1 and AMMIX2OUT2.
8. Input parameters of AM IF2 measured between pins AMIF2IN and AMIF2DEC.
9. Input parameters of FM mixer measured between pins FMMIXIN1 and FMMIXIN2.
10. Input parameters of IF amplifier 1 measured between pins IFAMP1IN and IFAMP1DEC.
11. Input parameters of IF amplifier 2 measured between pins IFAMP2IN and IFAMP2DEC.
12. Input parameters of FM limiter measured between pins FMLIMIN and FMLIMDEC.

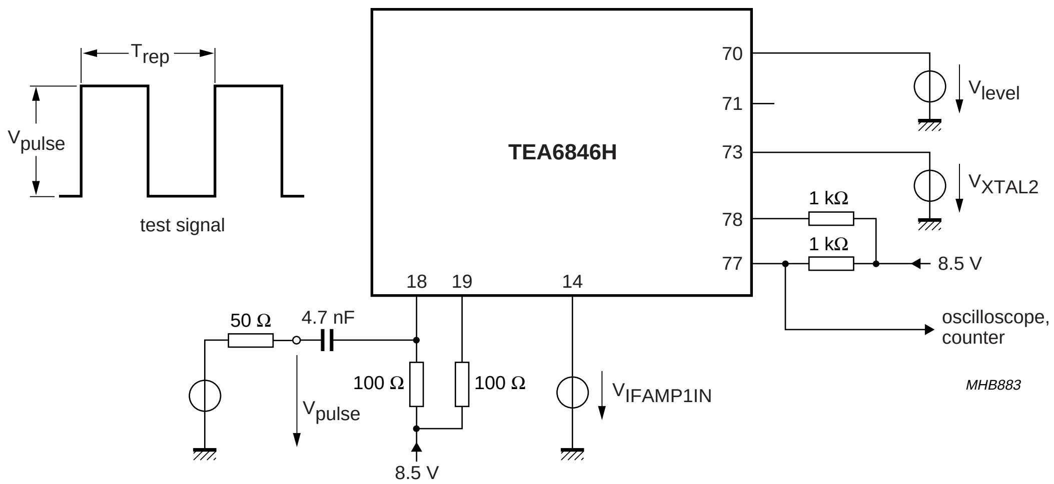


(1) Level DAA setting byte 6 = FFH.

(2) Level DAA setting byte 6 = 84H (standard setting).

(3) Level DAA setting byte 6 = 00H.

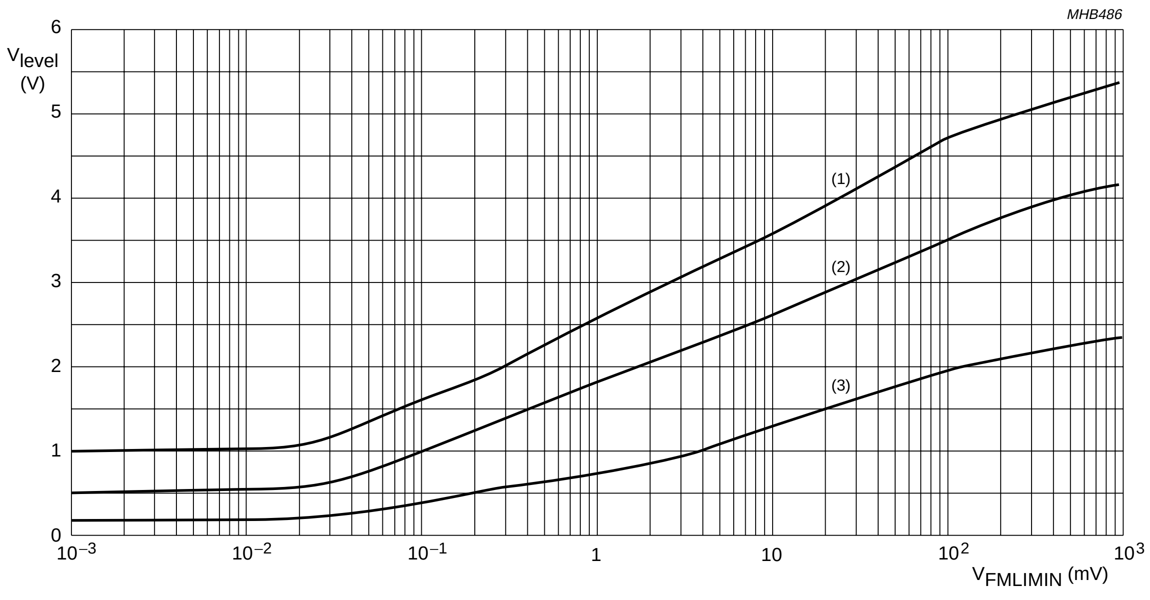
Fig.3 AM level output voltage (DAA) as a function of AM level circuit input voltage.



Test signal: T_{rep} = 2 ms, t_r < 50 ns, t_f < 50 ns and duty factor 50%.

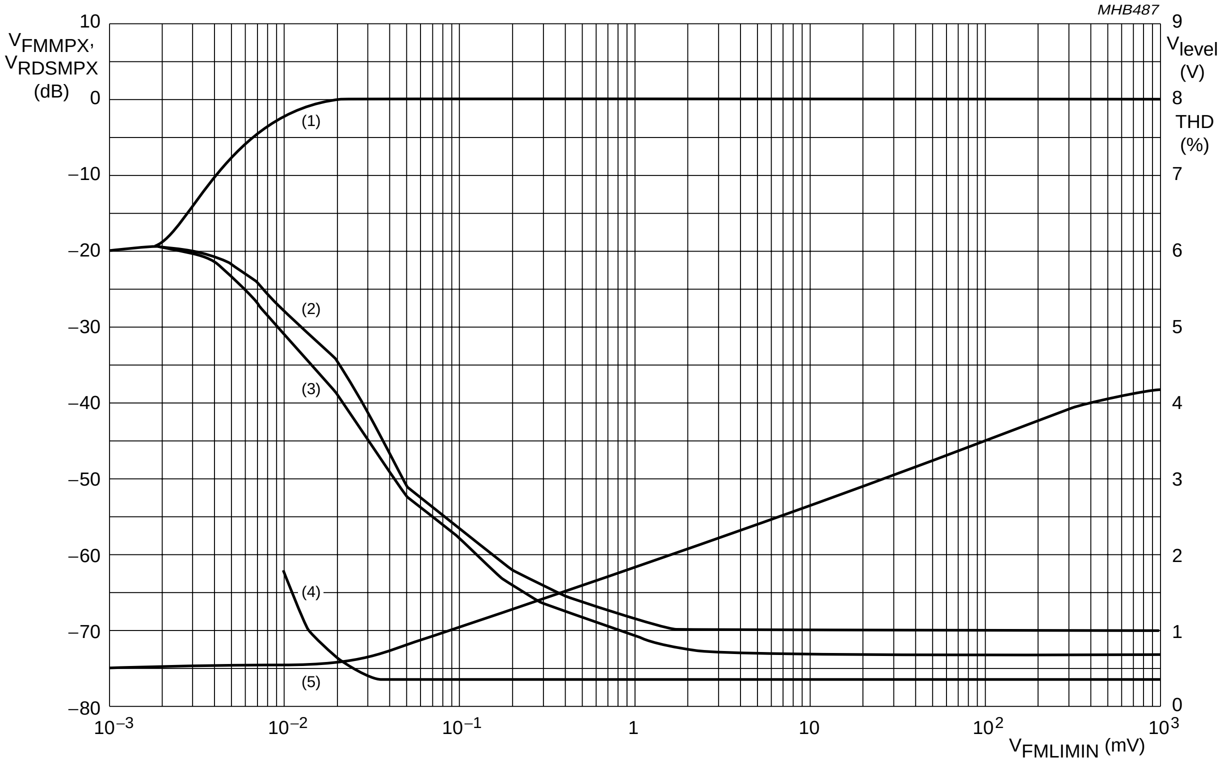
$V_{IFAMP1IN}$ = 4 V.
V_{XTAL2} = 3 V.

Fig.4 Test circuit for AM noise blanker.



(1) Level DAA setting byte 6 = FFH.
(2) Level DAA setting byte 6 = 84H (standard setting).
(3) Level DAA setting byte 6 = 00H.

Fig.5 FM level output voltage (DAA) as a function of FM limiter and level circuit input voltage.



(1) Output voltage for FMMPX and RDSMPX: f_{IF} = 10.7 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz.

(2) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 µs for FMMPX.

(3) Noise: unweighted B = 250 Hz to 15 kHz with de-emphasis 50 µs for RDSMPX.

(4) THD for FMMPX and RDSMPX.

(5) Level for standard setting of level DAA, byte 6 = 84H.

Fig.6 (S+N)/N, THD and level output voltage for FM mode as a function of FM demodulator input voltage.

12 I²C-BUS PROTOCOL

12.1 I²C-bus specification

Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

The standard I²C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2: 1100001
- 2nd IC address C0: 1100000.

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

Exception to the standard I²C-bus specification:

- The data hold time $t_{HD;DAT}$ must be at least 1 μs.

12.1.1 TEST MODE

Connecting pin FREF to V_{DDA1} via a 100 kΩ resistor or feeding 50 μA into that pin switches the IC into the test mode.

During test mode the digital-to-analog converters of the level and antenna DAA functions can be sequenced by the I²C-bus SCL line.

During test mode either the TEA688x or TEF689x reference frequency, the PLL reference frequency divider or the programmable divider output can be switched to pin FREF.

12.1.2 DATA TRANSFER

Data sequence: address, byte 1, byte 2, byte 3, byte 4, byte 5, and byte 6. The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6846H.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

In byte 5, 4 bits are reserved for test mode purposes. Those can only be used when the test mode is activated by the select pin FREF.

12.1.3 I²C-BUS PULL-UP RESISTORS

When the IC is used together with the TEA688x or TEF689x and both SCL and SDA lines are connected via the I²C-bus to the TEA688x or TEF689x, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA688x or TEF689x. Otherwise an I²C-bus pull-down can occur switching off the tuner IC supply when the I²C-bus buffer interface of the TEA688x or TEF689x is enabled for data transfer to the tuner IC.

12.1.4 FREQUENCY SETTING

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit MUTE = 1. To select an FM frequency, two I²C-bus transmissions are necessary:

- First: bit MUTE = 1
- Second: bit MUTE = 0.

12.2 I²C-bus protocol

12.2.1 DATA TRANSFER MODE AND IC ADDRESS

Table 1 Write mode

S[(1)]	address (write)	A[(2)]	data byte(s)	A[(2)]	P[(3)]

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

S[(1)]	address (read)	A[(2)]	data byte 1

Notes

1. S = START condition.
2. A = acknowledge.

Table 3 IC address byte

IC ADDRESS							MODE
1	1	0	0	0	0	0/1[(1)]	R/$\overline{W}$[(2)]

Notes

1. Defined by address pin FREF:
   a) 1 = 1st IC address
   b) 0 = 2nd IC address.
2. Read or write mode:
   a) 0 = write operation to TEA6846H
   b) 1 = read operation from TEA6846H.

12.2.2 WRITE MODE: DATA BYTE 1

Table 4 Format of data byte 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AF	PCA6	PCA5	PCA4	PCA3	PCA2	PCA1	PCA0

Table 5 Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7	AF	**Alternative frequency.** If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PCA[6:0]	**Setting of programmable counter of synthesizer PLL.** Upper byte of PLL divider word.

12.2.3 WRITE MODE: DATA BYTE 2

Table 6 Format of data byte 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PCB7	PCB6	PCB5	PCB4	PCB3	PCB2	PCB1	PCB0

Table 7 Description of data byte 2 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PCB[7:0]	**Setting of programmable counter of synthesizer PLL.** Lower byte of PLL divider word.

12.2.4 WRITE MODE: DATA BYTE 3

Table 8 Format of data byte 3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MUTE	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

Table 9 Description of data byte 3 bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	**FM audio mute.** If MUTE = 0, then FM audio not muted. If MUTE = 1, then FM audio muted; writing to programmable divider enabled.
6 to 0	DAA[6:0]	**Setting of antenna digital auto alignment.**

12.2.5 WRITE MODE: DATA BYTE 4

Table 10 Format of data byte 4

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFMT	RFS2	RFS1	RFS0	IFPR	BND1	BND0	AMFM

Table 11 Description of data byte 4 bits

BIT	SYMBOL	DESCRIPTION
7	IFMT	**IF measuring time.** If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms.
6 to 4	RFS[2:0]	**Reference frequency for synthesizer.** These 3 bits determine the reference frequency, see Table 12.
3	IFPR	**IF counter prescaler ratio.** If IFPR = 0, then IF prescaler ratio is 100. If IFPR = 1, then IF prescaler ratio is 10.
2 and 1	BND[1:0]	**Band switch.** These 2 bits select in FM mode band and local or distant, see Table 13; in AM mode band and AM stereo, see Table 14.
0	AMFM	**AM or FM switch.** If AMFM = 0, then FM mode. If AMFM = 1, then AM mode

Table 12 Reference frequency setting

RFS2	RFS1	RFS0	f_{ref} (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

Table 13 FM mode

BND1	BND0	SELECTION
0	0	FM standard: dead zone high current charge pump active, FM AGC defined by RF level and threshold level setting by I^2C-bus
0	1	FM local: dead zone high current charge pump active, FM AGC source current set to maximum
1	0	FM East Europe: dead zone high current charge pump switched off, current of low current charge pump set to 1 mA
1	1	FM weather band: N1 divider set to 1 and I and Q phase shift network switched on, WX flag signal activated

Table 14 AM mode; note 1

BND1	BND0	SELECTION
0	0	AM mono; N2 divider set to 5 (SW)
0	1	AM stereo; N2 divider set to 5 (SW)
1	0	AM mono; N2 divider set to 10 (LW, MW)
1	1	AM stereo; N2 divider set to 10 (LW, MW)

Note

1. In AM mode dead zone high current charge pump switched off, current of low current charge pump set to 1 mA.

12.2.6 WRITE MODE: DATA BYTE 5

Table 15 Format of data byte 5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
KAGC	WBA1	WBA0	AMSM	TMS3	TMS2	TMS1	TMS0

Table 16 Description of data byte 5 bits

BIT	SYMBOL	DESCRIPTION
7	KAGC	**Keyed FM AGC.** If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	WBA[1:0]	**Wide band AGC.** These 2 bits set the start value of wide band AGC. For AM, see Table 17 and for FM, see Table 18.
4	AMSM	**AM soft mute.** If AMSM = 0, then AM soft mute is off. If AMSM = 1, then AM soft mute is on.
3	TMS3	**In test mode charge pump 3-state.** If TMS3 = 0, then 3-state off. If TMS3 = 1, then 3-state on.
2	TMS2	**In test mode external clock for level and antenna DAA.** If TMS2 = 0, then external clock disabled. If TMS2 = 1, then external clock enabled.
1 and 0	TMS[1:0]	**In test mode setting of pin FREF.** These 2 bits define the function of pin FREF, see Table 19.

Table 17 Setting of wide band AGC for AM

WBA1	WBA0	AM MIXER 1 INPUT VOLTAGE (PEAK VALUE) (mV)
0	0	150
0	1	275
1	0	400
1	1	525

Table 18 Setting of wide band AGC for FM

WBA1	WBA0	FM RF MIXER INPUT VOLTAGE (RMS VALUE) (mV)
1	1	4
1	0	8
0	1	12
0	0	16

Table 19 Setting function of pin FREF in test mode

TMS1	TMS0	OUTPUT AT PIN FREF
0	0	reference frequency of TEA688x or TEF689x
0	1	tuner oscillator frequency divided by division ratio of programmable divider
1	0	PLL synthesizer reference frequency
1	1	not used (no output)

12.2.7 WRITE MODE: DATA BYTE 6

Table 20 Format of data byte 6

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

Table 21 Description of data byte 6 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	LST[4:0]	**Setting of level DAA starting point.** These 5 bits determine the offset of the level detector output voltage.
2 to 0	LSL[2:0]	**Setting of level DAA slope.** These 3 bits determine the steepness of the level detector output voltage.

Table 22 Standard setting of data byte 6 bits

SETTING OF LEVEL DAA STARTING POINT					SETTING OF LEVEL DAA SLOPE		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

12.2.8 READ MODE: DATA BYTE 1

Table 23 Format of 1st data byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

Table 24 Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	IFC[7:0]	**IF counter result.** These bits contain the last eight bits of the IF counter result.

13 TEST AND APPLICATION INFORMATION

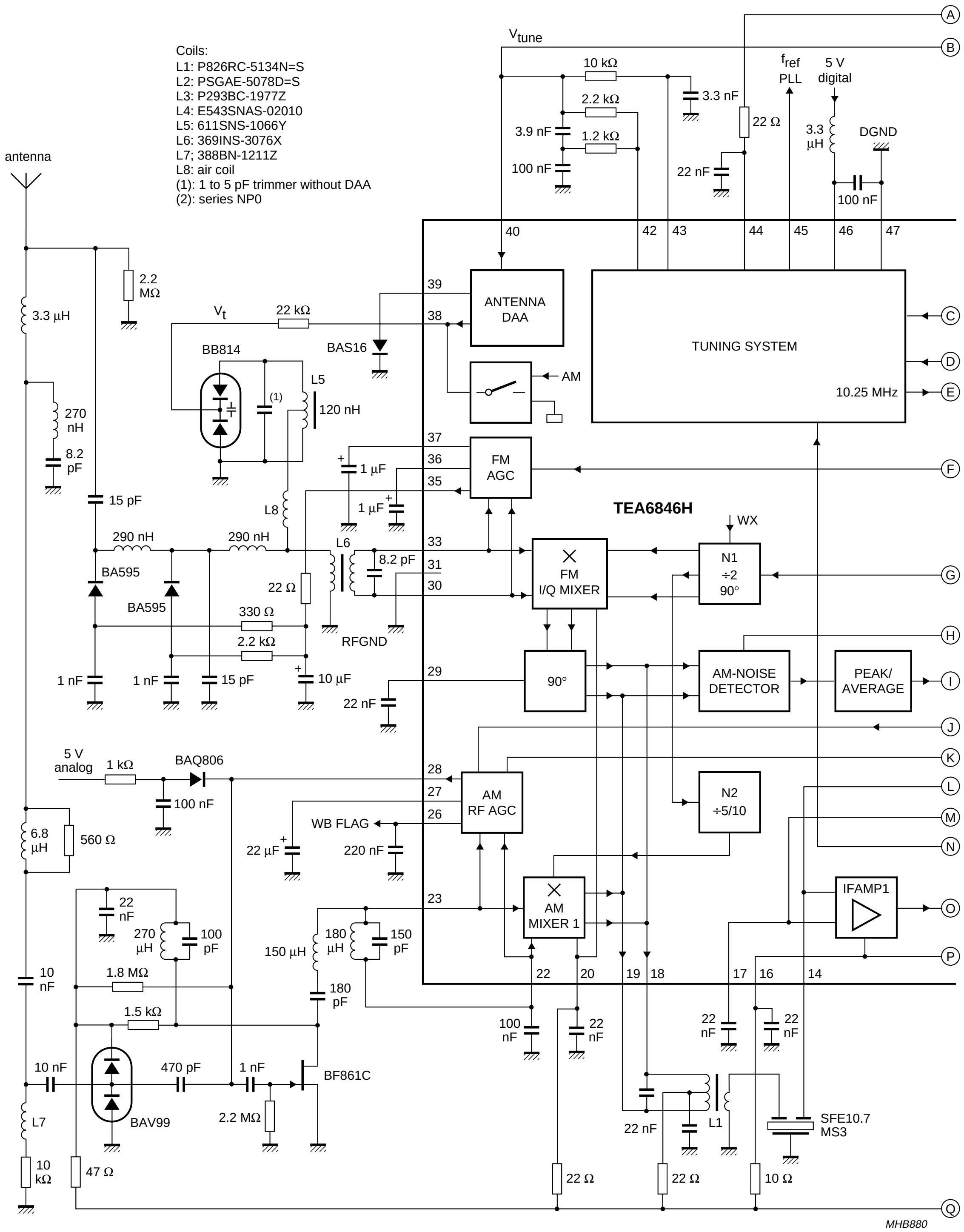


Fig.7 Application diagram (continued in Fig.8).

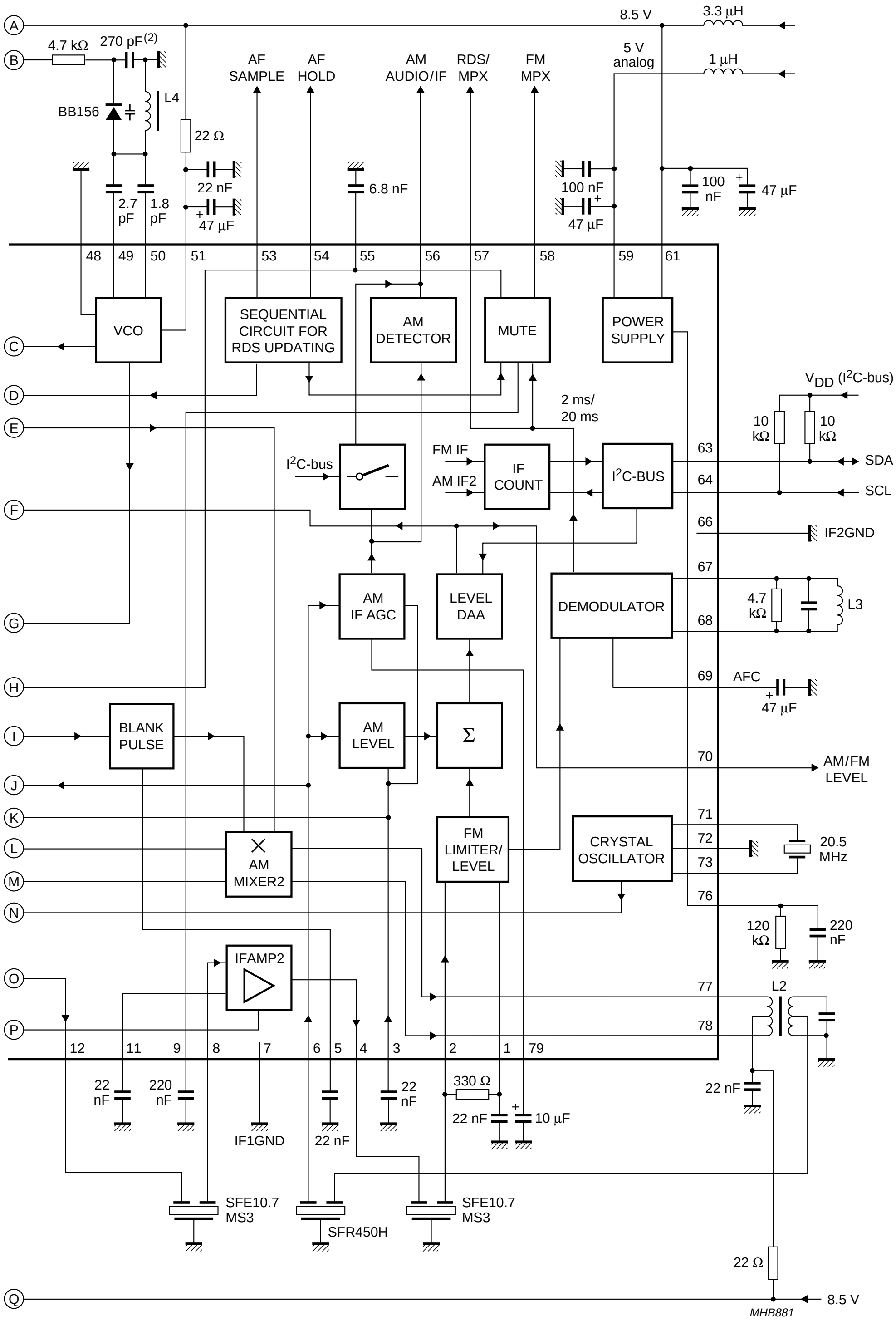


Fig.8 Application diagram (continued from Fig.7).

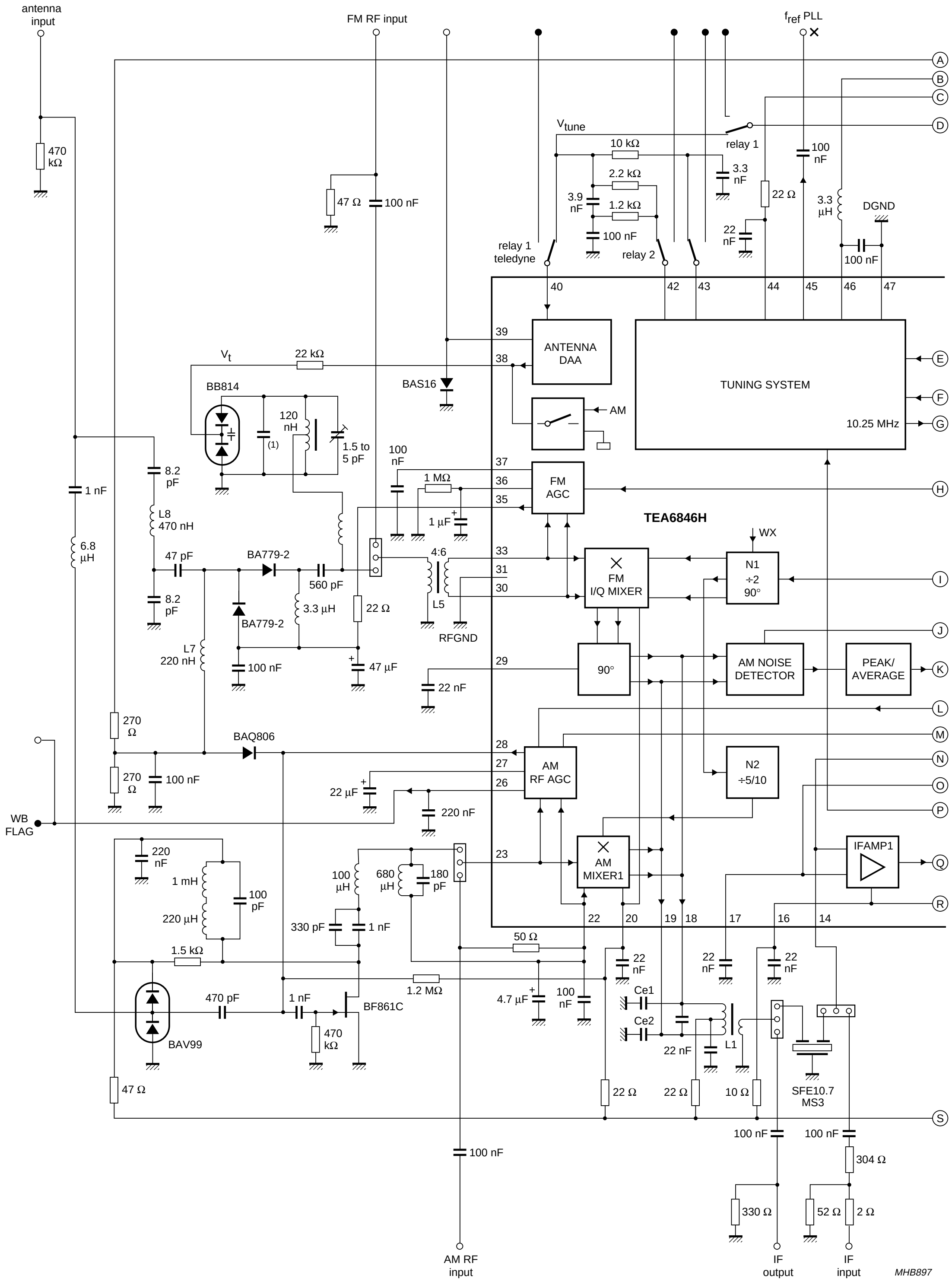


Fig.9 Test circuit (continued in Fig.10).

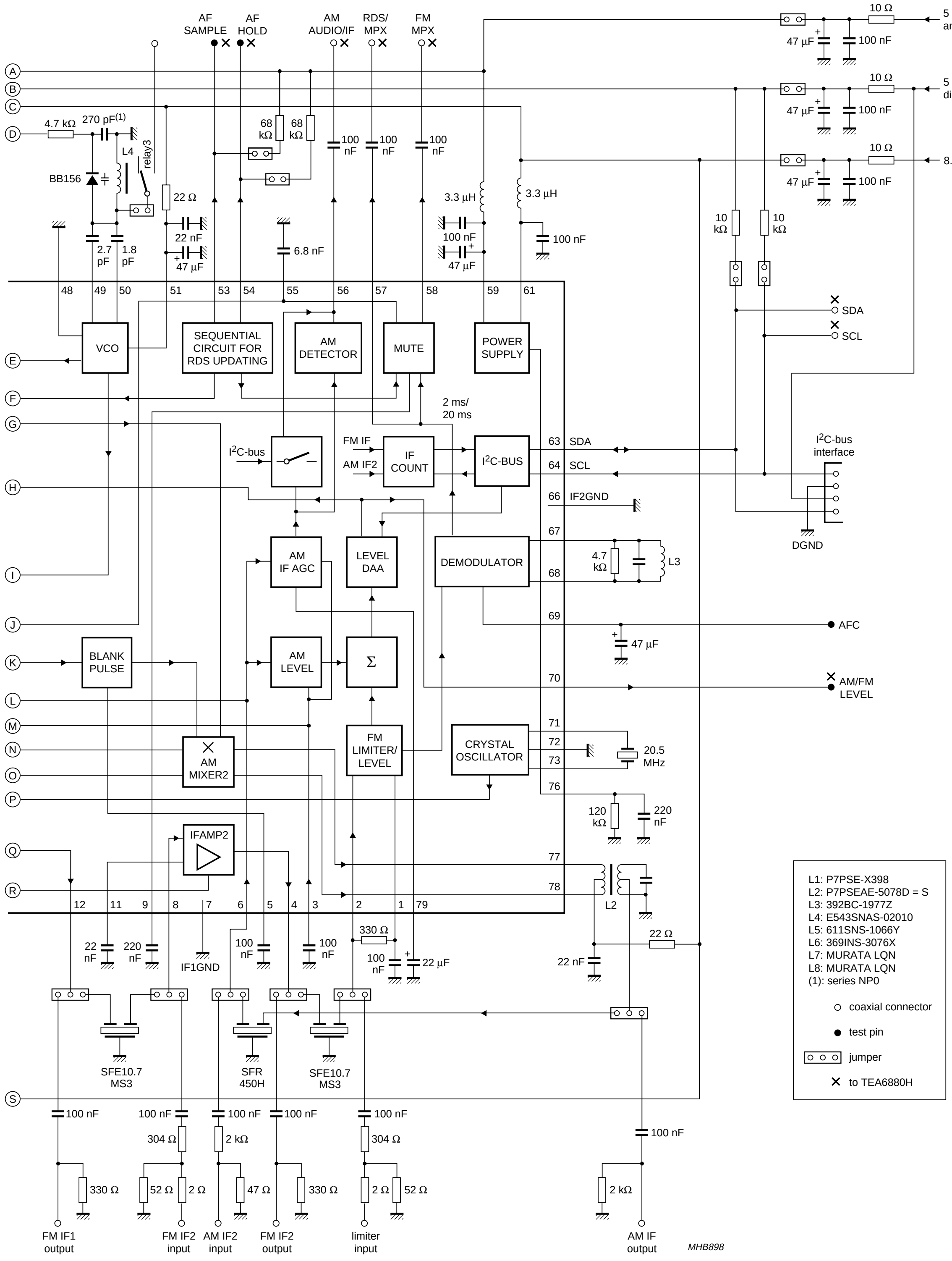


Fig.10 Test circuit (continued from Fig.9).

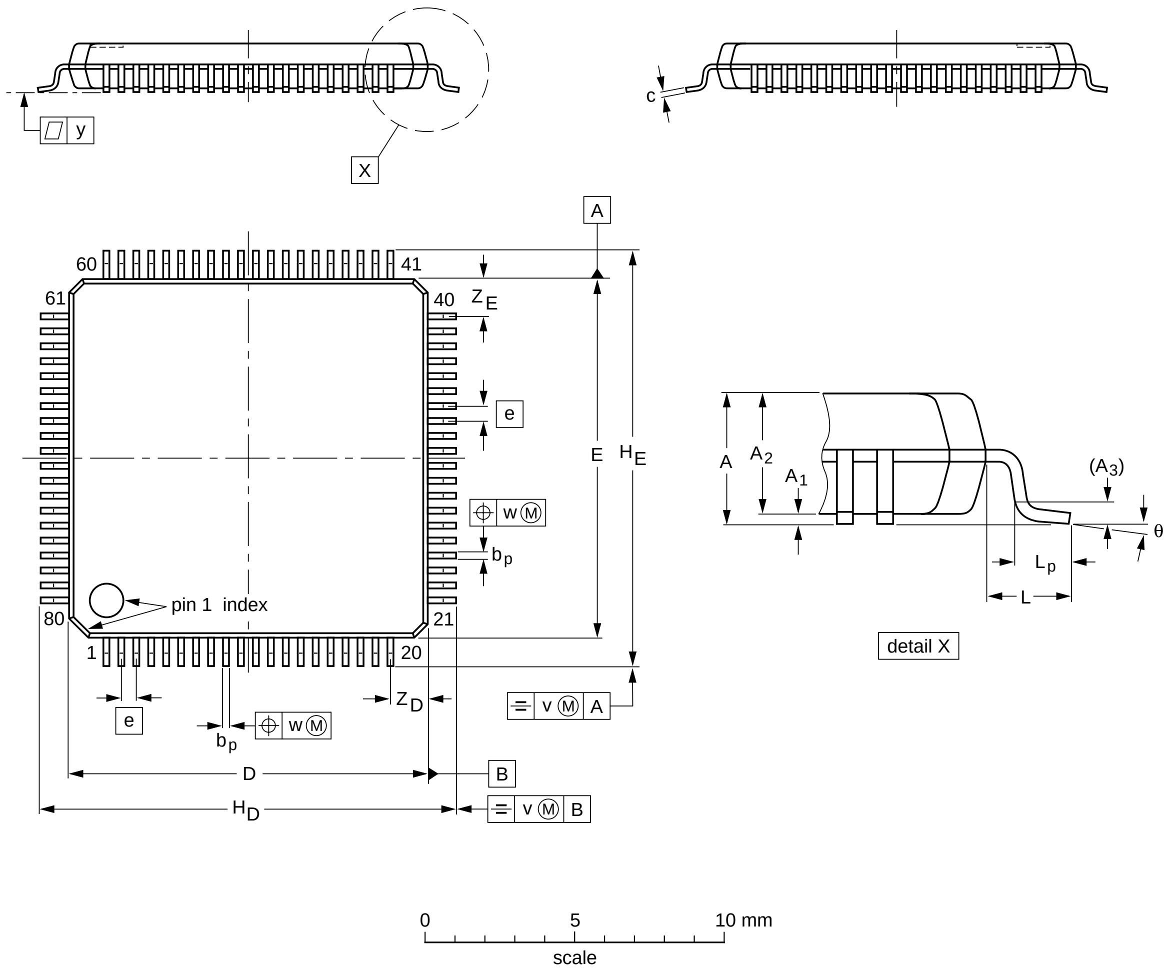
Table 25 DC operating points

SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM MODE			FM MODE		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FMLIMDEC	1	2.5	3	3.5	2.5	2.8	3.1
FMLIMIN	2	2.5	3	3.5	2.5	2.8	3.1
AMIF2DEC	3	2.4	2.7	3.2	floating		
IFAMP2OUT	4	7.2	7.9	–	3.4	3.9	4.4
AMNBHOLD	5	4.3	4.6	5.1	8	8.4	–
AMIF2IN	6	2.4	2.7	3.2	floating		
IF1GND	7	external 0			external 0		
IFAMP2IN	8	3	4	5	2.7	3.1	3.5
C_{offset}	9	floating			3	3.5	4
IFAMP2DEC	11	3	4	5	2.7	3.1	3.5
IFAMP1OUT	12	7.2	7.9	–	3.6	4	4.4
IFAMP1IN	14	2.4	2.7	3	2.3	2.7	3.1
V_{DDA6}	16	external 8.5			external 8.5		
IFAMP1DEC	17	2.4	2.7	3	2.3	2.7	3.1
MIX1OUT1	18	external 8.5			external 8.5		
MIX1OUT2	19	external 8.5			external 8.5		
V_{DDA5}	20	external 8.5			external 8.5		
AMMIX1IN1	22	2.3	2.75	3.1	floating		
AMMIX1IN2	23	2.3	2.75	3.1	floating		
T1AMAGC	26	0	2.8	4.6	0 (no WX)	0.3 (no WX)	0.5 (no WX)
T2AMAGC	27	2.5	2.8	3.1	floating		
IAMAGC	28	open-collector			open-collector		
$V_{ref(FMMIX)}$	29	2.7	3.1	3.4	6.5	7.1	7.9
FMMIXIN2	30	1	1.3	1.6	2.3	2.8	3.3
RFGND	31	external 0			external 0		
FMMIXIN1	33	1	1.3	1.6	2.3	2.8	3.3
IFMAGC	35	floating			1.5 (external biasing)	–	4 (external biasing)
T2FMAGC	36	7.5	8	8.3	3.9	4.6	5.3
T1FMAGC	37	floating			1	–	7
DAAOUT	38	–	0.2	0.3	0.2	–	8.25
DAATD	39	floating			0.2	–	1.5
DAAIN	40	0	–	8.5	0	–	8.5
V_{tune}	42	0	–	8.5	0	–	8.5
CPOUT	43	0	–	8.5	0	–	8.5
V_{DDA4}	44	external 8.5			external 8.5		
FREF	45	3.2	3.4	3.7	3.2	3.4	3.7

SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM MODE			FM MODE		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
V_{DDD}	46	external 5			external 5		
DGND	47	external 0			external 0		
VCOGND	48	external 0			external 0		
OSCFDB	49	2.2	2.8	3.4	2.2	2.8	3.4
OSCTNK	50	5	6.1	7.2	5	6.1	7.2
V_{DDA3}	51	external 8.5			external 8.5		
AFSAMPLE	53	0	0.2	0.5	0	0.2	0.5
AFHOLD	54	open-collector			open-collector		
TRDSMUTE	55	1.9	2.2	2.5	0.7 (muted)	1.2 (muted)	1.7 (muted)
					5.2 (not muted)	5.7 (not muted)	6.2 (not muted)
AMAFIF2	56	4	4.3	4.6	floating		
RDSMPX	57	floating			2.6	3.1	3.3
FMMPX	58	floating			3	3.5	4
V_{DDA2}	59	external 5			external 5		
V_{DDA1}	61	external 8.5			external 8.5		
SDA	63	4.8	5	5.2	4.8	5	5.2
SCL	64	4.8	5	5.2	4.8	5	5.2
IF2GND	66	external 0			external 0		
QDET1	67	floating			3.6	4.1	4.6
QDET2	68	floating			3.6	4.1	4.6
C_{AFC}	69	floating			1.2	3.4	4.1
V_{level}	70	0.05	–	7	0	–	7
XTAL1	71	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	72	external 0			external 0		
XTAL2	73	1.7	2.1	2.5	1.7	2.1	2.5
IREF	76	4	4.25	4.5	4	4.25	4.5
AMMIX2OUT1	77	external 8.5			external 8.5		
AMMIX2OUT2	78	external 8.5			external 8.5		
C_{AGC}	79	3.6	4.3	4.8	4.1	4.6	5.1

14 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1	136E15	MS-026				~~99-12-27~~ 00-01-19

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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19 PURCHASE OF PHILIPS I^2C COMPONENTS

Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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