SPECTRUM DIGITAL INCORPORATED

TMS320VC5509A DSK

Technical Reference

2005 *DSP Development Systems*

TMS320VC5509A DSK
Technical Reference

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Contents

About This Manual

This document describes the board level operations of the TMS320VC5509A DSP Starter Kit (DSK). The DSK is based on the Texas Instruments TMS320VC5509A Digital Signal Processor.

The TMS320VC5509A DSK is a table top card to allow engineers and software developers to evaluate certain characteristics of the TMS320VC5509A DSP to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The TMS320VC5509A will sometimes be referred to as the C55XX.

The TMS320VC5509A DSK will sometimes be referred to as the DSK.

Program listings, program examples, and interactive displays are shown is a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents

Texas Instruments TMS320VC55XX DSP CPU Reference Guide
Texas Instruments TMS320VC55XX DSP Peripherals Reference Guide

Table 1: Hardware History

Revision	History
A	Alpha Release

Table 2: Manual History

Revision	History
A	Alpha Release

Chapter 1

Introduction to the TMS320VC5509A DSK

Chapter One provides a description of the TMS320VC5509A DSK along with the key features and a block diagram of the circuit board.

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1.0 Key Features

The 5509A DSK is a low-cost standalone development platform that enables users to evaluate and develop applications for the TI C55XX DSP family. The DSK also serves as a hardware reference design for the TMS320VC5509A DSP. Schematics, logic equations and application notes are available to ease hardware development and reduce time to market.

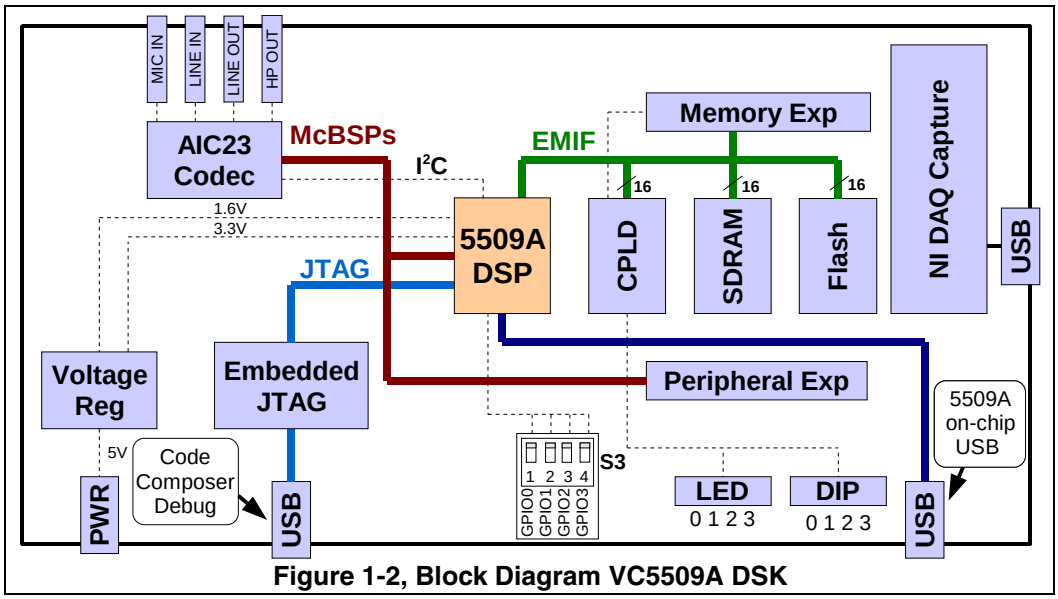

Figure 1-2, Block Diagram VC5509A DSK

The DSK comes with a full compliment of on-board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments TMS320VC5509A-GHH DSP
- Selectable core voltages (1.2V, 1.4V, 1.6V)
- Power capture for core, I/O, and board current via USB to National Instruments power monitor applications
- CPU clock frequency measurement
- An AIC23B stereo codec
- 8 Mbytes of synchronous DRAM
- 512 Kbytes of non-volatile Flash memory
- 4 user accessible LEDs and DIP switches
- User USB port via VC5509A

- Software board configuration through registers implemented in CPLD
- Standard expansion connectors for daughter card use
- JTAG emulation via on-board USB embedded emulator or external JTAG emulator
- Single voltage power supply (+5V)

1.2 Functional Overview of the TMS320VC5509A DSK

The DSP interfaces to external SDRAM, Flash memory and an expansion memory interface connector through its 16-bit External Memory Interface (EMIF). The SDRAM accesses are in 16-bit mode in chip enable 0 memory space. The EMIF provides the necessary refresh signals. The Flash accesses are in 16-bit asynchronous mode in the bottom half of chip enable 1 space. The EMIF signals are brought out to the daughter card expansion connectors which use chip enables 2 and 3.

An on-board AIC23B codec allows the DSP to transmit and receive analog signals. I^2C is used for the codec control interface and McBSP0 is used for data. Analog I/O is done through four 3.5mm audio jacks that correspond to microphone input, line input, line output and headphone output. The codec can select the microphone or the line input as the active input. The analog output is driven to both the line out (fixed gain) and headphone (adjustable gain) connectors.

McBSP1 and McBSP2 are routed to the expansion connectors.

A programmable logic device called a CPLD is used to implement glue logic that ties the board components together. The CPLD has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside in the upper half of chip enable 1.

The DSK includes 4 LEDs and 4 position DIP switch as a simple way to provide the user with interactive feedback. Both are accessed by reading and writing to the CPLD registers. A wake-up push button allows the DSP to be interrupted, to “wake up” the DSP when it is in sleep or idle mode.

An included 5V external power supply is used to power the board. On-board voltage regulators provide the 1.6V to 1.2V DSP core voltage, 3.3V digital and 3.3V analog voltages. A voltage supervisor monitors the internally generated voltage, and will hold the board in reset until the supplies are within operating specifications and the reset button is released.

Code Composer communicates with the DSK through an embedded JTAG emulator with a USB host interface. The DSK can also be used with an external emulator through the external JTAG connector.

1.3 Basic Operation

The DSK is designed to work with TI's Code Composer Studio (CCS) development environment. Code Composer communicates with the board through the on-board JTAG emulator, or an external emulator. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

After the install is complete, follow these steps to run Code Composer. The DSK must be fully connected to launch Code Composer Studio.

1) Connect the included power supply to the DSK.

2) Connect the DSK to your PC with a mini USB cable (also included).

3) Launch Code Composer from its icon on your desktop.

Detailed information about the CCS including a tutorial, examples and reference material is available in the DSK's help file. You can access the help file through Code Composer's help menu.

1.4 Memory Map

The C55x family of DSPs has a unified program and data space with a separate distinct I/O space dedicated to on-chip peripheral registers. For a number of reasons (historical and technical) though, program code is addressable in 8-bit bytes while data is addressable in 16-bit words. Both programs and data can reside anywhere in the unified memory space.

The address reach of the 5509A is 24 bits for a total of 16 megabytes (8 bits/byte) or alternatively 8 megawords (16 bits/word). The external memory interface controller (EMIF) divides the address space into 4 equally sized chip enable (CE) spaces when dealing with external memory. The lower 21 address bits are driven on the EMIF as address lines while the top 3 are decoded and driven as the chip enable for that particular region.

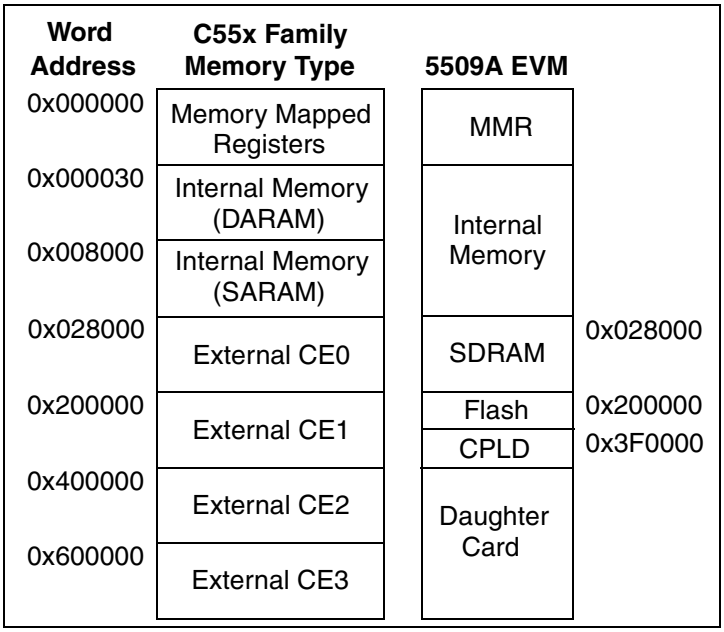

Figure 1-2, Memory Map, VC5509A DSK

The figure above shows a generic memory space map for a C55x family processor and a second map specific to the components on a 5509A DSK. The SDRAM occupies chip enable 0. The Flash and memory mapped registers of the CPLD share CE1 with the Flash in the lower section and the CPLD in the upper section of memory.

Internal memory on the 5509A starts at address 0 and takes precedence over any external memory. The DSP's memory mapped registers occupy the first few bytes of the address space, followed by internal DARAM and a larger amount of internal SARAM. DARAM stands for Dual-Access RAM and is differentiated from SARAM (Single-Access RAM) in that two concurrent memory operations can be performed on the same block rather than one.

Internal memory is divided into blocks, each capable of supporting independent operations. Performance can be optimized by placing code and data so that instructions have their operands spread to different blocks so no stalls are introduced due to contention for one specific block. DARAM blocks are the most precious because their dual-ported nature allows a higher rate of operation. There are 32K words of DARAM and 96K words of SARAM on a 5509A for a total of 128K words of internal memory.

1.5 Boot Mode Settings

The 5509A DSK has 4 position switch that define the DSP's boot configuration at reset. The figure below shows this switch.

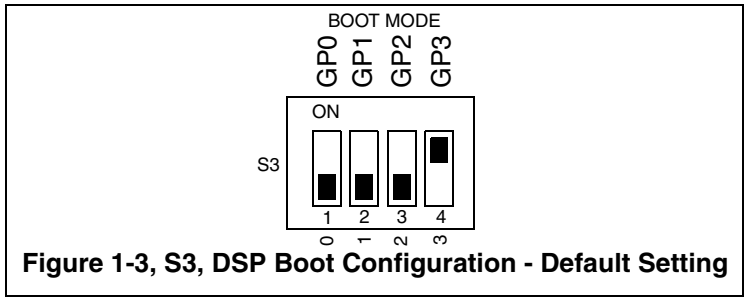

Figure 1-3, S3, DSP Boot Configuration - Default Setting

The switches drive signals that directly correspond to the input on one of the DSP's GP[3-0] configuration pins. If the switch is on, the signal is driven to a logic 0. If the DSP. A view of the switch is shown in the figure below.

The 5509A DSK default boot option is from asynchronous memory mapped in CE1 (Flash on the 5509A DSK board). To boot from a particular device you must pack the object code into a C55x bootloader formatted table and store it in the device. When you set the appropriate BOOTM jumper switches and power cycle the board, the 5509A will parse the bootloader table, load the code into memory and begin execution at the entry point specified in the bootloader table.

The bootloader functionality is contained in on-chip ROM. At reset, the 5509A usually begins execution from the ROM and runs the appropriate bootloader based on the BOOTM pins.

1.6 Power Supply

The DSK operates from a single +5V external power supply connected to the main power input (J5). Internally, the +5V input is converted into +1.6V and +3.3V. The +1.6V supply is used for the DSP core while the +3.3V supply is used for the DSP's I/O buffers and all other chips on the board. The power connector is a 2.5mm. barrel-type plug.

The core voltage on the DSK is selectable based on the output of GPIO5 and GPIO6 or CPLD control registers. If GPIO5 and GPIO6 are high or configured as an input the core voltage will remain at +1.6V. If GPIO5 and GPIO6 are driven low the voltage will drop to +1.2V. The table below shows the 3 core voltage levels available on the VC5509 DSK.

Table 1: Core Voltage Level Select

GPIO6	GPIO5	Core Voltage Selected
0	0	1.2V
0	1	1.4V
1	0	1.4V
1	1	1.6V

There are three power test points on the DSK at JP2, JP3 and JP6. All board current passes through JP2 (the +5V supply). All DSP core current passes through JP3. JP6 allows measurement of DSP I/O pins. To measure the current passing connect the pins with a voltage measuring device. A current shunt is also supplied to amplify this voltage. The output of the shunts are driven into the on board National Instruments capture logic.

The DSK also provides +3.3V for the daughter card. It is also possible to provide the daughter card with +12V and -12V when the external power connector is used.

1.7 National Instruments Capture Interface

The EVM incorporates a National Instruments power capture interface. A separate USB port communicates to the capture logic processor and interface logic. This port is used to monitor on board currents and DSP frequency.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the TMS320VC5509A DSK.

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2.1 CPLD (Programmable Logic)

The VC5509A DSK uses an Altera MAXII EPM240TC100 Complex Programmable Logic Device (CPLD) device to implement:

- 8 Memory-mapped control/status registers that allow software control of various board features.
- Address decode and memory access logic.
- Control of the daughter card interface and signals.
- Assorted "glue" logic that ties the board components together.

2.1.1 CPLD Overview

The CPLD logic is used to implement functionality specific to the 5509A DSK. Your own hardware designs will likely implement a completely different set of functions or take advantage of the DSPs high level of integration for system design and avoid the use of external logic completely.

The EMIF on the 5509A can support several heterogeneous memory types with a glueless interface. However, to reserve CE2 and CE3 for potential daughter-card use on the 5509A DSK, CE1 is split to include the Flash in its bottom half and the CPLD memory-mapped registers in its top half. The address decode logic is used to implement the split.

The CPLD implements simple random logic functions that eliminate the need for additional discrete devices. In particular, the CPLD aggregates the various reset signals coming from the reset button and power supervisors and generates a global reset.

The EPM240TC100 is a +3.3V, 100-pin QFP device that provides 80 I/O pins. The device is EEPROM-based and is in-system programmable via a dedicated JTAG interface (a 10-pin header on the 5509A DSK). The CPLD source files are written in the industry standard VHDL (Hardware Design Language) and are included with the 5509A DSK on the installation CD-ROM.

2.1.2 CPLD Registers

There are 6 DSP CPLD registers mapped into the DSP's lower CE1 address space starting at address 0x3F0000. Since the CPLD decoder only uses part of the address for decoding, the registers will be mirrored within the space.

The table below shows the bit definitions for the 8 registers in CPLD.

Table 1: CPLD Register Definitions

Addr LSB A4-A1	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000	USER_REG	USR_SW3 R	USR_SW2 R	USR_SW1 R	USR_SW0 R	USR_LED3 R/W 0(Off)	USR_LED2 R/W 0(Off)	USR_LED1 R/W 0(Off)	USR_LED0 R/W 0(Off)
0001	DC_REG	DC_DET R	0	DC_STAT1 R	DC_STAT0 R	DC_RST R 0(No reset)	0	DC_CNTL1 R/W 0(Low)	DC_CNTL0 R/W 0(Low)
0010	Reserved								
0011	Reserved								
0100	VERSION	CPLD_VER[3.0] R				0	BOARD VERSION[2.0] R		
0101	Reserved								
0110	MISC	VCORE_CTL1	VCORE_CTL0	Reserved NI Test	VCORE_SEL CPLD REGISTERS 0 GPIO 1 BIT 6 & 7 THIS REG	NI Event Trigger	TIN0 IN/OUT R/W (0 INPUT)	Reserved	Reserved
0111	INT REG	Reserved	Reserved	Reserved	Reserved	WAKEUP INT3	Reserved	WAKUP INT1	WAKEUP INT0

2.1.3 USER_REG Register

USER_REG is used to read the state of the 4 DIP switches and turn the 4 LEDs on or off to allow the user to interact with the 5509A DSK. The DIP switches are read by reading the top 4 bits of the register and the LEDs are set by writing to the low 4 bits.

Table 2: CPLD USER_REG Register

Bit	Name	R/W	Description
7	USER_SW3	R	User DIP Switch S2, position 3 (1 = Off, 0 = On)
6	USER_SW2	R	User DIP Switch S2, position2 (1 = Off, 0 = On)
5	USER_SW1	R	User DIP Switch S2, position 1 (1 = Off, 0 = On)
4	USER_SW0	R	User DIP Switch S2, position 0 (1 = Off, 0 = On)
3	USER_LED3	R/W	User-defined LED 3 Control (0 = Off, 1 = On)
2	USER_LED2	R/W	User-defined LED 2 Control (0 = Off, 1 = On)
1	USER_LED1	R/W	User-defined LED 1 Control (0 = Off, 1 = On)
0	USER_LED0	R/W	User-defined LED 0 Control (0 = Off, 1 = On)

2.1.4 DC_REG Register

DC_REG is used to monitor and control the daughter card interface. DC_DET detects the presence of a daughter card. DC_STAT and DC_CNTL provide simple communications with the daughter card through readable status lines and writable control lines.

The daughter card is released from reset when the DSP is released from reset. DC_RST can be used to put the card back in reset.

Table 3: DC_REG Register

Bit	Name	R/W	Description
7	DC_DET	R	Daughter Card Detect (1= Board detected)
6	0	R	Always 0
5	DC_STAT1	R	Daughter Card Status 1 (0=Low, 1 = High)
4	DC_STAT0	R	Daughter Card Status 0 (0=Low, 1 = High)
3	DC_RST	R/W	Daughter Card Reset (0=No Reset, 1 = Reset)
2	0	R	Always zero
1	DC_CNTL1	R/W	Daughter Card Control 1(0 = Low, 1 = High)
0	DC_CNTL0	R/W	Daughter Card Control 0(0 = Low, 1 = High)

2.1.5 VERSION Register

The VERSION register contains two read only fields that indicate the BOARD and CPLD versions. This register will allow your software to differentiate between production releases of the 5509A DSK and account for any variances. This register is not expected to change often, if at all.

Table 4: Version Register Bit Definitions

Bit #	Name	R/W	Description
7	CPLD_VER3	R	Most Significant CPLD Version Bit
6	CPLD_VER2	R	CPLD Version Bit
5	CPLD_VER1	R	CPLD Version Bit
4	CPLD_VER0	R	Least Significant CPLD Version Bit
3	0	R	Always 0
2	5509A DSK_VER2	R	Most Significant 5509A DSK Board Version Bit
1	5509A DSK_VER1	R	5509A DSK Board Version Bit
0	5509A DSK_VER0	R	Least Significant 5509A DSK Board Version Bit

2.1.6 MISC Register

The MISC register is used to provide software control for miscellaneous board functions. On the 5509A DSK, the MISC register controls how auxiliary signals are brought out to the daughter-card connectors.

The TIN0 bit is used to select whether the DSP's TIN0 (timer) signal is connected to the peripheral expansion connector as inputs or outputs. The expansion connector has separate pins for inputs and outputs so each signal must be routed to one of two physical pins. A 0 indicates that the signal should be connected to the input pin on the expansion connector. A 1 indicates that it should be connected to the output pin.

The NI Event Trigger is a software controllable bit that allows the VC5509A DSP to signal the National Instrument capture controller of an event. This pin is driven to one of the ADC channels on the capture controller.

Table 5: MISC Register

Bit	Name	R/W	Description
7	VCORE_CTL1	R/W	Selects Voltage Control 1
6	VCORE_CTL0	R/W	Selects Voltage Control 0
5	NI Test	R/W	Reserved for factory test
4	VCORE_SEL	R/W	0 = GPIO, 1= CPLD Reg bits 6 & 7
3	NI Event Trigger	R/W	Notify capture logic of event
2	TINSEL0	R/W	TIN0 in/out on daughter card (0 = input, 1 = output)
1	Reserved	R	
0	Reserved	R	

2.1.7 Interrupt Register

The DSK allows interrupts to be generated from the “Wake Up” switch, S4. These interrupts can be routed to various pins on the VC5509A DSP. The interrupt register does this routing. When the corresponding bit is set to a “1” the DSP will be interrupted by the “Wake Up” switch. The interrupts to choose from are DSP interrupts 0, 1, or 3 as shown in the table below.

Table 6: Interrupt Register

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Wakeup Int3
2	Reserved
1	Wakeup Int1
0	Wakeup Int0

2.2 AIC23 Codec

The 5509A DSK uses a Texas Instruments AIC23B (part #TLV320AIC23B) stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line and headphone outputs so the user can hear the output.

The codec communicates using I^2C and a McBSPs. The I^2C controls the codec's internal configuration registers. The McBSP is used to send and receive digital audio samples. The control channel is typically only used when configuring the codec, it is generally idle when audio data is being transmitted,

McBSP0 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The 5509A DSK examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side. The preferred serial format is DSP mode which is designed specifically to operate with the McBSP ports on TI DSPs.

The codec has a 12MHz system clock. The 12MHz system clock corresponds to USB sample rate mode, named because many USB systems use a 12MHz clock and can use the same clock for both the codec and USB controller. The internal sample rate generate subdivides the 12MHz clock to generate common frequencies such as 48KHz, 44.1KHz and 8KHz. The sample rate is set by the codec's SAMPLERATE register. The figure below shows the Coded interface on the VC5509A DSK.

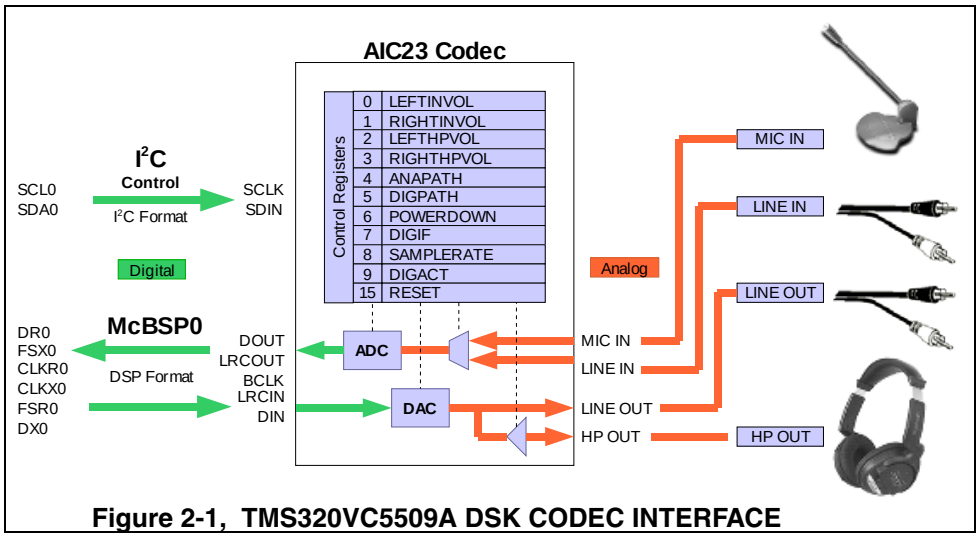


Figure 2-1, TMS320VC5509A DSK CODEC INTERFACE

2.3 Synchronous DRAM

The 5509A DSK uses an industry standard 32 megabit Synchronous SDRAM. It uses a 16-bit interface and is used with a 92 MHz external memory clock. Since the DSP runs at 192 MHz, the EMIF must be programmed to use the SDRAM at half the core clock rate.

The SDRAM occupies both chip enable 0 and 1. It appears on both chip enables because it is twice the size of a single chip enable space. Since the Flash and CPLD use chip enable 1, the 5509A DSK examples configure CE1 as asynchronous memory for their use and the SDRAM on CE1 is invisible.

SDRAM must be constantly refreshed to maintain the integrity of its contents. This SDRAM must update one row every 15.6 microseconds to meet its minimum requirements. The EMIF can be programmed to automatically generate refresh signals based on this time period.

2.4 Flash Memory

The 5509A DSK provides 256K x 16-bit words of external Flash memory. The board itself is pinned out to allow expansion to 1M x 16 parts. The Flash is mapped into CE1 space because that is where the 16-bit asychronous bootloader looks for a boot image when booting from the Flash. The space is shared by the CPLD, but the CPLD timings are subsetted by the Flash so the Flash is the critical factor in configuring CE1.

The Flash itself is a 70ns device but some additional delays are incurred in the CPLD logic that separates the Flash and CPLD registers. Because of this, the EMIF should be programmed for an access time of at least 100ns.

2.5 LEDs and DIP Switches

The 5509A DSK includes 4 software accessible LEDs (DS1-DS4) and DIP switches (S2) that provide the user a simple form of input/output. Both are accessed through the CPLD USER_REG register.

2.6 Core Power Control

The VC5509A DSK uses two transistors to modify the feedback to the TPS62000 regulator used to supply the DSP's core voltage. These two transistors form a voltage divider on the feedback to allow the core voltage to switch from 1.6 volts to 1.4 volts to 1.2 volts.

Control of the feedback can be done in 2 ways. The default mechanism is with GPIO5 and GPIO6 of the DSP. The alternative method is to use the 2 bits VCORE_CTL1 and VCORE_CTL0 in the CPLD MISC register. VCORE_SEL in the MISC register determines which mode is used. At power up the register is set to "0" for GPIO mode when VCORE_SEL is set to a "1" the bits 6 and 7 control the voltage control.

2.7 Current Shunts

The VC5509A DSK has 3 shunt devices to convert the small currents of the core, I/O and board currents to voltages. These voltages are then driven into an op-amp which directly interfaces embedded National Instruments power measurement logic. The shunt resistance, shunt gain, and op-amp gain are shown in the table below.

Table 7: Current Shunts

	Shunt Resistance	Shunt Output Resistance	Op-Amp Gain	Total Gain	Volts per MA	Typical Current	Typical Output
DSP Core	0.1	50K	3	150	.015 volts	150 MA	
DSP I/O	0.1	100K	3	300	.03 volts	5 MA	
DSK	0.025	100K	3	300	.0075 volts	400 MA	

To determine the formula for output voltage to the input current we calculate the value in stages. An example is shown below.

The voltage going into the shunt resistor is derived from:

```
V = IR
```

So for the core current of 1 MA. we have:

```
V = .001 amp  x  .1 ohm = .0001
```

The internal resistance of the shunt current device is 1K ohm. The output is basically a constant current source with a load resistance of 100K(see table above), with this value gain is 50 or 100 regardless of the input shunt resistance. So for 1 MA. we have .001 x .1 x 100 at the output of the current shunt amplifier. This is driven into a non-inverting output amplifier with a gain of 3 so we have .001 x .1 x 100 x 3 for .03 volts per milliampere.

2.8 CPU Frequency Encoder

The 5509A DSK incorporates a CPU frequency encoder for debug and demo purposes to the integrated National Instruments capture logic. The 5509A's CLKOUT pin needs to be programmed to the divide by 4 option for this feature to be operational. The frequency encoder uses a base 24 Mhz clock driving a counter for the timebase which resets every 208 clocks. The CPU clock drives another counter. Every time the timebase counter rolls over the upper 5 bits of the CPU clock counter is output to the NI capture logic. Depending on the output code the capture unit can detect the average CPU frequency for every timebase interval.

A separate bit is used to indicate when the frequency encoder is being updated. The mapping of these bits is discussed in the NI capture interface.

2.9 National Instruments Capture Interface

The National Instruments capture logic integrates logic onto the DSK to allow power measurement and frequency detection monitoring. The on board capture processor allows 3 analog voltages, one event pin, and 8 digital I/Os to be monitored. Four LEDs are also driven by this logic.

The analog inputs on the NI analog inputs are used to measure on board current from the VC5509A processor and to detect a user driven VC5509a driven event. The table below indicates the mapping of the analog channels.

Table 8: NI Analog Channel Interface

Analog Channel	Function
0	VC5509A Core current input
1	VC5509A I/O current input
2	DSK board current
3	VC5509A event trigger

The capture unit has eight digital I/O pins. These are used for CPU frequency detection along with other user defined items. The mapping is shown below.

Table 9: NI Frequency Detection Interface

Digital Input	Description	
0	Frequency Detect 0	LSB of frequency detect mode
1	Frequency Detect 1	Second bit of frequency detect mode
2	Frequency Detect 2	Third bit of frequency detect mode
3	Frequency Detect 3	Fourth bit of frequency detect mode
4	Frequency Detect 4	MSB of frequency detect mode
5	Capture interface valid	
6	Reserved	
7	Reserved	

2.10 Daughter Card Interface

The 5509A DSK provides two expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their 5509A DSK platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are for memory and peripherals.

The memory connector provides access to the DSP's asynchronous EMIF signals to interface with memories and memory mapped devices. It supports byte addressing. The peripheral connector brings out the DSP's peripheral signals like McBSPs, timers, and clocks. Both connectors provide power and ground to the daughter card

Most of the expansion connector signals are buffered so that the daughter card cannot directly influence the operation of the 5509A DSK board. The use of TI low voltage, 5V tolerant buffers, and CBT interface devices allows the use of either +5V or +3.3V devices to be used on the daughter card.

Other than the buffering, most daughter card signals are not modified on the board. However, a few daughter card specific control signals like DC_RESET and DC_DET exist and are accessible through the CPLD DC_REG register. The 5509A DSK also multiplexes the McBSP2 for on-board or external use.
This function is controlled through the CPLD MISC register.

The timer signals on the peripheral expansion connector have connections for both inputs and outputs. since the VC5509A does not have separate timer inputs and outputs, the CPLD is used to select whether the input or output pin should be connected to the timer. This selection is also controlled through the CPLD MISC register.

Chapter 3

Physical Description

This chapter describes the physical layout of the TMS320VC5509A DSK and its connectors.

Topic **Page**

3.1 Board Layout

The VC5509A DSK is a 8.25 x 4.5 inch (210 x 115 mm.) ten (10) layer board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the VC5509A DSK.

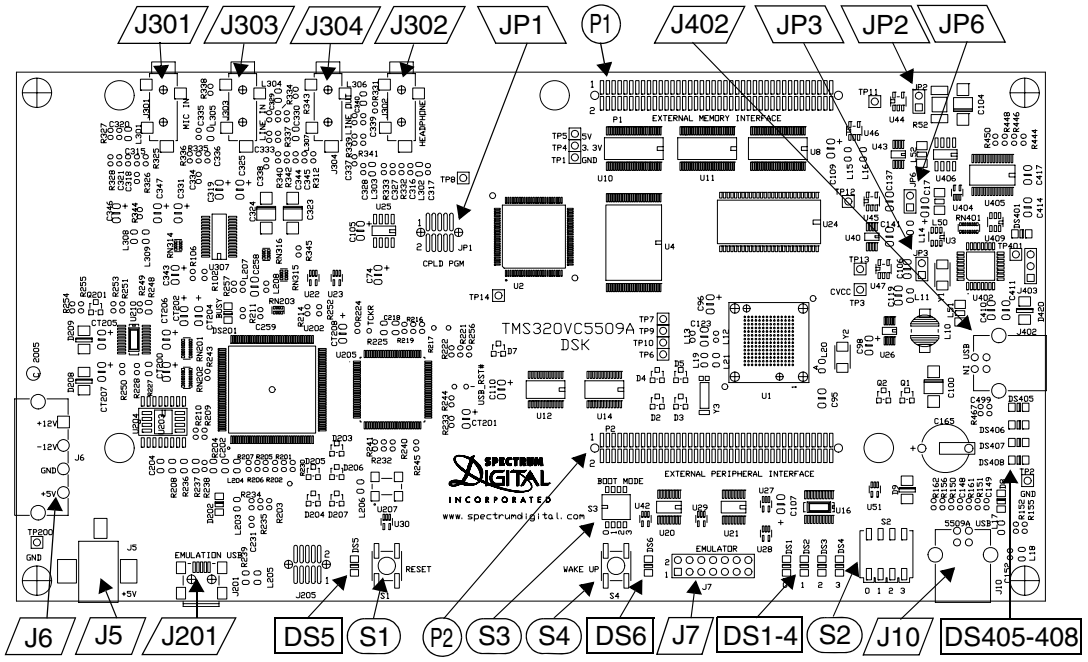


Figure 3-1, TMS320VC5509A DSK

3.2 Connector Index

The TMS320VC5509A DSK has many connectors which provide the user access to the various signals on the DSK.

Table 1: TMS320VC5509A DSK Connectors

Connector	# Pins	Function	Schematic Page
P1	80	Memory	9
P2	80	Peripheral	9
J301	2	Microphone	17
J303	2	Line In	17
J304	2	Line Out	17
J302	2	Headphone	17
J5	2	+5 Volt	10
J6 *	4	Optional Power Connector	10
J7	14	External JTAG	14
J201	5	USB Port	15
JP1	10	CPLD Programming	3
J402	4	National Instruments Power Monitoring Interface	15

Note: **"*"** Not populated

3.3 Expansion Connectors

The TMS320VC5509A DSK supports two expansion connectors that follow the Texas Instruments interconnection guidelines. The expansion connector pinouts are described in the following two sections.

The two expansion connectors are all 80 pin 0.050 x 0.050 inches low profile connectors from Samtec or AMP. The Samtec SFM Series (surface mount) connectors are designed for high speed interconnections because they have low propagation delay, capacitance, and cross talk. The connectors present a small foot print on the DSK. Each connector includes multiple ground, +5V, and +3.3V power signals so that the daughter card can obtain power directly from the DSK. The peripheral expansion connector additionally provides both +12V and -12V to the daughter card. The recommended mating connector, whose part number is TFM-140-32-S-D-LC, is a surface mount connector that provides a 0.465" mated height.

Note: I is on an Input pin
O is on an Output pin
Z is on a High Impedance pin

3.3.1 P1, Memory Expansion Connector

Table 2: P1, Memory Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+5 Volts	O	2	+5 volts	O
3	Reserved	O	4	A20	O
5	A19	O	6	A18	O
7	A17	O	8	A16	O
9	A15	O	10	A14	O
11	GND	O	12	GND	O
13	A13	O	14	A12	O
15	A11	O	16	A10	O
17	A9	O	18	A8	O
19	A7	O	20	A6	O
21	+5 Volts	O	22	+5 Volts	O
23	A5	O	24	A4	O
25	A3	O	26	A2	O
27	A1		28	A0	
29	BE1n	O	30	BE0n	O
31	GND	O	32	GND	O
33	Reserved		34	Reserved	
35	Reserved		36	Reserved	
37	Reserved		38	Reserved	
39	Reserved		40	Reserved	
41	+3.3 Volts	O	42	+3.3 Volts	O
43	Reserved		44	Reserved	
45	Reserved		46	Reserved	
47	Reserved		48	Reserved	
49	Reserved		50	Reserved	
51	GND	O	52	GND	O
53	D15	I/O/Z	54	D14	I/O/Z
55	D13	I/O/Z	56	D12	I/O/Z
57	D11	I/O/Z	58	D10	I/O/Z
59	D9	I/O/Z	60	D8	I/O/Z
61	GND	O	62	GND	O
63	D7	I/O/Z	64	D6	I/O/Z
65	D5	I/O/Z	66	D4	I/O/Z
67	D3	I/O/Z	68	D2	I/O/Z
69	D1	O	70	D0	O
71	GND	O	72	GND	O
73	REn	O	74	WEn	O
75	OEn	O	76	RDYn	I
77	CE3n	O	78	CE2n	O
79	GND	O	80	GND	O

3.3.2 P2, Peripheral Expansion Connector

Table 3: P2, Peripheral Expansion Connector

Pin #	Signal Name	I/O/Z	Pin #	Signal Name	I/O/Z
1	+12 Volts *	O	2	-12 Volts *	O
3	GND	O	4	GND	O
5	+5 Volts	O	6	+5 Volts	O
7	GND	O	8	GND	O
9	+5 Volts	O	10	+5 Volts	O
11	RESERVED		12	RESERVED	
13	RESERVED		14	RESERVED	
15	RESERVED		16	RESERVED	
17	RESERVED		18	RESERVED	
19	+3.3 Volts	O	20	+3.3 Volts	O
21	CLKX1	I/O/Z	22	RESERVED	
23	FSX1	I/O/Z	24	DX1	O/Z
25	GND	O	26	GND	O
27	CLKR1	I/O/Z	28	RESERVED	
29	FSR1	I/O/Z	30	DR1	I
31	GND	O	32	GND	O
33	CLKX2	I/O/Z	34		
35	FSX2	I/O/Z	36	DX2	O/Z
37	GND	O	38	GND	O
39	CLKR2	I/O/Z	40	RESERVED	
41	FSR2	I/O/Z	42	DR2	Z
43	GND	O	44	GND	O
45	TOUT0	Z	46	TIN0	I
47	INT0n	I	48	INT2n	I
49			50		
51	GND	O	52	GND	O
53	INT1n	I	54		
55	RESERVED		56		
57	RESERVED		58	INT4n	I
59	RESETn	O	60	RESERVED	
61	GND	O	62	GND	O
63	DC_CNTL1	O	64	DC_CNTL0	O
65	DC_STAT1	I	66	DC_STAT0	I
67	INT3n	I	68	RESERVED	
69	RESERVED		70	RESERVED	
71	RESERVED		72	RESERVED	
73	RESERVED		74	RESERVED	
75	DETECTn	I	76	GND	O
77	GND	O	78	CLKOUT	O
79	GND	O	80	GND	O

3.3.3 J402, National Instruments Power Monitoring Interface

The VC5509A DSK provides a direct integration the National Instruments series of instrumentation products. This instrumentation is connected to the host development computer via a USB connection.

3.3.3.1 Analog Probe Connectors

Four connectors are available to monitor inputs to the National Instruments connector for analog probing. The functions are shown in the table below.

Table 4: Analog Probe Connectors

Connector	Signal Name
JP3, Pin 1	Core Shunt
JP3, Pin 2	Core Shunt
JP6, Pin 1	I/O Shunt
JP6, Pin 2	I/O Shunt
JP2, Pin 1	T2 Board Shunt
JP2, Pin 2	Board Shunt
JPX, Pin 1	T3 Trigger Event
JPX, Pin 2	Ground

3.4 Audio Connectors

The VC5509A DSK has 4 audio connectors. They are described in the following sections. These connectors provide audio inputs and outputs to the on board AIC23B device.

3.4.1 J301, Microphone Connector

The input is a 3.5 mm. stereo jack. Both inputs are connected to the microphone so it is monaural. The signals on the plug are shown in the figure below.

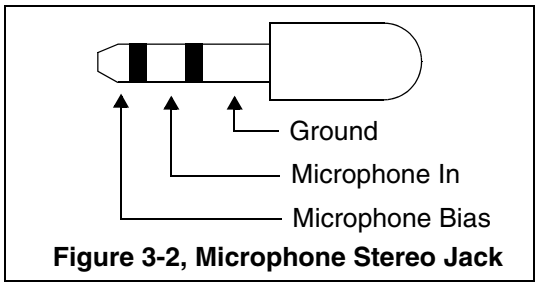


Figure 3-2, Microphone Stereo Jack

3.4.2 J303, Audio Line In Connector

The audio line in is a stereo input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

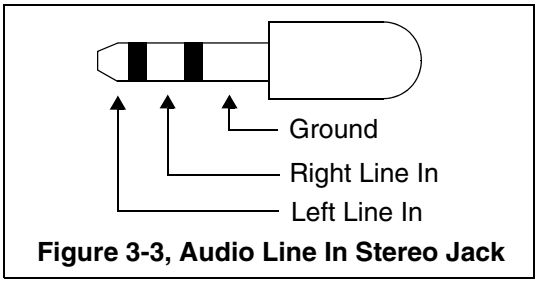


Figure 3-3, Audio Line In Stereo Jack

3.4.3 J304, Audio Line Out Connector

The audio line out is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

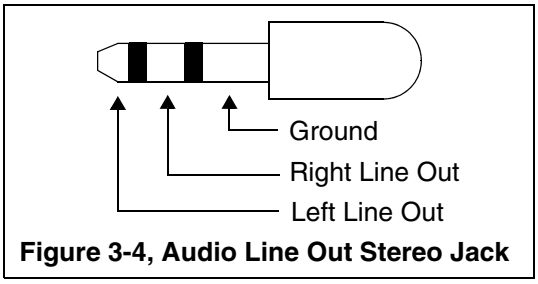


Figure 3-4, Audio Line Out Stereo Jack

3.4.4 J302, Headphone Connector

Connector J4 is a headphone/speaker jack. It can drive standard headphones or a high impedance speaker directly. The standard 3.5 mm jack is shown in the figure below

.

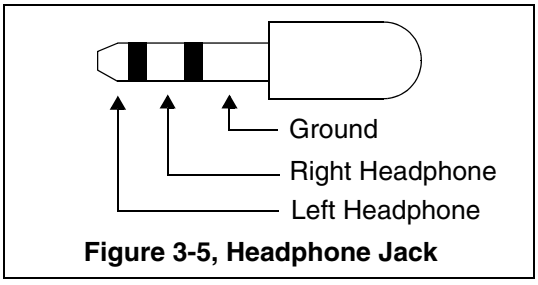


Figure 3-5, Headphone Jack

3.5 Power Connectors

The VC5509A DSK has 2 power connectors. They are described in the following sections.

3.5.1 J5, +5 Volt Connector

Power (+5 volts) is brought onto the TMS320VC5509A DSK via the J5 connector. The connector has an outside diameter of 5.5 mm. and an inside diameter of 2.5 mm. The A diagram of J5 is shown below.

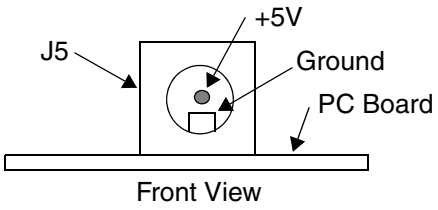


Figure 3-6, TMS320VC5509A DSK Power Connector

3.5.2 J6, Optional Power Connector

Connector J6 is an optional power connector. It will operate with the standard personal computer power supply. To populate this connector use a Molex #15109-0410 or Tyco #174552-1. The table below shows the voltages on the respective pins.

Table 5: J6, Optional Power Connector

Pin #	Voltage Level
1	+12 Volts
2	-12 Volts
3	Ground
4	+5 Volts

WARNING !
Do not plug into J5 and J6 at the same time.

3.6 Miscellaneous Connectors

The VC5509A DSK has 3 additional connectors to aid the user in developing with this product. They are described in the following sections.

3.6.1 J201, Mini USB Connector

Connector J201 provides a Universal Serial Bus (USB) Interface to the embedded JTAG emulation logic on the DSK. This allows for code development and debug without the use of an external emulator. The signals on this connector are shown in the below.

Table 6: J201, USB Connector

Pin #	USB Signal Name
1	USBVdd
2	D+
3	D-
4	USB Vss
5	Shield
6	Shield

3.6.2 J7, External JTAG Connector

The TMS320VC5509A DSK is supplied with a 14 pin header interface, J7. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown figure 3-6 below.

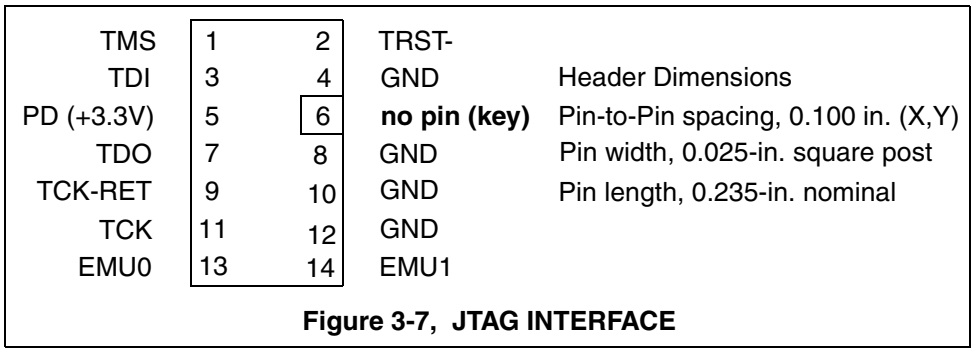


Figure 3-7, JTAG INTERFACE

3.6.3 JP1, PLD Programming Connector

This connector interfaces to the Altera CPLD, U2. It is used in the in the factory for the programming of the CPLD. This connector is not intended to be used outside the factory.

3.7 User LEDs

The VC5509A DSK provides 4 LEDs which show self test status at power up and are available for application programs or demonstrations. The LEDs are accessed via the user register of the CPLD. For more information on the control of the LEDs refer to the user register section of the CPLD.

3.8 System LEDs

TheTMS320VC5509A DSK has three control system light emitting diodes (LEDs). These LEDs indicate various conditions on the DSK. These function of each LED is shown in the table below.

Table 7: System LEDs

Reference Designator	Color	Function
DS6	Green	USB Emulation in use. When External JTAG Emulator is used this LED is off.
DS5	Orange	RESET Active
DS201	Green	USB Active, Blinks during USB data transfer

3.9 NI Power Capture Interface LEDs

The National Instruments Power Capture Interface has 4 LEDs which indicate the status of the interface. Their function is shown in the table below.

Table 8: NI Power Capture Interface LEDs

Reference Designator	Color	Function
DS405	Green	NI User
DS405	Green	NI User
DS407	Green	NI User
DS408	Green	NI User
	Green	USB Channel Busy

3.10 VC5509A DSK Switches

The VC5509A DSK has 4 switches. The logic connections for these switches are shown on page 5 of the schematics in appendix A. A list of the switches is shown in the table below:

Table 9: VC5509A Switches

Switch Designator	Function
S1	RESET Switch
S2	User DIP Switch
S3	DSK Boot Load Mode Select
S4	Wake Up Switch

3.10.1 S1, Reset Switch

There are three resets on the TMS320VC5509A DSK. The first reset is the power on reset. This circuit waits until power is within the specified range before releasing the power on reset pin to the TMS320VC5509A.

External sources which control the reset are push button S1, and the on board embedded USB JTAG emulator.

3.10.2 S2, User DIP Switch

S2 is a 4 position DIP switch to be used by application and demonstration programs. The switch is mapped into the CPLD and can be accessed via the User register. For more details see the section on CPLD register 2, User register.

3.10.3 S3, Boot Mode Select Switch

S3 is a 4 position DIP switch that allows the user to select the boot load mode of the DSP. A view of the switch is shown in the figure below.

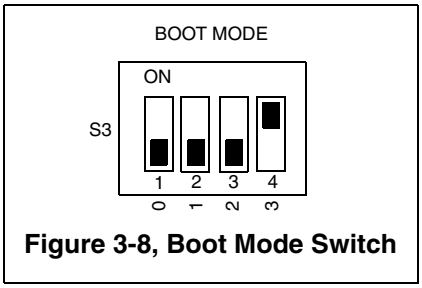


Figure 3-8, Boot Mode Switch

The switch settings and boot load mode are shown in the table below.

Table 10: VC5509A DSK Boot Load Options

Position 1 GPIO0	Position 2 GPIO1	Position 3 GPIO2	Position 4 GPIO3	BOOT MODE PROCESS	SUPPORTED ON DSK
0	0	0	0	Reserved	No
0	1	0	0	Serial SPI EPROM boot (24 bit address) via McBSP0	No
0	0	1	0	USB	Yes
0	1	1	0	I^2C EEPROM (7 bit address)	No
0	0	0	1	Reserved	No
0	1	0	1	HPI - multiplexed mode	No
0	0	1	1	HPI - non multiplexed mode	No
0	1	1	1	Reserved	No
1	0	0	0	Execute from 16-bit wide asychronous memory (on CE1- space)	Yes
1	1		0	Serial SPI EPROM boot (16 bit address) via McBSP0	No
1	0	1	0	8-bit wide asychronous memory (on CE1- space)	No
1	1	1	0	16-bit wide asychronous memory (on CE1- space)	Yes *
1	0	0	1	Reserved	No
1	1	0	1	Reserved	No
1	0	1	1	Standard serial boot from McBSP0 (16-bit data)	No
1	1	1	1	Standard serial boot from McBSP0 (8-bit data)	No

* default on DSK

3.10.4 S4, Wake Up Switch

S4 is a “Wake Up” switch to the DSP. When the DSP is in idle mode the switch can generate an interrupt to wake up the DSP. See the section on the CPLD Interrupt register to enable interrupts for the “Wake Up” switch.

3.11 Test Points

The VC5509A DSK has fifteen (15) test points. The position of these test points are shown in the figure below.

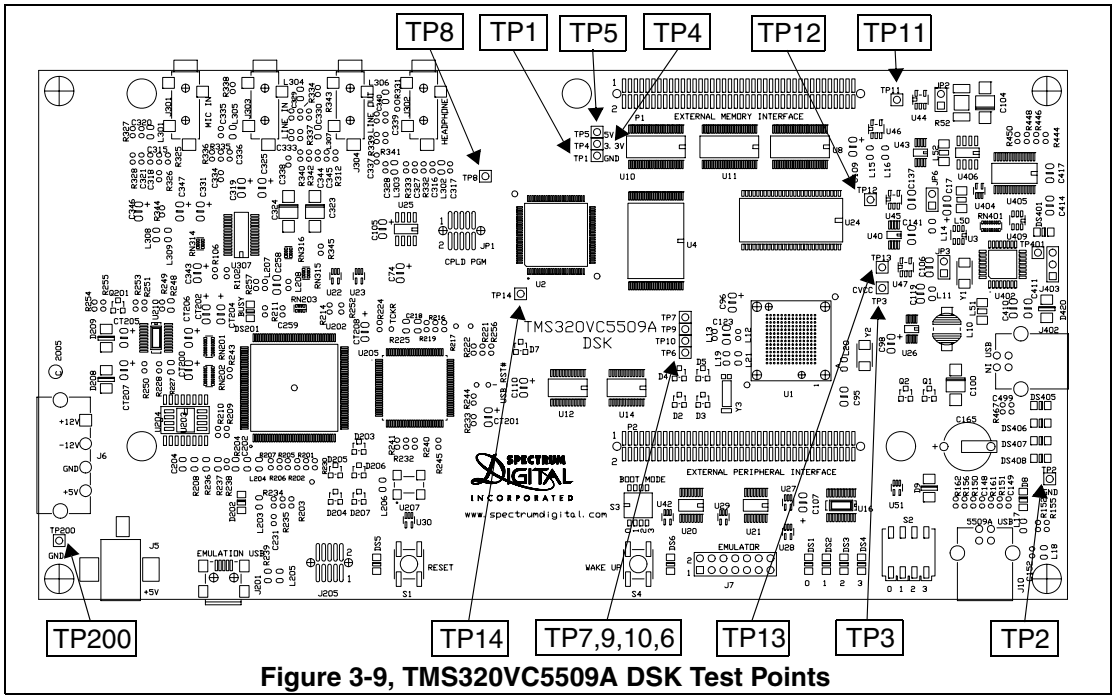


Figure 3-9, TMS320VC5509A DSK Test Points

The table below shows the signals present on each test point.

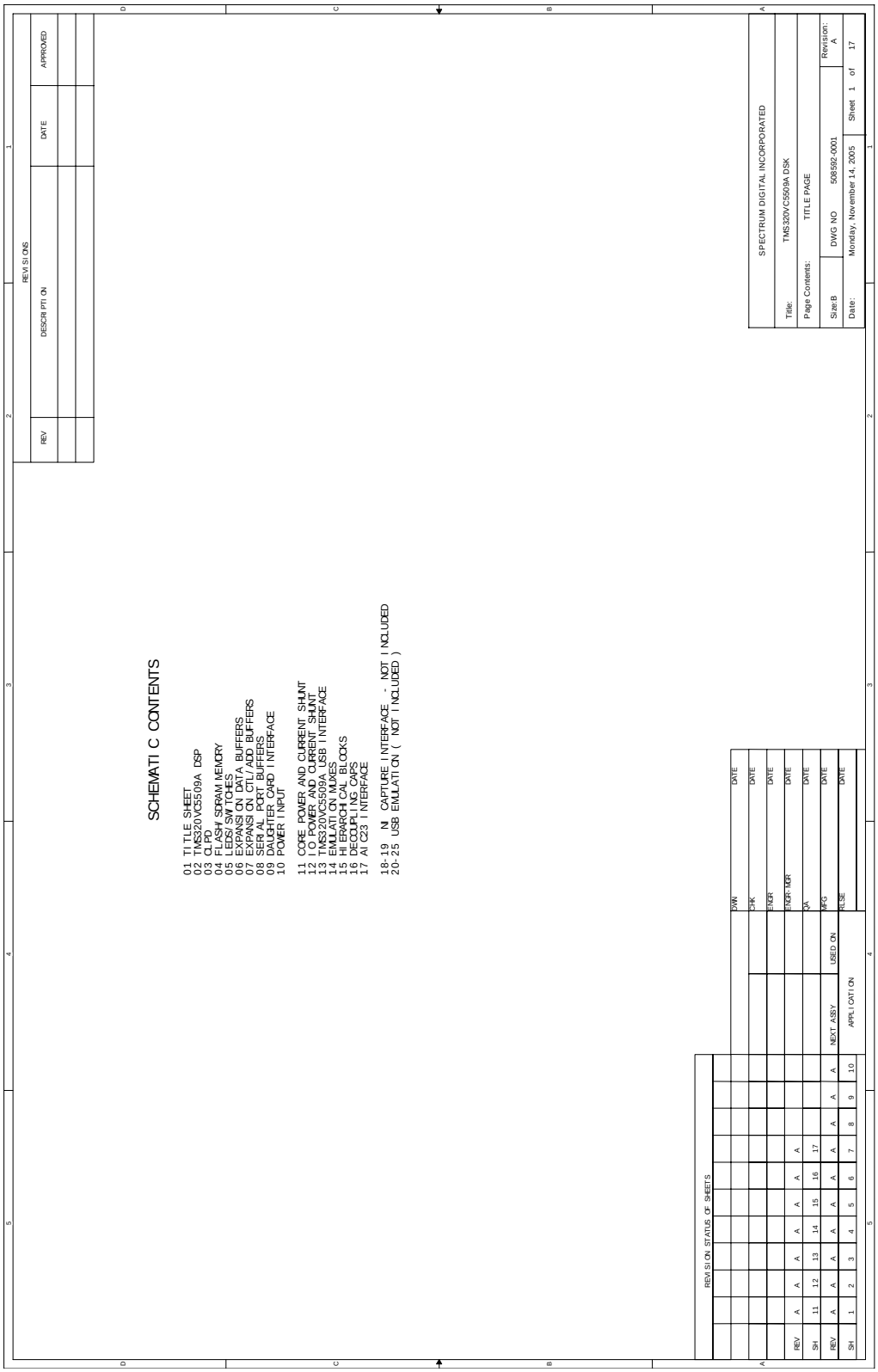
Table 11: VC5509A DSK Test Points

Test Point #	Signal
TP1	GND
TP2	GND
TP3	DSP_CVCC
TP4	+3.3V
TP5	+5V
TP6	+3.3V
TP7	GND
TP8	U2, B2.PIN97
TP9	
TP10	
TP11	U44, Pin 1
TP12	U45, Pin 1
TP13	U47, Pin 1
TP14	B1.GCLK1
TP200	GND

Appendix A

Schematics

This appendix contains the schematics for the TMS320VC5509A DSK. Board components with designators over 200 (e.g. DS210, R211) are part of Spectrum Digital's embedded JTAG emulator and are not included in these schematics.


REVISIONS
REV
DESCRIPTION
DATE
APPROVED
SCHEMATIC CONTENTS
01 TITLE SHEET
02 TMS320VC5509A DSP
03 CLPD
04 FLASH, SDRAM MEMORY
05 LEDS, SW TCHES
06 EXPANSION DATA BUFFERS
07 EXPANSION CTL/ADD BUFFERS
08 SERIAL PORT BUFFERS
09 DAUGHTER CARD INTERFACE
10 POWER INPUT
11 CORE POWER AND CURRENT SHUNT
12 I/O POWER AND CURRENT SHUNT
13 TMS320VC5509A USB INTERFACE
14 EMULATION MUXES
15 HIERARCHICAL BLOCKS
16 DECOUPLING CAPS
17 AIC23 INTERFACE
18-19 NI CAPTURE INTERFACE - NOT INCLUDED
20-25 USB EMULATION (NOT INCLUDED)
REVISION STATUS OF SHEETS
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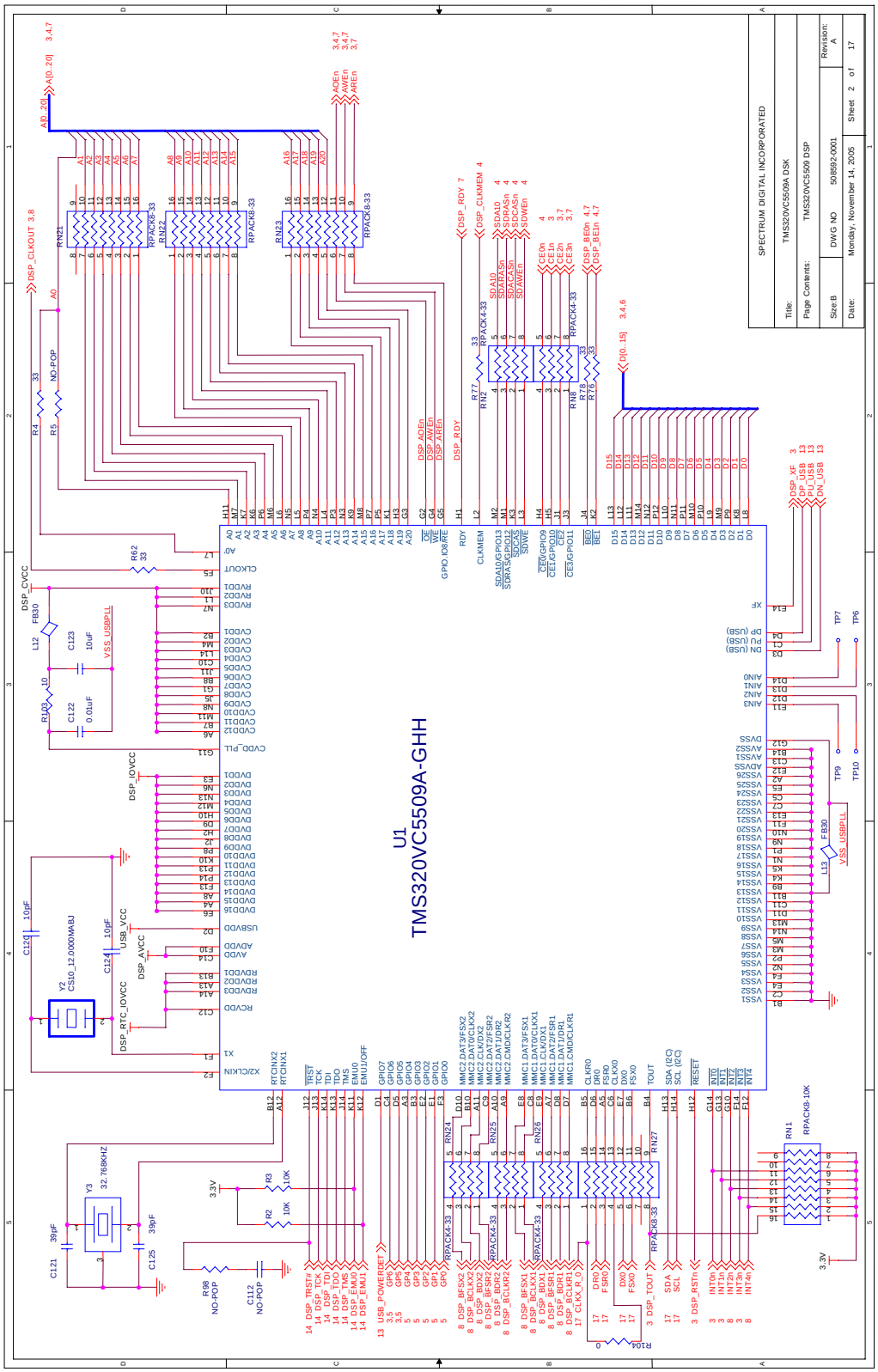
Page Contents: TITLE PAGE
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 1 of 17


U1
TMS320VC5509A-GHH
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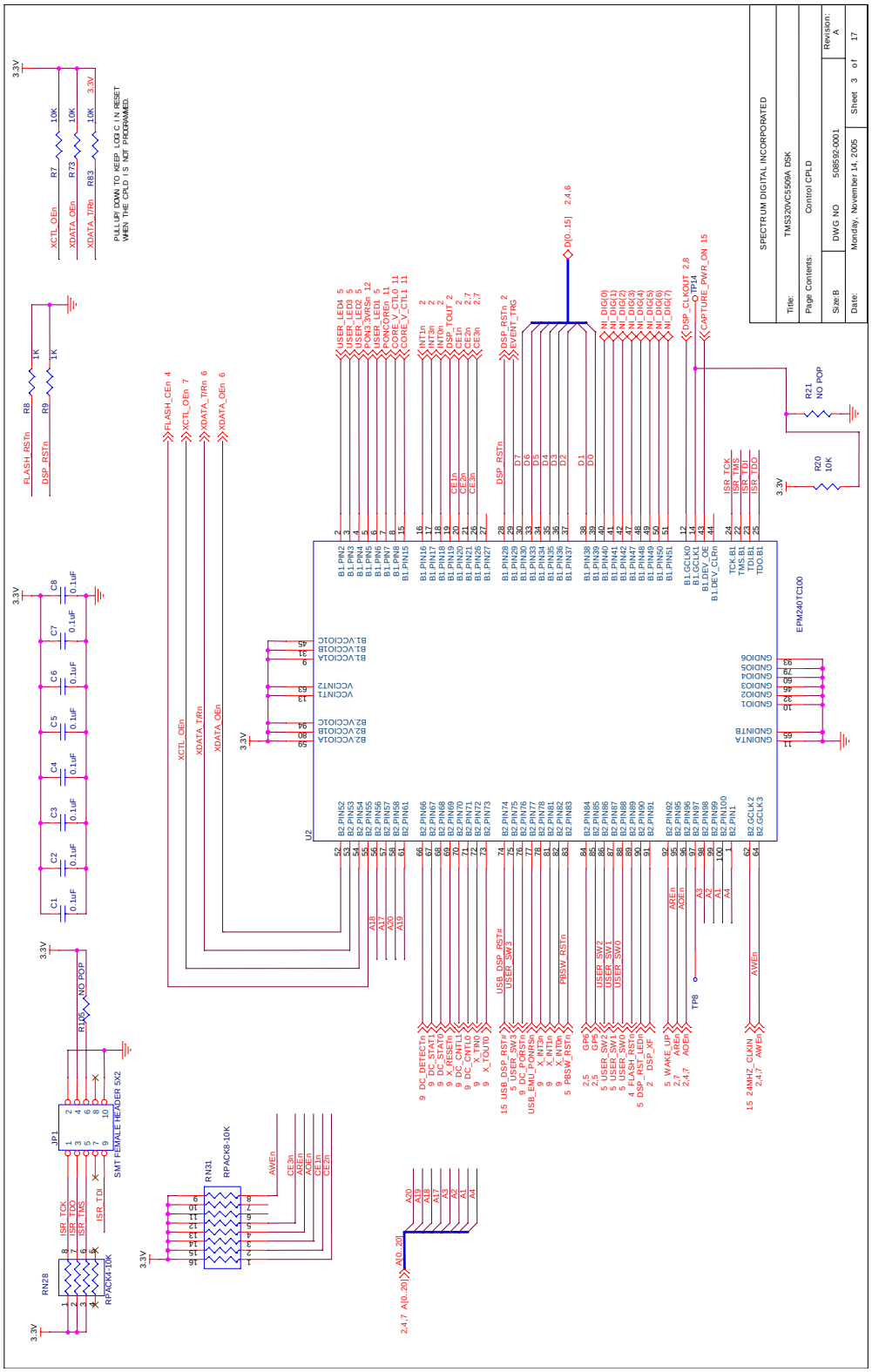
Page Contents: TMS320VC5509 DSP
Size: B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 2 of 17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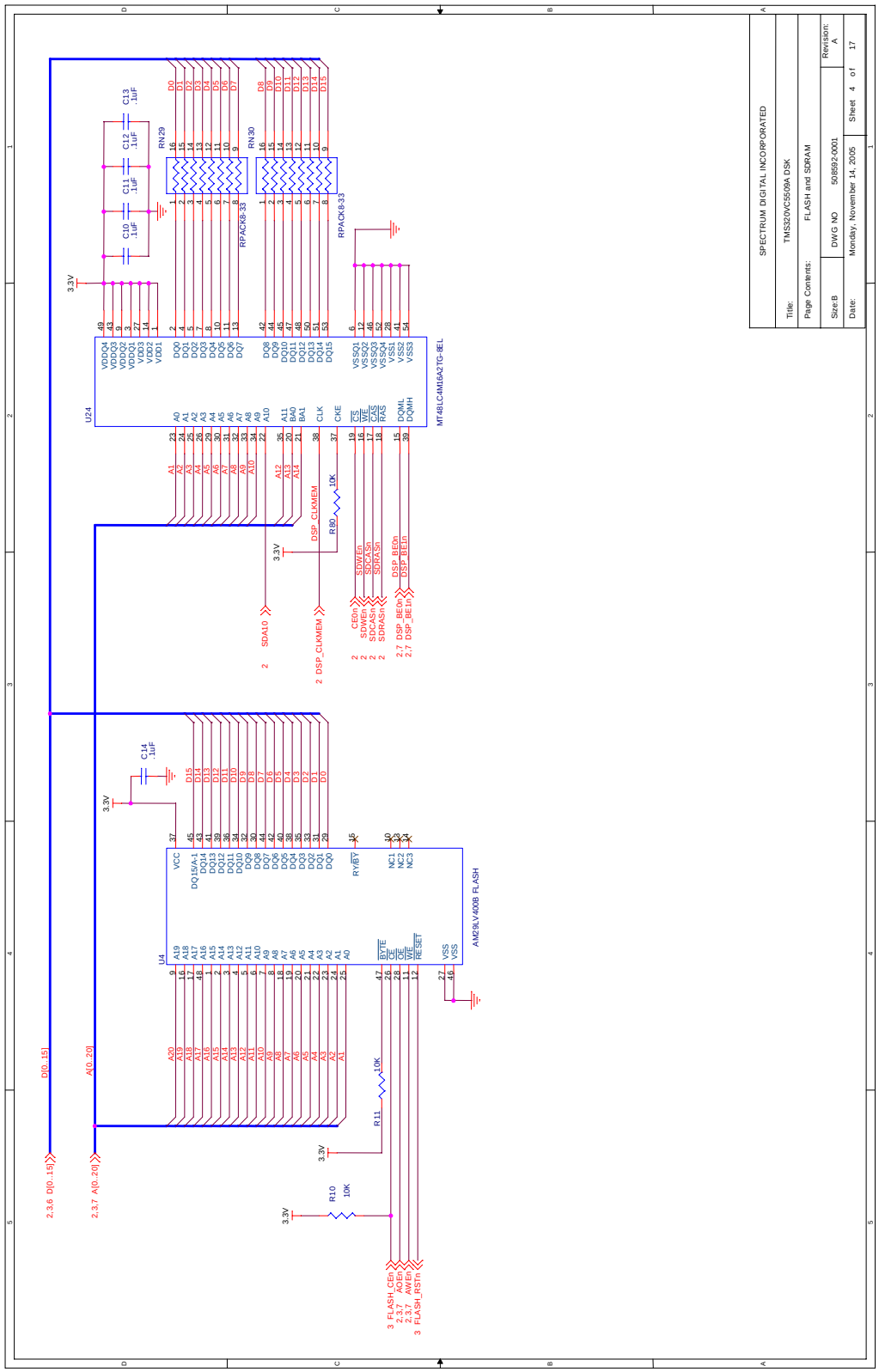
Page Contents: Control CPLD
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 3 of 17
PULL UP/ DOWN TO KEEP LOGIC IN RESET WHEN THE CPLD IS NOT PROGRAMMED
EPM2407TC100
RPACK4-10K
RPACK8-10K
SMT FEMALE HEADER 5X2
U2
JP1
RN28
RN31
R105
NO POP
R8
R9
1K
R7
R73
R83
10K
R21
R20
C1
C2
C3
C4
C5
C6
C7
C8
0.1uF
TP4
TP8
FLASH_CEn 4
XCTL_OEn 7
XDATA_TiRn 6
XDATA_OEn 6
FLASH_RSTn
DSP_RSTn
XCTL_OEn
XDATA_OEn
XDATA_TiRn
ISR_TCK
ISR_TDO
ISR_TMS
ISR_TDI
AWEn
CE3n
AREn
AOEn
CE1n
CE0n
A[0..20]
D[0..15] 2,4,6
3.3V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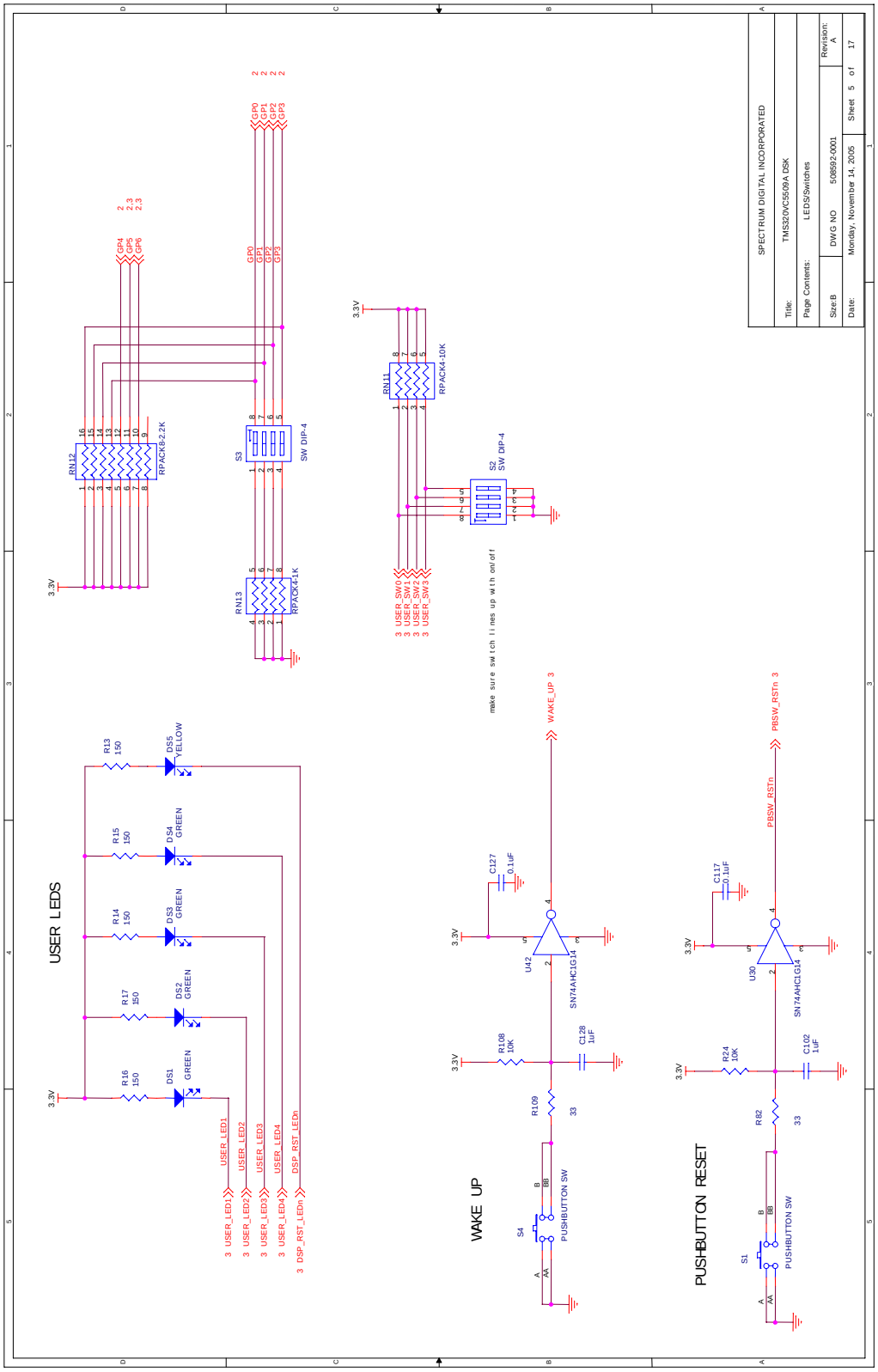
Page Contents: FLASH and SDRAM
Size: B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 4 of 17
U24
MT48LC4M16A2TG-8EL
U4
AM29LV400B FLASH
RPACK8-33
RN29
RN30
C10 .1uF
C11 .1uF
C12 .1uF
C13 .1uF
C14 .1uF
R10 10K
R11 10K
R80 10K
3.3V
DSP_CLKMEM
SDA10
CEDn
SDWEn
SDCASn
SDRASn
DSP_BE0n
DSP_BE1n
D[0..15]
A[0..20]
FLASH_CEn
AOEn
AWEn
FLASH_RSTn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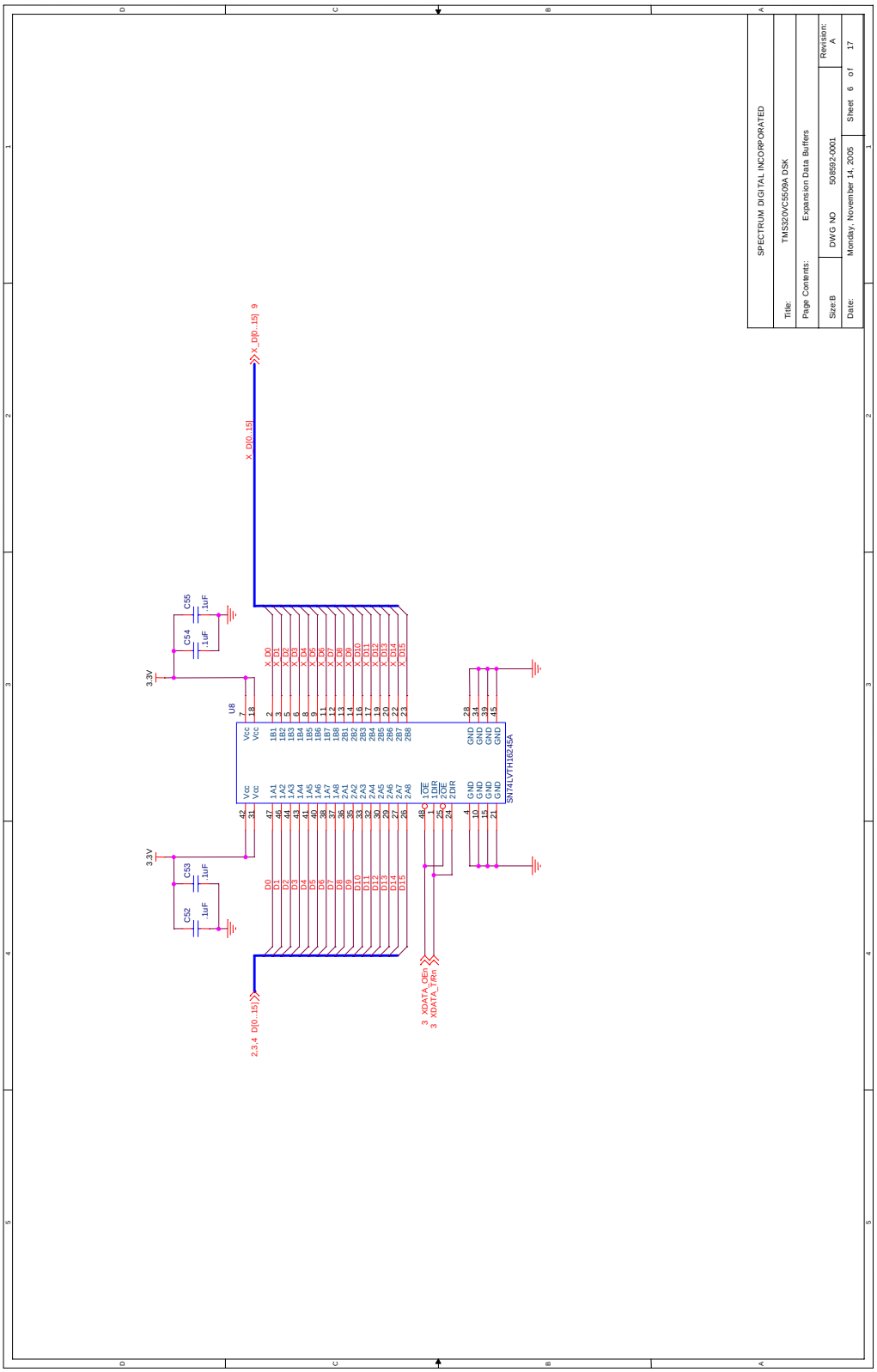
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 5 of 17
USER LEDS
WAKE UP
PUSHBUTTON RESET
make sure switch lines up with on/off
3.3V
R13 150
R15 150
R14 150
R17 150
R16 150
DS5 YELLOW
DS4 GREEN
DS3 GREEN
DS2 GREEN
DS1 GREEN
USER_LED1
USER_LED2
USER_LED3
USER_LED4
DSP_RST_LEDn
RN12 RPACK8-2.2K
RN13 RPACK4-1K
RN11 RPACK4-10K
S3 SW DIP-4
S2 SW DIP-4
USER_SW0
USER_SW1
USER_SW2
USER_SW3
GP0
GP1
GP2
GP3
GP4
GP5
GP6
WAKE_UP
C127 0.1uF
U42 SN74AHC1G14
R108 10K
C128 1uF
R109 33
S4 PUSHBUTTON SW
PBSW_RSTn
C117 0.1uF
U30 SN74AHC1G14
R24 10K
C102 1uF
R82 33
S1 PUSHBUTTON SW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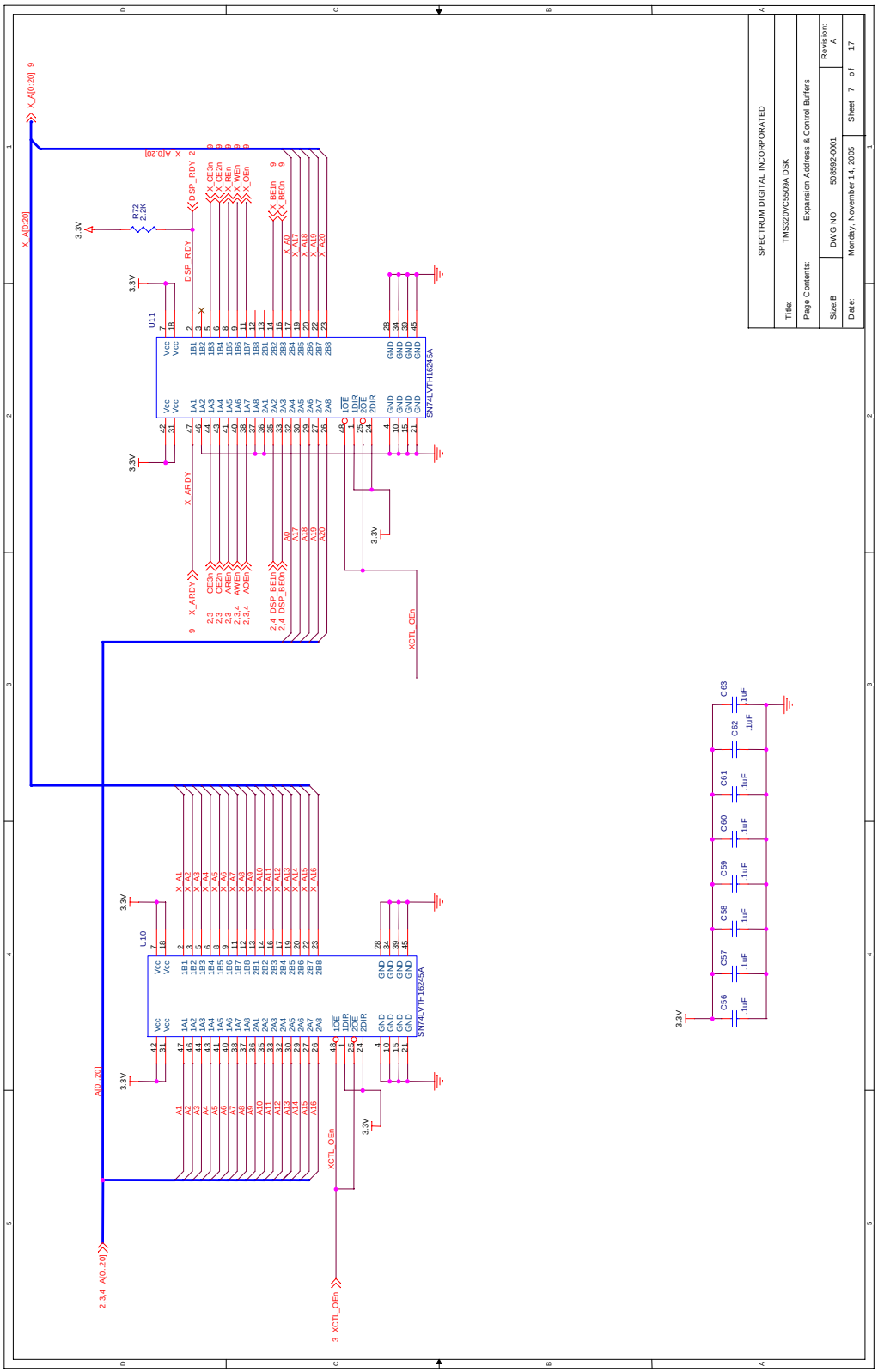
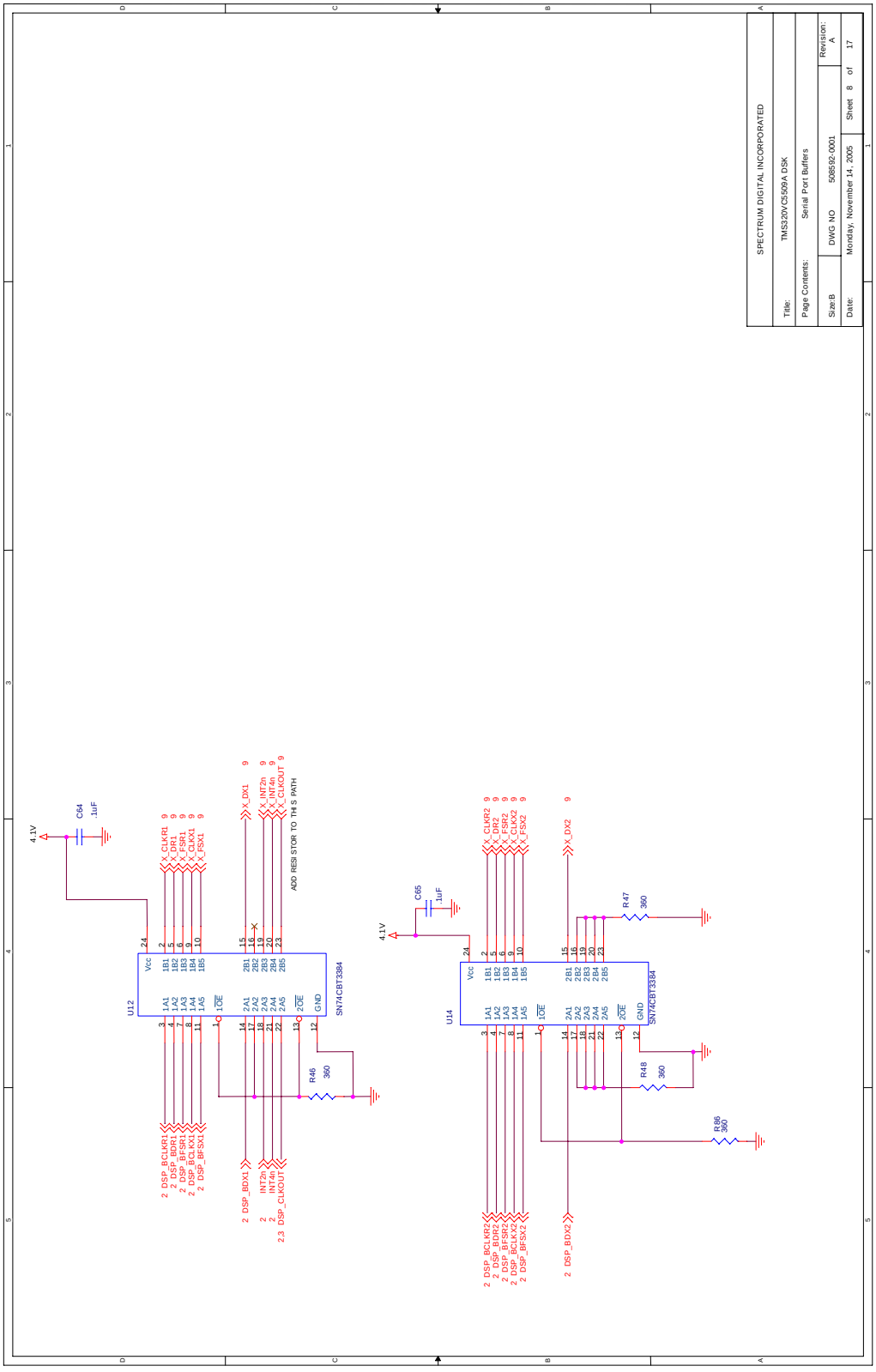
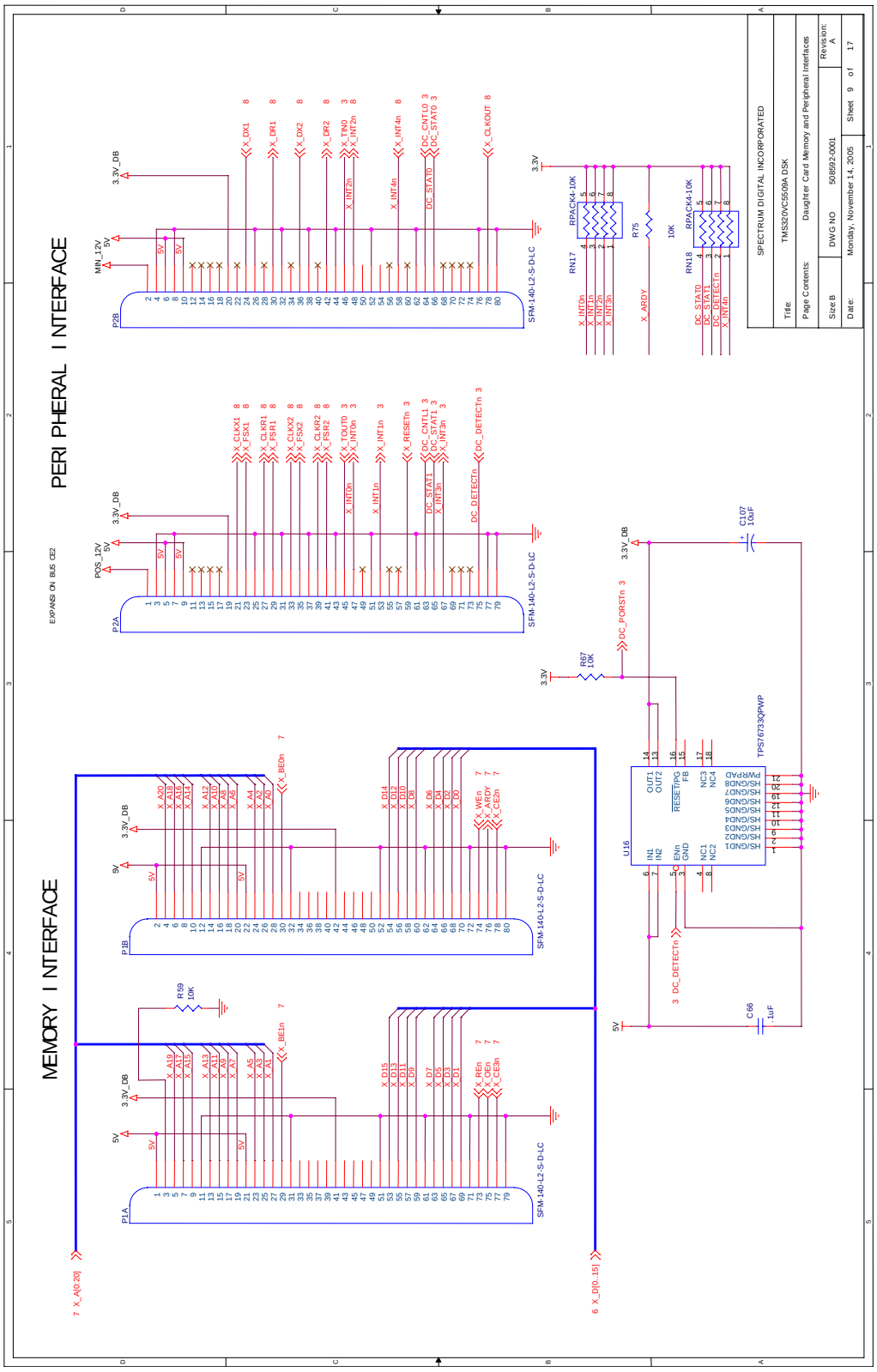
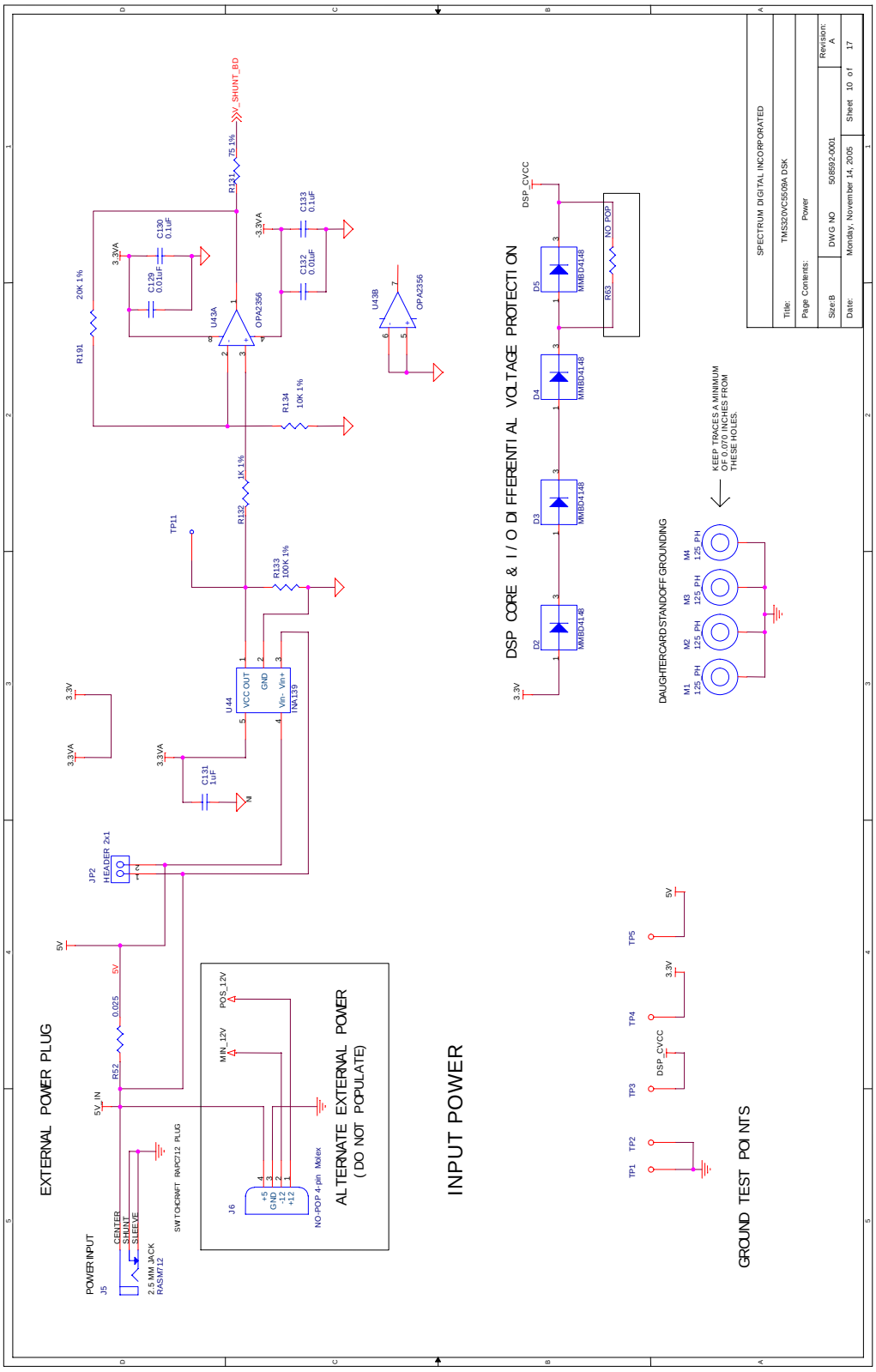
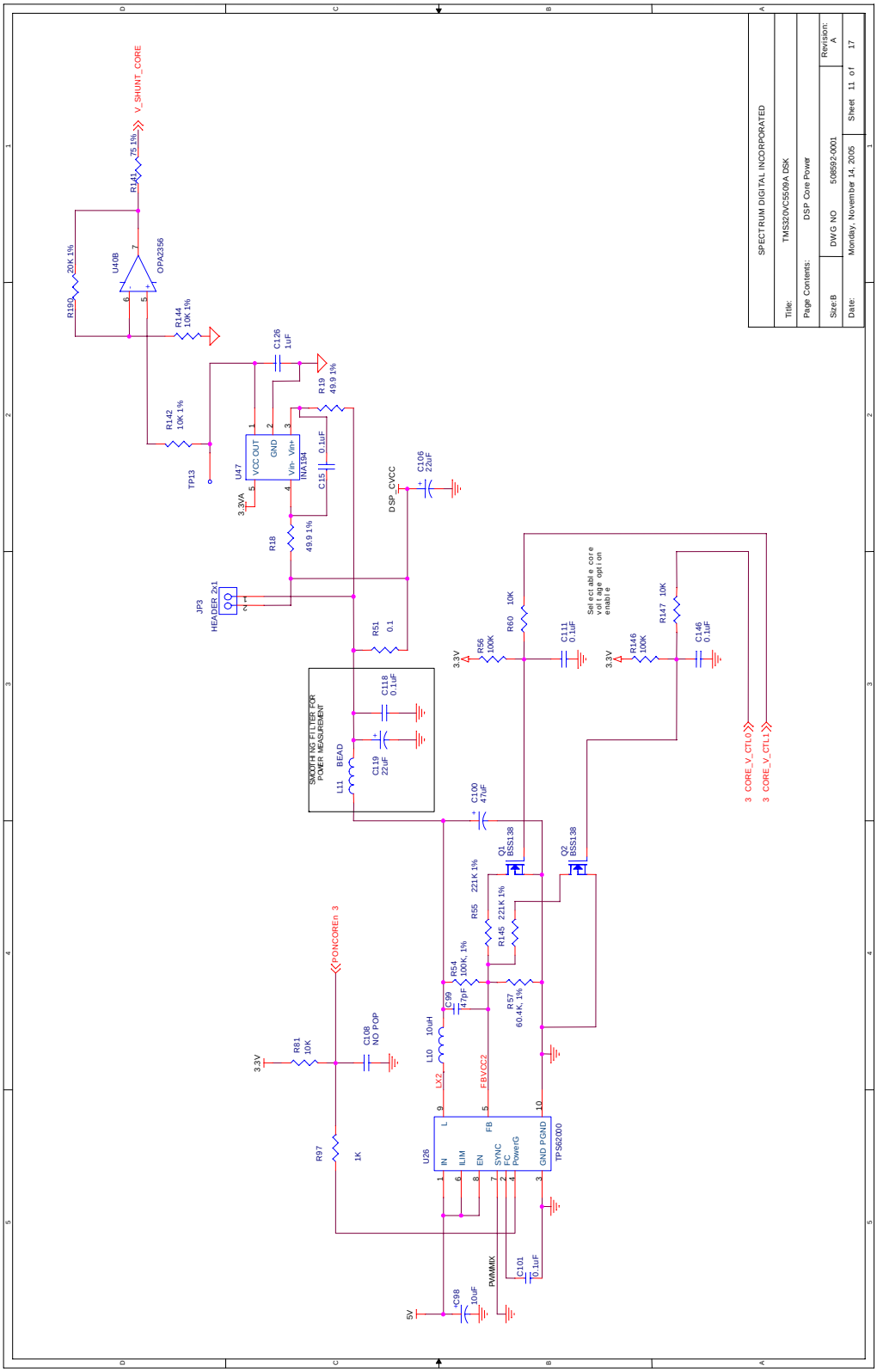
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 6 of 17
X_D[0..15] 9
2,3,4 D[0..15]
3 XDATA_OEn
3 XDATA_TiRn
U8
SN74LVTH162245A
C55 .1uF
C54 .1uF
C53 .1uF
C52 .1uF
3.3V

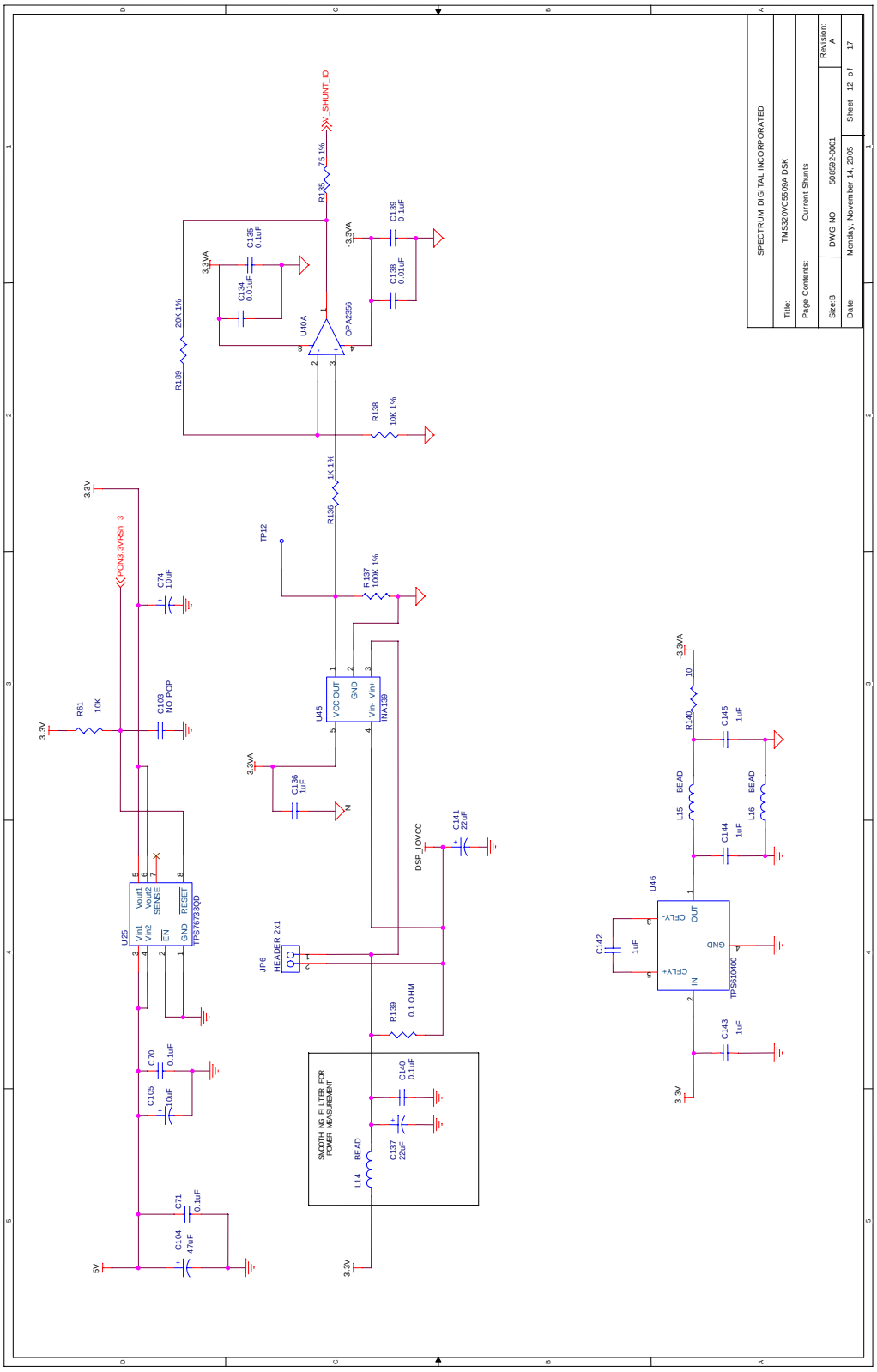

SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Expansion Address & Control Buffers
Size: B
DWG NO 508992-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 7 of 17
X_A[0:20] 9
A[0:20]
DSP_RDY 2
X_CE3n 9
X_CE2n 9
X_CE1n 9
X_AREn 9
X_WEn 9
X_OEn 9
X_BE1n 9
X_BE0n 9
X_A17 9
X_A18 9
X_A19 9
X_A20 9
R72 2.2K
3.3V
U11
SN74LVTH16245A
X_ARDY
9 X_ARDY
2.3 CE3n
2.3 CE2n
2.3 CE1n
2.3 ARE
2.3.4 AWEn
2.3.4 AOEn
2.4 DSP_BE1n
2.4 DSP_BE0n
A0
A17
A18
A19
A20
XCTL_OEn
U10
SN74LVTH16245A
A[0:20]
2.3.4 A[0:20]
3 XCTL_OEn
C56 .1uF
C57 .1uF
C58 .1uF
C59 .1uF
C60 .1uF
C61 .1uF
C62 .1uF
C63 .1uF

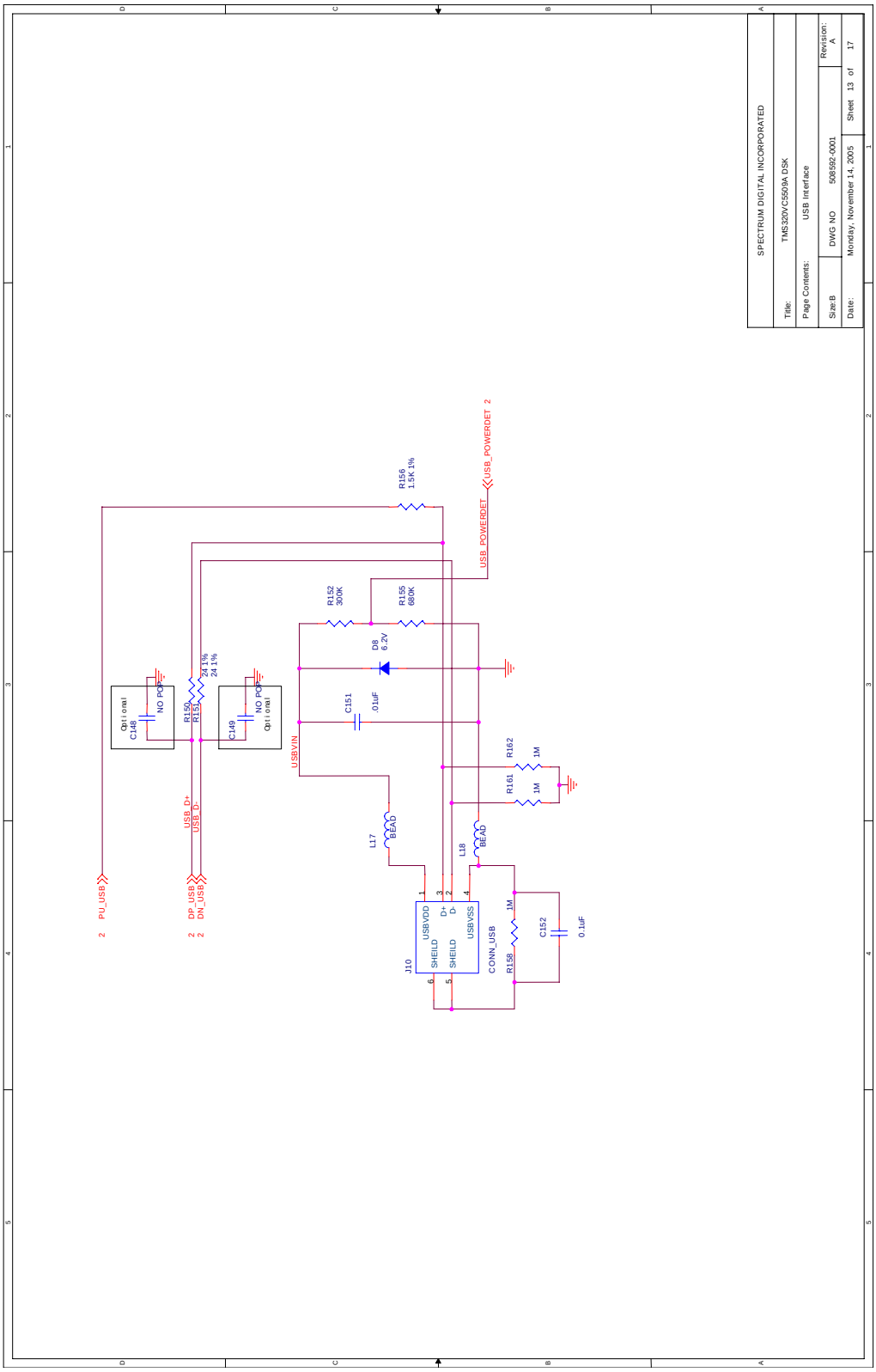

SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Serial Port Buffers
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 8 of 17
ADD RESISTOR TO THIS PATH
U12
U14
SN74CBT3384
4.1V
C64 .1uF
C65 1uF
R46 360
R47 360
R48 360
R86 360
X_CLKR1
X_DR1
X_FSR1
X_CLKX1
X_FSX1
X_DX1
X_INT2n
X_NMI/AIS
X_CLKOUT
X_CLKR2
X_DR2
X_FSR2
X_CLKX2
X_FSX2
X_DX2
2 DSP_BCLKR1
2 DSP_BDR1
2 DSP_BFSR1
2 DSP_BCLKX1
2 DSP_BFSX1
2 DSP_BDX1
2 DSP_CLKOUT
2 DSP_BCLKR2
2 DSP_BDR2
2 DSP_BFSR2
2 DSP_BCLKX2
2 DSP_BFSX2
2 DSP_BDX2

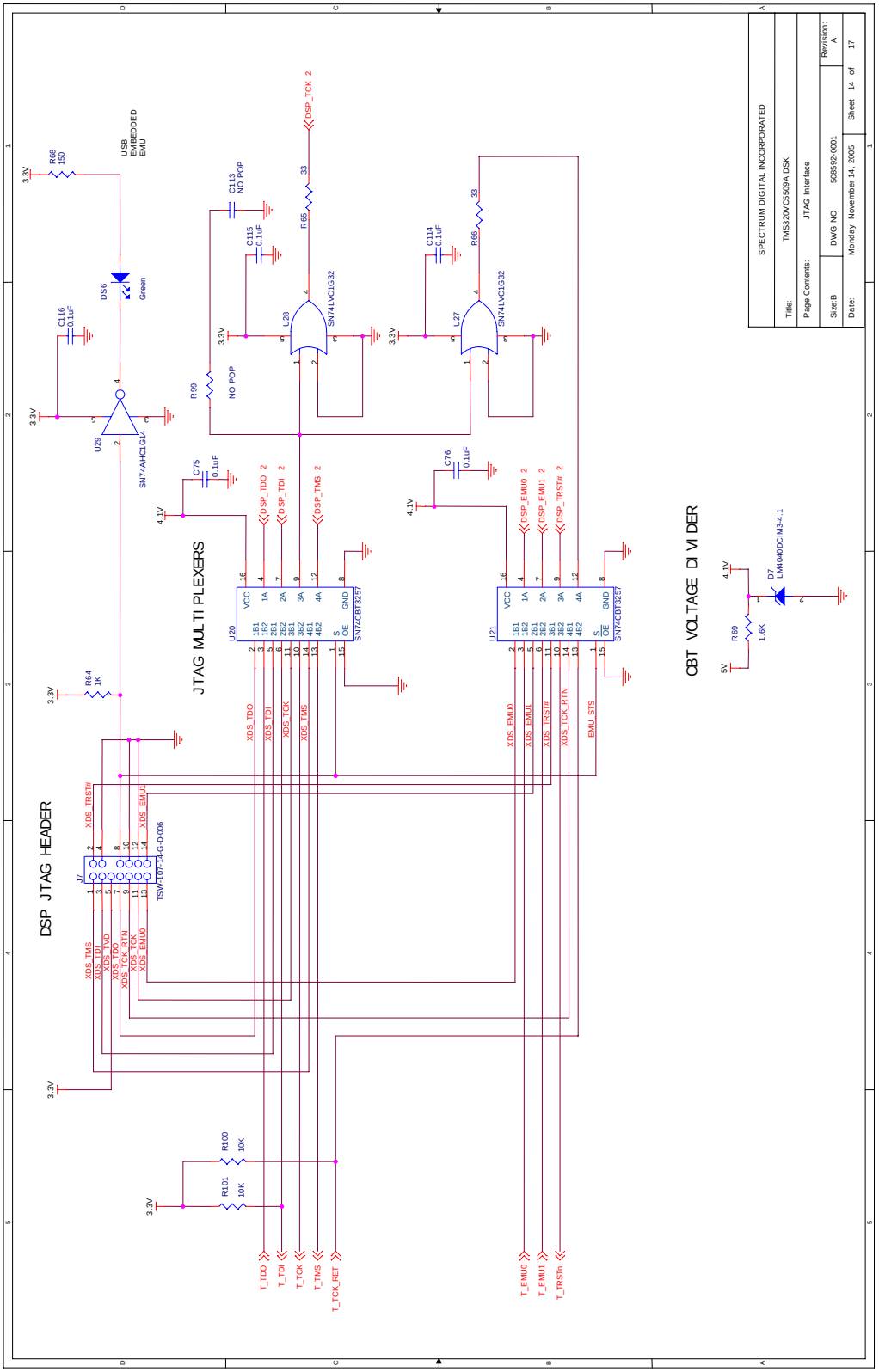

PERIPHERAL INTERFACE
MEMORY INTERFACE
EXPANSION BUS CE2
SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Daughter Card Memory and Peripheral Interfaces
Size: B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 9 of 17
SFM-140-L2-S-D-LC
P1A
P1B
P2A
P2B
U16
TPS76733QPWP
RPACK4-10K
RN17
RN18
R59 10K
R67 10K
R75 10K
C107 10uF
C66 .1uF
3.3V_DB
MIN_12V
POS_12V
X_A[0-20]
X_D[0..15]
X_DX1
X_DR1
X_DX2
X_DR2
X_TIN0
X_INT2n
X_INT4n
X_CLKOUT
X_CLKX1
X_FSX1
X_CLKR1
X_FSR1
X_CLKX2
X_FSX2
X_CLKR2
X_FSR2
X_TOUT0
X_INT0n
X_INT1n
X_RESETn
X_INT3n
X_ARDY
DC_DETECTn
DC_PORSTn
DC_CNTL0
DC_CNTL1
DC_STAT0
DC_STAT1
X_BE0n
X_BE1n
X_WEn
X_OEn
X_CE2n
X_CE3n

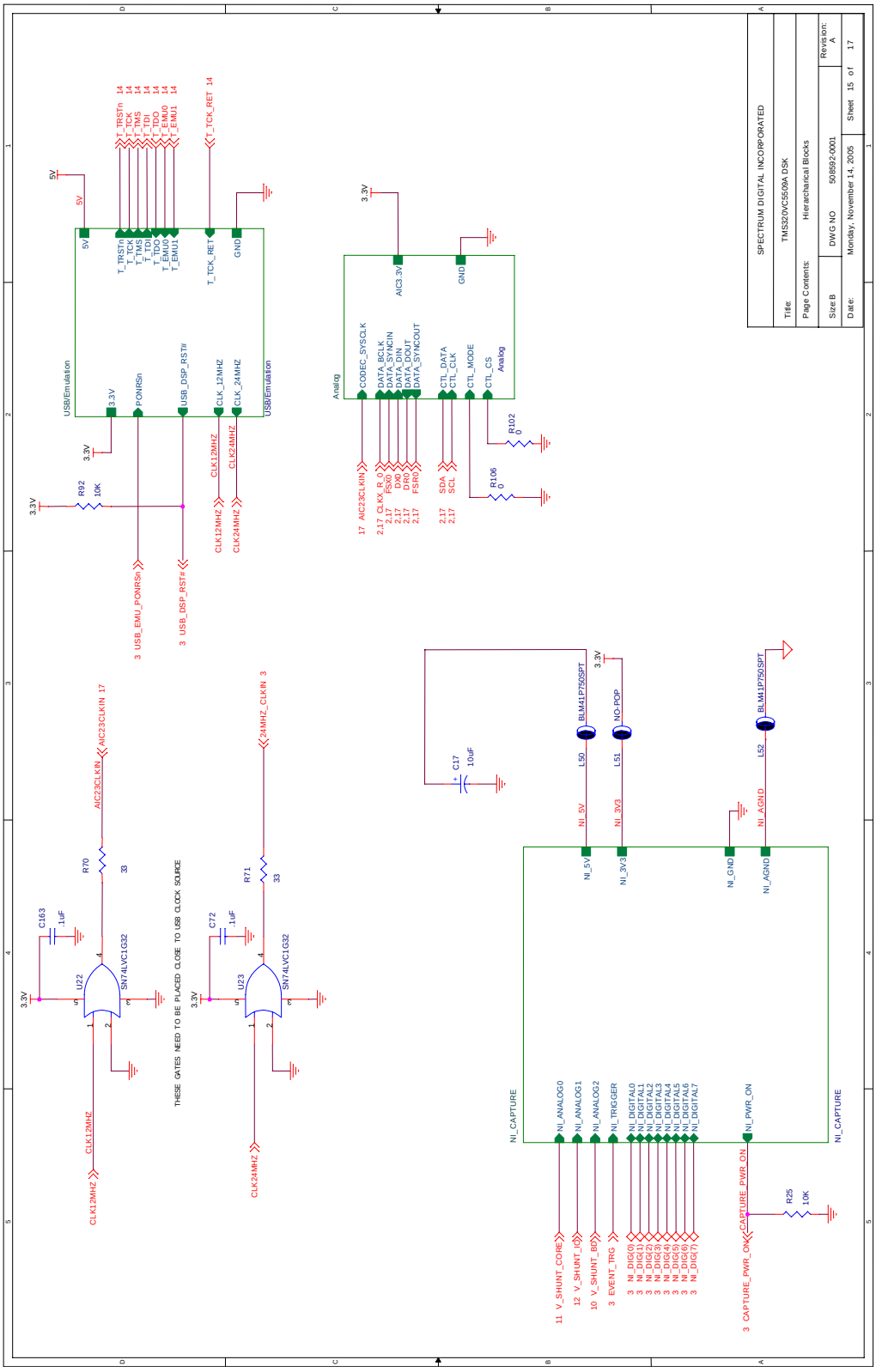

EXTERNAL POWER PLUG
ALTERNATE EXTERNAL POWER
(DO NOT POPULATE)
INPUT POWER
DSP CORE & I/O DIFFERENTIAL VOLTAGE PROTECTION
DAUGHTERCARD STANDOFF GROUNDING
GROUND TEST POINTS
KEEP TRACES A MINIMUM OF 0.070 INCHES FROM THESE HOLES.
SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Power
Size: B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 10 of 17

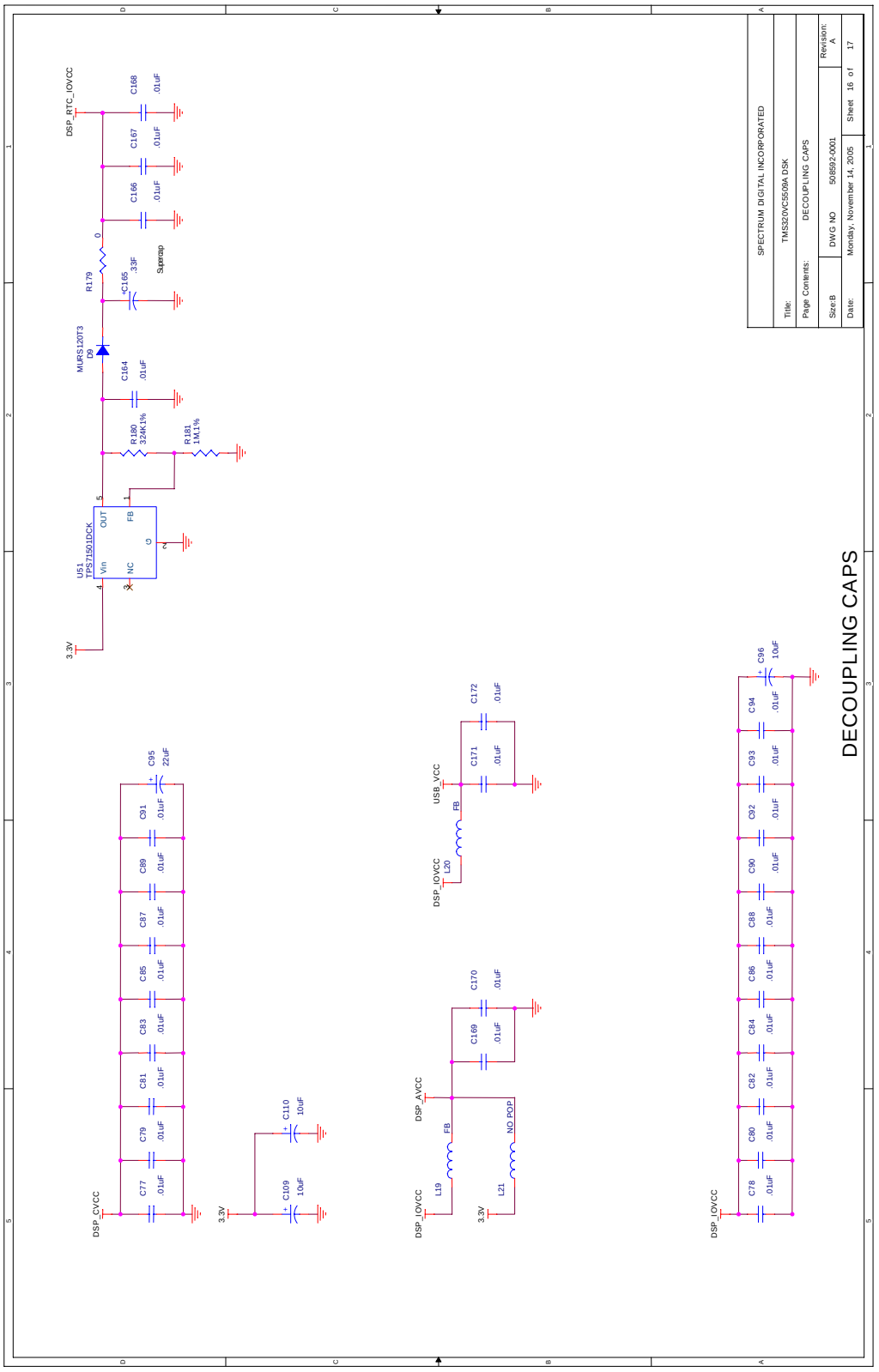

SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: DSP Core Power
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 11 of 17
V_SHUNT_CORE
R143 .75 1%
U40B
OPA2356
R190 20K 1%
R144 10K 1%
R142 10K 1%
TP13
C126 1uF
R19 49.9 1%
U47
VCC OUT
GND
Vin- Vin+
INA194
C15 0.1uF
3.3VA
R18 49.9 1%
C106 22uF
DSP_CVCC
JP3
HEADER 2x1
R51 0.1
SHOTTKY DIODE FOR POWER MEASUREMENT
L11 BEAD
C118 0.1uF
C119 22uF
C100 47uF
Select able core voltage option enable
R56 100K
R60 10K
C111 0.1uF
R146 100K
R147 10K
C146 0.1uF
3.3V
3 CORE_V_CTL0
3 CORE_V_CTL1
Q1 BSS138
Q2 BSS138
R55 221K 1%
R145 221K 1%
R54 100K 1%
R57 60.4K 1%
C99 47pF
PONCOREn 3
R81 10K
C108 NO POP
L10 10uH
LX2
FBVCC2
R97 1K
U26
IN
ILIM
EN
L
FB
SYNC
FC
PowerG
GND PGND
TPS62000
PWMMIX
C101 0.1uF
C98 10uF
5V

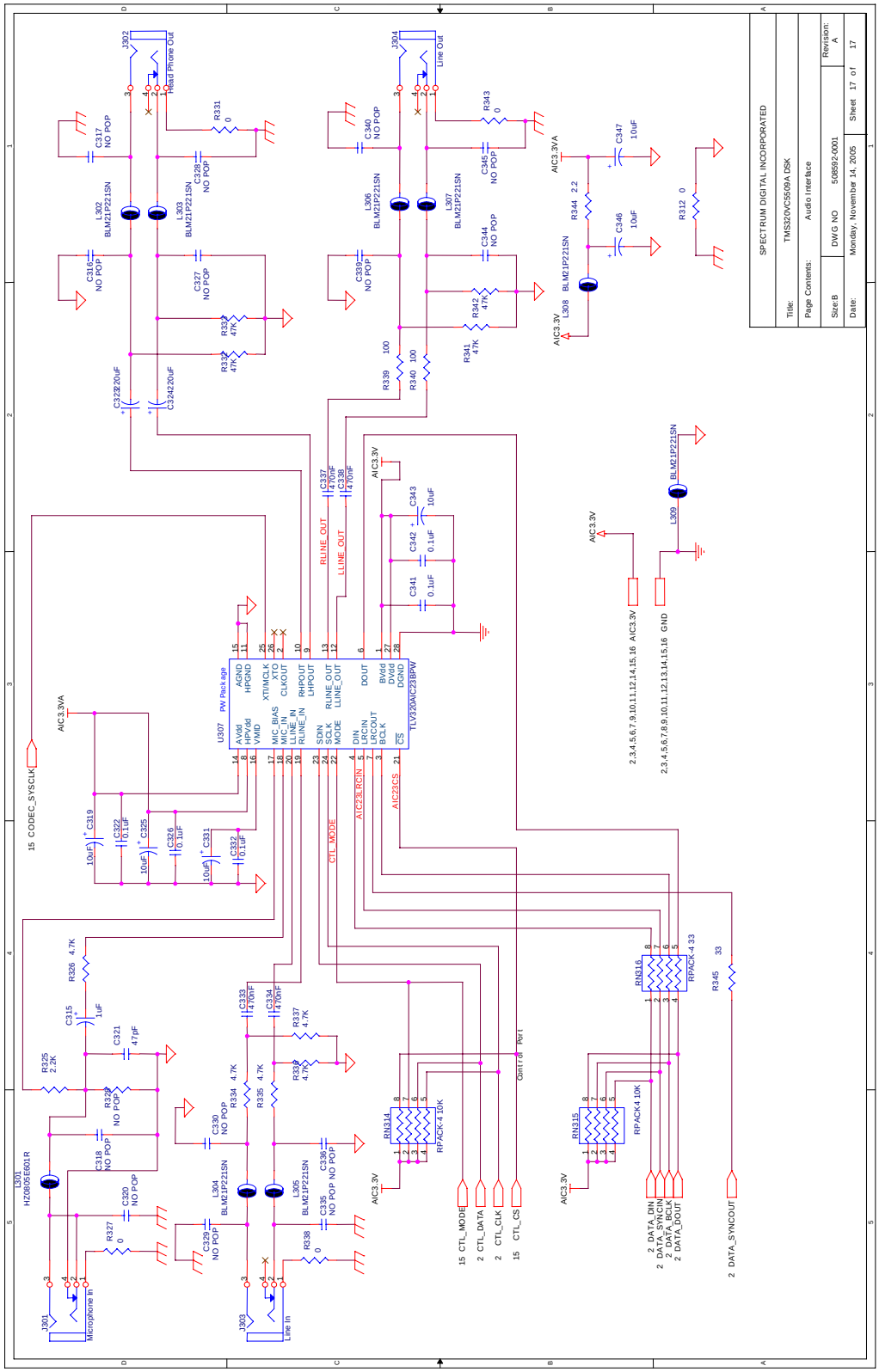

SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Current Shants
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 12 of 17
I_SHUNT_IO
R135 .75 1%
C139 0.1uF
C135 0.1uF
C134 0.01uF
C138 0.01uF
U40A OPA2356
R189 20K 1%
R138 10K 1%
R136 1K 1%
TP12
R137 100K 1%
U45 INA139
C136 1uF
DSP_IOVCC
C141 22uF
JP6 HEADER 2x1
R139 0.1 OHM
SMOOTH NG FILTER FOR POWER MEASUREMENT
L14 BEAD
C137 22uF
C140 0.1uF
3.3V
5V
PON3.3VRSn
C74 10uF
R61 10K
C103 NO POP
U25 TPS767330D
C70 0.1uF
C105 1.0uF
C71 0.1uF
C104 47uF
-3.3VA
R140 10
C145 1uF
L15 BEAD
L16 BEAD
C144 1uF
U46 TPS610400
C142 1uF
C143 1uF


SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: USB Interface
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 13 of 17
R156 1.5K 1%
USB_POWERDET
R152 300K
R155 680K
D8 6.2V
C151 .01uF
R150 24.1%
R151 24.1%
Optional C148 NO POP
Optional C149 NO POP
USBVIN
R162 1M
R161 1M
L17 BEAD
L18 BEAD
PU_USB
DP_USB
DN_USB
USB_D+
USB_D-
J10
USBVDD
D+
D-
USBVSS
SHEILD
SHEILD
CONN_USB
R158 1M
C152 0.1uF


SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: JTAG Interface
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 14 of 17
DSP JTAG HEADER
JTAG MULTIPLEXERS
CBT VOLTAGE DIVIDER
USB EMBEDDED EMU
SN74AHC1G14
SN74LVC1G32
SN74CBT3257
LM4040DIM3-4.1
TSW-107-14-G-D-006
XDS_TMS
XDS_TDI
XDS_TVD
XDS_TCK_RTN
XDS_TCK
XDS_EMU0
XDS_TRST#
XDS_EMU1
XDS_TDO
XDS_TDI
XDS_TCK
XDS_TMS
XDS_TCK_RTN
EMU_STS
XDS_EMU0
XDS_EMU1
XDS_TRST#
DSP_TDO 2
DSP_TDI 2
DSP_TMS 2
DSP_TCK 2
DSP_EMU0 2
DSP_EMU1 2
DSP_TRST# 2
T_TDO
T_TDI
T_TCK
T_TMS
T_TCK_RET
T_EMU0
T_EMU1
T_TRSTn
3.3V
4.1V
5V
NO POP


SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Hierarchical Blocks
Size: B
DWG NO: 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 15 of 17
USB/Emulation
T_TRSTn
T_TCK
T_TMS
T_TDI
T_TDO
T_EMU0
T_EMU1
T_TCK_RET
GND
3.3V
PONRSn
USB_DSP_RST#
CLK_12MHZ
CLK_24MHZ
R92
10K
3 USB_EMU_PONRSn
3 USB_DSP_RST#
CLK12MHZ
CLK24MHZ
Analog
AIC3.3V
CODEC_SYSCLK
DATA_BCLK
DATA_SYNCIN
DATA_DIN
DATA_DOUT
DATA_SYNCOUT
CTL_DATA
CTL_CLK
CTL_MODE
CTL_CS
R102
0
R106
0
17 AIC23CLKIN
2.17 CLKX_R_0
2.17 FSX0
2.17 DX0
2.17 DR0
2.17 FSR0
2.17 SDA
2.17 SCL
C17
10uF
BLM41P750SPT
L50
L51
L52
NO-POP
NI_5V
NI_3V3
NI_AGND
NI_GND
NI_CAPTURE
NI_ANALOG0
NI_ANALOG1
NI_ANALOG2
NI_TRIGGER
NI_DIGITAL0
NI_DIGITAL1
NI_DIGITAL2
NI_DIGITAL3
NI_DIGITAL4
NI_DIGITAL5
NI_DIGITAL6
NI_DIGITAL7
NI_PWR_ON
CAPTURE_PWR_ON
R25
10K
11 V_SHUNT_CORE
12 V_SHUNT_IO
10 V_SHUNT_BAT
3 EVENT_TRG
3 CAPTURE_PWR_ON
AIC23CLKIN
24MHZ_CLKIN
R70
33
R71
33
C163
.1uF
C72
.1uF
U22
U23
SN74LVC1G32
THESE GATES NEED TO BE PLACED CLOSE TO USB CLOCK SOURCE

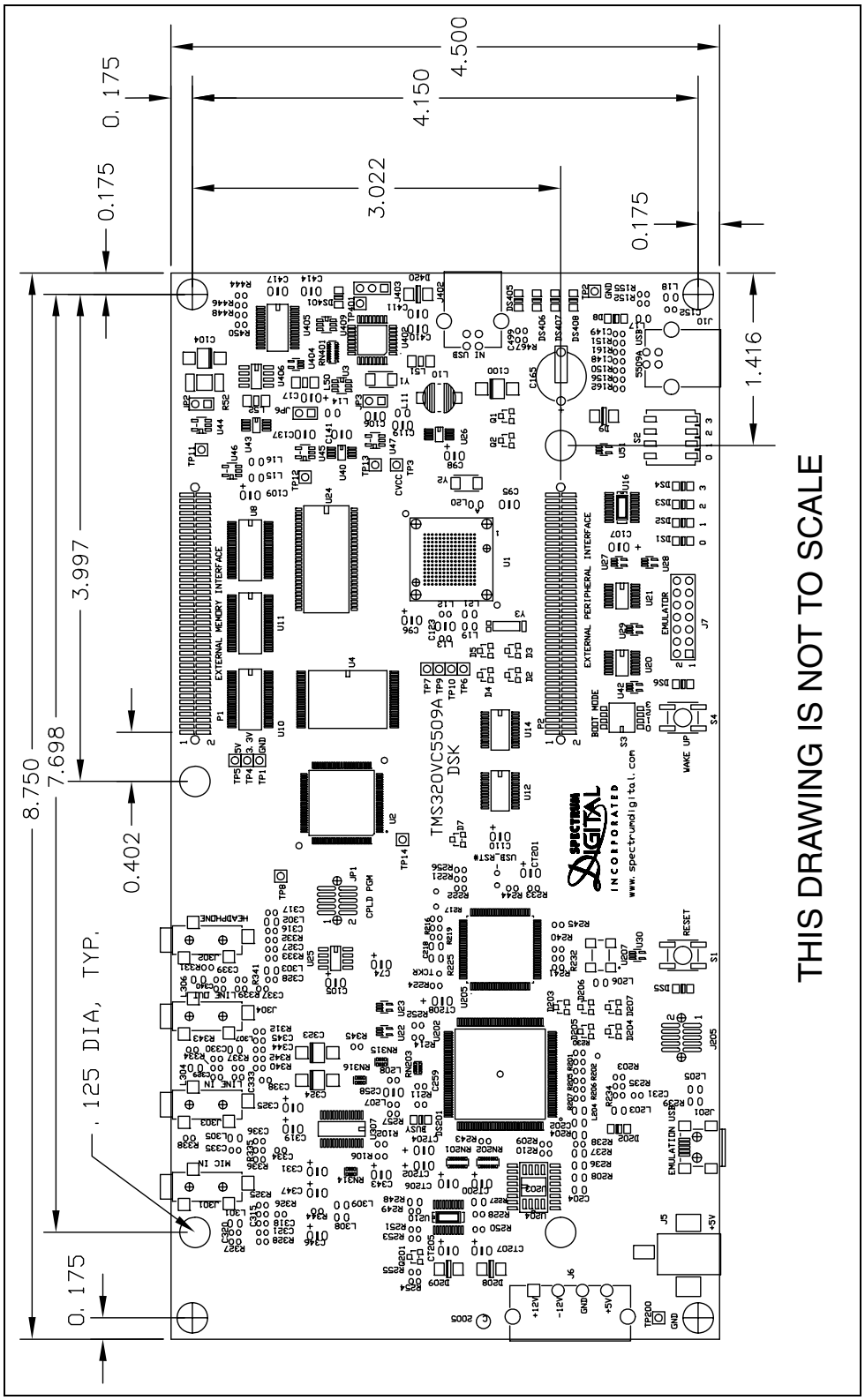

DECOUPLING CAPS
SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: DECOUPLING CAPS
Size: B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 16 of 17
DSP_RTC_IOVCC
C168 .01uF
C167 .01uF
C166 .01uF
R179 0
C165 .33F Supercap
MURS120T3 D9
C164 .01uF
R180 324K1%
R181 1M,1%
U51 TPS71501DCK
OUT FB Vin NC GND
3.3V
C95 22uF
C91 .01uF
C89 .01uF
C87 .01uF
C85 .01uF
C83 .01uF
C81 .01uF
C79 .01uF
C77 .01uF
DSP_CVCC
C110 10uF
C109 10uF
3.3V
C172 .01uF
C171 .01uF
USB_VCC
FB
L20
DSP_IOVCC
C170 .01uF
C169 .01uF
DSP_AVCC
FB
L19
NO_POP
L21
3.3V
C96 10uF
C94 .01uF
C93 .01uF
C92 .01uF
C90 .01uF
C88 .01uF
C86 .01uF
C84 .01uF
C82 .01uF
C80 .01uF
C78 .01uF
DSP_IOVCC


SPECTRUM DIGITAL INCORPORATED
Title: TMS320VC5509A DSK
Page Contents: Audio Interface
Size:B
DWG NO 508592-0001
Revision: A
Date: Monday, November 14, 2005
Sheet 17 of 17
Head Phone Out
Line Out
Microphone In
Line In
Control Port
TLV320AIC23BPW
15 CODEC_SYSCLK
15 CTL_MODE
2 CTL_DATA
2 CTL_CLK
15 CTL_CS
2 DATA_DIN
2 DATA_SYNCIN
2 DATA_BCLK
2 DATA_DOUT
2 DATA_SYNCOUT

Appendix B

Mechanical Information

This appendix contains the mechanical information about the TMS320VC5509A DSK produced by Spectrum Digital.


4.500
4.150
3.022
0.175
0.175
0.175
1.416
8.750
7.698
3.997
0.402
0.175
.125 DIA, TYP.
THIS DRAWING IS NOT TO SCALE
TMS320VC5509A
DSK
EXTERNAL MEMORY INTERFACE
EXTERNAL PERIPHERAL INTERFACE
EMULATOR
BOOT MODE
WAKE UP
RESET
CPLD PGM
HEADPHONE
LINE IN
MIC IN
EMULATION USB
SPECTRUM DIGITAL INCORPORATED
www.spectrumdigital.com

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