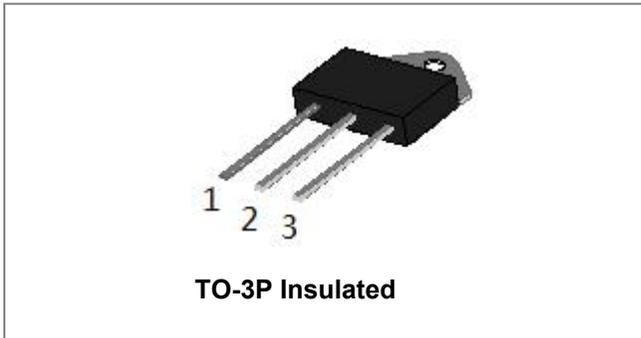
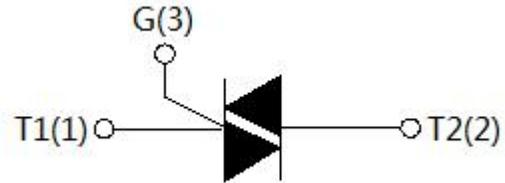


SST41 Series 40A TRIACs



Circuit Diagram



Description

With high ability to withstand the shock loading of large current, SST41 series triacs provide high dv/dt rate with strong resistance to electromagnetic interference. With high commutation performances, 3 quadrant products especially recommended for use on inductive load. From all three terminals to external heatsink, SST41Z provides a rated insulation voltage of 2500 V_{RMS}.

Maximum Ratings:

Characteristics	Symbol	Condition	Max.	Units
Storage junction temperature range	T _J	-	-40 to +125	°C
Operating junction temperature range	T _{stg}	-	-40 to +150	°C
Repetitive peak off-state voltage	V _{DRM}	-	600/800/1200/1600	V
Repetitive peak reverse voltage	V _{RRM}	-	600/800/1200/1600	V
Non repetitive peak off-state voltage	V _{DSM}	-	V _{DRM} +100	V
Non repetitive peak reverse voltage	V _{RSM}	-	V _{RRM} +100	V
RMS on-state current	I _(TRMS)	TO-3P(Ins)(T _C =80°C)	40	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)	I _{TSM}	-	400	A
I ² t value for fusing (tp=10ms)	I ² t	-	880	A ² s
Critical rate of rise of on-state current (I _G =2×I _{GT})	di/dt	-	50	A/us
Peak gate current	I _{GM}	-	4	A
Average gate power dissipation	P _{GM}	-	1	W
Peak gate power	P _{G(AV)}	-	10	W

Electrical Characteristics ($T_j=25^\circ\text{C}$ unless otherwise specified)

3 Quadrants

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12\text{V } R_L=33\Omega$	I - II -III	MAX	50	mA
V_{GT}		I - II -III	MAX	1.3	V
V_{GD}	$V_D=V_{DRM} T_j=125^\circ\text{C } R_L=3.3\text{K}\Omega$	I - II -III	MIN	0.2	V
I_L	$I_G=1.2I_{GT}$	I -III	MAX	80	mA
		II		100	
I_H	$I_T=100\text{mA}$		MAX	60	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ\text{C}$		MIN	1500	V/ μs

4 Quadrants

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12\text{V } R_L=33\Omega$	I - II -III	MAX	50	mA
		IV		70	
V_{GT}		ALL	MAX	1.3	V
V_{GD}	$V_D=V_{DRM} T_j=125^\circ\text{C}, R_L=3.3\text{K}\Omega$	ALL	MIN	0.2	V
I_L	$I_G=1.2I_{GT}$	I -III-IV	MAX	90	mA
		II		100	
I_H	$I_T=100\text{mA}$		MAX	80	mA
dV/dt	$V_D=2/3V_{DRM}$ Gate Open $T_j=125^\circ\text{C}$		MIN	1000	V/ μs

Static Characteristics

Symbol	Condition	Max.	Units
V_{TM}	$I_T=60\text{A } t_p=380\mu\text{s}, T_j=25^\circ\text{C}$	1.5	V
I_{DRM}	$V_D=V_{DRM} V_R=V_{RRM}, T_j=25^\circ\text{C}$	10	μA
I_{RRM}	$V_D=V_{DRM} V_R=V_{RRM}, T_j=125^\circ\text{C}$	5	mA

Thermal Resistances

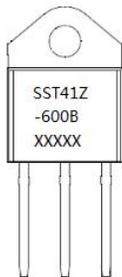
Symbol	Condition		Value	Units
$R_{th(j-c)}$	Junction to case(AC)	TO-3P(Ins)	1.1	$^\circ\text{C}/\text{W}$

Ordering Information

<p>S ST 41 Z -600 BW</p> <p>SMC Diode Solutions — S</p> <p>Triacs — ST</p> <p>$I_{T(RMS)}:40A$ — 41</p> <p>Z:TO-3P(Ins) — Z</p>	<p>-600 BW</p> <p>BW: $I_{GT1-3} \leq 50mA$ B: $I_{GT1-3} \leq 50mA$ $I_{GT4} \leq 70mA$</p> <p>600: $V_{DRM}/V_{RRM} \geq 600V$ 800: $V_{DRM}/V_{RRM} \geq 800V$ 1200: $V_{DRM}/V_{RRM} \geq 1200V$ 1600: $V_{DRM}/V_{RRM} \geq 1600V$</p>
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Device	Package	Shipping
SST41Z-600B/SST41Z-800B SST41Z-600BW/SST41Z-800BW SST41Z-1200BW/SST41Z-1600BW	TO-3P	30pcs/ Tube

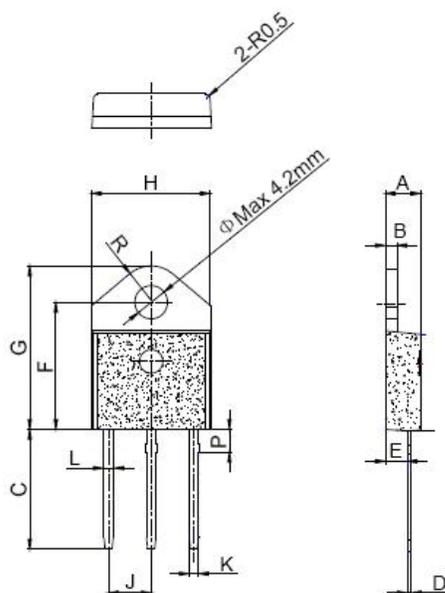
Marking Diagram



Where XXXXX is YYWWL

SST41Z-600B = Part name
YY = Year
WW = Week
L = Lot Number

Mechanical Dimensions TO-3P



SYMBOL	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	1.45		1.55	0.057		0.061
C	14.35		15.60	0.565		0.614
D	0.50		0.70	0.020		0.028
E	2.70		2.90	0.106		0.114
F	15.80		16.50	0.622		0.650
G	20.40		21.10	0.803		0.831
H	15.10		15.50	0.594		0.610
J	5.40		5.65	0.213		0.222
K	1.10		1.40	0.043		0.055
L	1.35		1.50	0.053		0.059
P	2.80		3.00	0.110		0.118
R		4.35			0.171	

Ratings and Characteristics Curves

FIG.1 Maximum power dissipation versus RMS on-state current

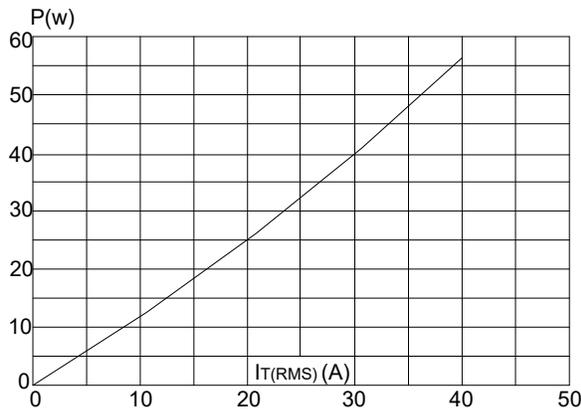


FIG.2: RMS on-state current versus case temperature

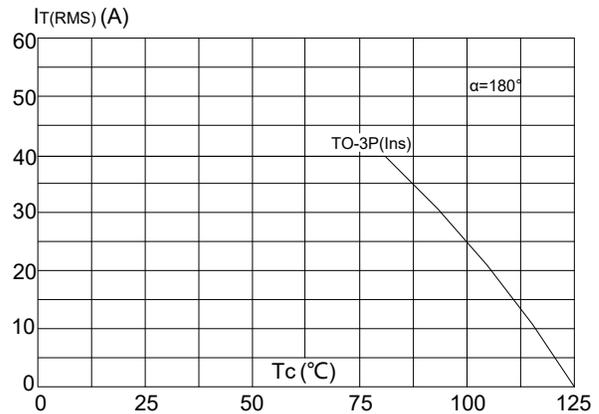


FIG.3: Surge peak on-state current versus number of cycles

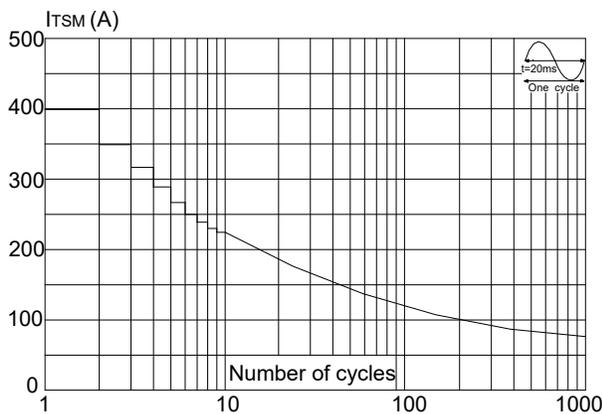


FIG.4: On-state characteristics (maximum values)

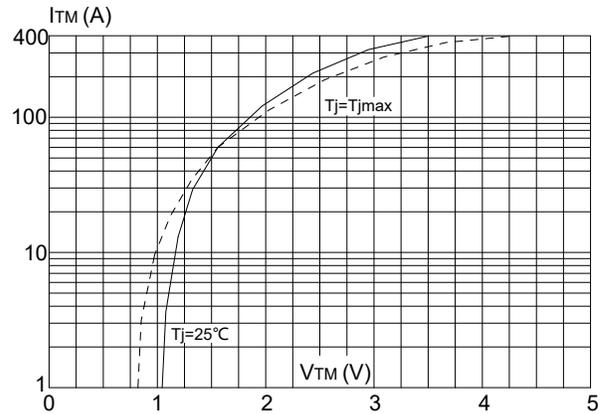


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of $I^2 t$ ($di/dt < 50\text{A}/\mu\text{s}$)

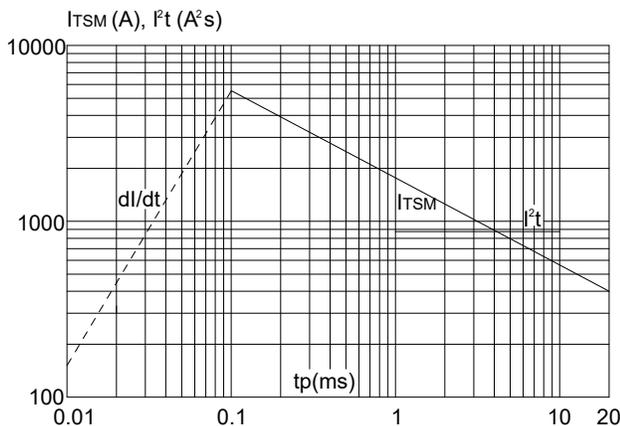
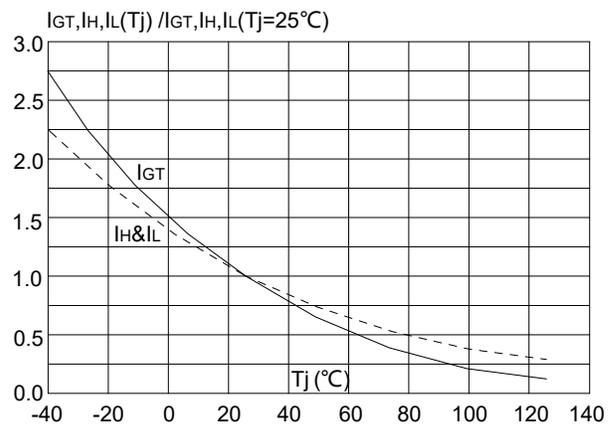


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature



Technical Data
Data Sheet N2034, Rev.-



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