ZL30691, ZL30692, ZL30693
1-, 2-, 3-Channel, 10-Input, 18-Output System Synchronizers

Product Brief

August 2019

Features

- **One, Two or Three DPLL Channels**

  - Timing compliance with ITU-T G.8262, G.813, G.812, G.8273.2; Telcordia GR-1244, GR-253

  - Programmable bandwidth, 0.1mHz to 470Hz

  - Freerun or holdover on loss of all inputs

  - Hitless reference switching

  - High-resolution holdover averaging

  - Per-DPLL phase adjustment, 1ps resolution

  - Programmable tracking range, phase-slope limiting, frequency-change limiting and other advanced features

- **Input Clocks**

  - Accepts up to 10 differential or CMOS inputs

  - Any input frequency from 0.5Hz to 900MHz

  - Per-input activity and frequency monitoring

  - Automatic or manual reference switching

  - Revertive or nonrevertive switching

  - Any input can be a 1PPS SYNC input for REF+SYNC frequency/phase/time locking

  - Any input can be a clock with embedded 1PPS

  - Input-input phase measurement, 1ps resolution

  - Input-DPLL phase measurement, 1ps resolution

  - Per-input phase adjustment, 1ps resolution

- **Output Clock Frequency Generation**

  - Any output frequency from <0.5Hz to 1045MHz (180MHz max for Synth0)

  - High-resolution fractional frequency conversion with 0ppm error

  - Synthesizers 1 & 2 have integer and fractional dividers to make a total of 5 frequency families

  - Output jitter from Synth 1 & 2 is <0.3ps RMS

  - Output jitter from fractional dividers is typically < 1ps RMS, many frequencies <0.5ps RMS

  - Each HPOUTP/N pair can be LVDS, LVPECL, HCSL, 2xCMOS, HSTL or programmable diff.

  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)

  - Four output banks each with VDDO pin; CMOS output voltages from 1.5V to 3.3V

  - Per-synthesizer phase adjust, 1ps resolution

- Per-output programmable duty cycle

- Precise output alignment circuitry and per-output phase adjustment

- Per-output enable/disable and glitchless start/stop (stop high or low)

- **Local Oscillator**

  - Operates from a single TCXO or OCXO: 23.75-25MHz, 47.5-50MHz, 114.285-125MHz

  - Very-low-jitter applications can connect a TCXO or OCXO as the stability reference and a low-jitter XO as the jitter reference

- **General Features**

  - Automatic self-configuration at power-up from internal Flash memory

  - Input-to-output alignment <200ps (ext feedback)

  - Fast REF+SYNC locking for frequency and 1PPS phase alignment with lower-cost oscillator

  - Internal compensation (1ppt) for local oscillator frequency error in DPLLs and input monitors

  - Numerically controlled oscillator behavior in each DPLL and each fractional output divider

  - Easy-to-configure design requires no external VCXO or loop filter components

  - 7 GPIO pins with many possible behaviors

  - SPI or I²C processor Interface

  - 1.8V and 3.3V core VDD voltages

  - Power: 1.3W for 2 inputs, 1 synth, 6 LVDS out

  - Easy-to-use evaluation/programming software

Applications

- Central system timing ICs for SyncE, SyncE+1588, SONET/SDH, OTN, wireless base station and other carrier-grade systems

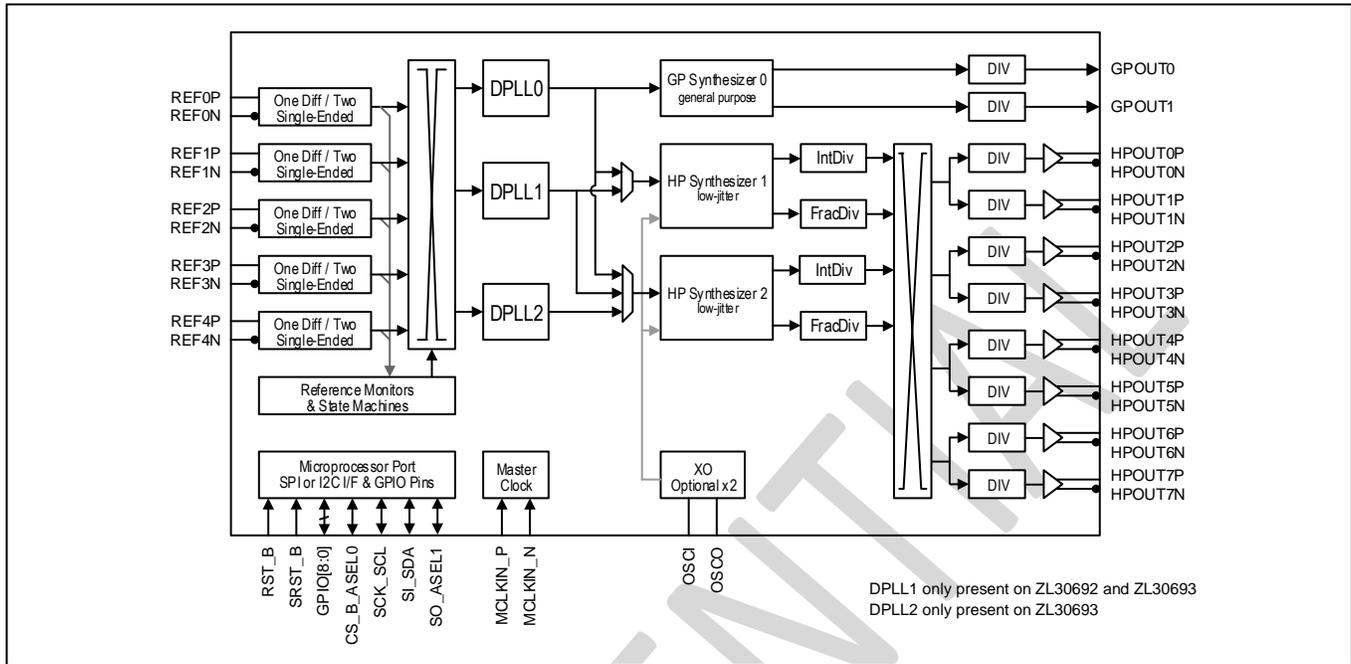- G.8262/813 EEC/SEC, Telcordia Stratum 2-4

1. Block Diagram

Figure 1 - Functional Block Diagram
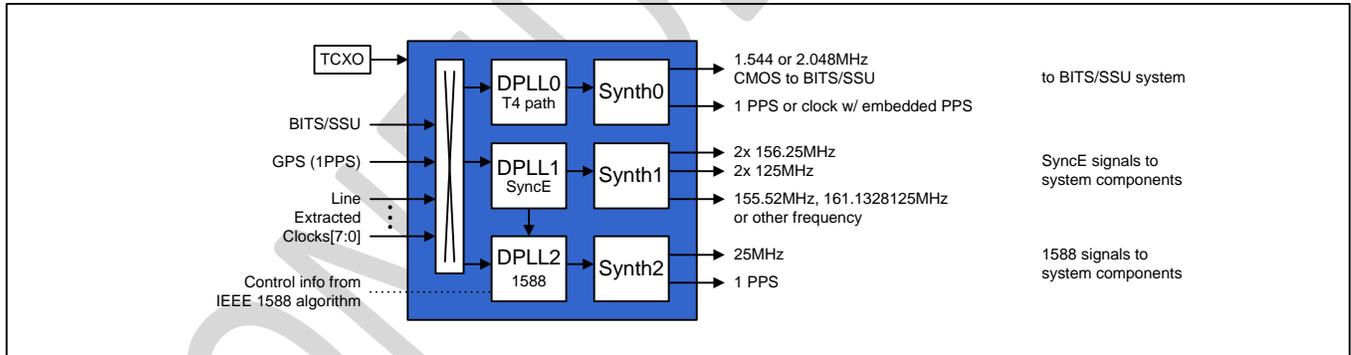
2. Application Example

Figure 2 - Synchronous Ethernet and IEEE 1588 Central Timing Application

3. Detailed Features

3.1 Input Block Features

- Ten input reference pins; each can accept a CMOS signal or the POS side of a differential pair; or two can be paired to accept both sides of a differential pair
- Any input can be a SYNC signal for REF+SYNC frequency/phase/time locking
- Any input can be a clock signal with embedded PPS signal (duty cycle distortion indicates PPS location)
- Input clocks can be any frequency from 0.5Hz up to 900MHz (180MHz max for CMOS inputs)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Inputs constantly monitored by programmable frequency and single-cycle monitors
- Single-cycle monitor can quickly disqualify a reference when measured period is incorrect
- Frequency measurement (ppb or Hz) and monitoring (coarse, fine, and frequency-step monitors)
- Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs
- Input-to-input phase measurement, 1ps resolution
- Input-to-DPLL phase measurement, 1ps resolution
- Per-input phase adjustment, 1ps resolution

3.2 DPLL Features

- One, two or three full-featured DPLLs
- Very high-resolution DPLL architecture
- State machine automatically transitions among freerun, tracking and holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1mHz to 470Hz
- Less than 0.1dB gain peaking
- Fast frequency/phase/time lock capability for 1PPS or clock+1PPS input references
- Programmable phase-slope limiting (PSL)
- Programmable frequency rate-of-change limiting (FCL)
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching
- Per-DPLL phase adjustment, 1ps resolution
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- High-resolution holdover frequency averaging
- Time-of-Day registers: 48-bit seconds, 32-bit nanoseconds, writeable on input PPS edge

3.3 Synthesizer Features

- Any-to-any frequency conversion with 0ppm error
- Two low-jitter synthesizers (Synth1, Synth2) with very high-resolution fractional scaling (i.e. non-integer multiplication)
- Two output dividers per low-jitter synthesizer: one integer (4 to 15 plus half divides 4.5 to 7.5) and one 40-bit fractional
- One general-purpose synthesizer (Synth0)
- A total of five output frequency families
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

3.4 Low-Jitter Output Clock Features

- Up to 16 single-ended outputs (up to 8 differential outputs) from Synth1 and Synth2
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 0.5Hz to 1045MHz (250MHz max for CMOS and HSTL)
- Output jitter from Synth1 and Synth2 integer dividers is <0.3ps RMS
- Output jitter from fractional dividers is <1ps RMS, many frequencies <0.5ps RMS
- In CMOS mode, the HPOUTxN frequency can be an integer divisor of the HPOUTxP frequency (Example 1: HPOUT3P 125MHz, HPOUT3N 25MHz. Example 2: HPOUT2P 25MHz, HPOUT2N 1Hz)

- Outputs directly interface (DC coupled) with LVDS, LVPECL, HSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks
- Sophisticated output-to-output phase alignment
- Per-synthesizer phase adjustment, 1ps resolution
- Per-output phase adjustment
- Per-output duty cycle / pulse width configuration
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

3.5 General-Purpose Output Clock Features
- Two CMOS outputs from Synth0
- Any frequency from 0.5Hz to 180MHz
- Output jitter is typically 20-30ps
- Useful for applications where the component or system receiving the signal has low bandwidth such as a central timing IC
- Can output a clock signal with embedded PPS (ePPS) (duty cycle distortion indicates PPS location)

3.6 Local Oscillator
- Operates from a single TCXO or OCXO (jitter reference for the device). Acceptable frequencies: 23.75MHz to 25MHz, 47.5MHz to 50MHz, 114.285MHz to 125MHz. Best jitter: $\geq$48MHz.
- Very-low-jitter applications can connect a TCXO or OCXO (any frequency, any output jitter) as the stability reference and a low-cost low-jitter XO as the jitter reference
- This ability to have separate jitter and stability references greatly reduces the cost of the TCXO or OCXO (no jitter requirement, no high-frequency-requirement) and allows reuse of already-qualified TCXO and OCXO components

3.7 General Features
- Automatic self-configuration at power-up from internal Flash memory
- Input-to-output alignment <200ps with external feedback
- Fast REF+SYNC locking for frequency and 1PPS phase alignment with lower-cost oscillator
- Generates output SYNC signals: 1PPS (IEEE 1588), 2kHz or 8kHz (SONET/SDH) or other frequency
- JESD204B clocking: device clock and SYSREF signal generation with skew adjustment
- Internal compensation for local oscillator frequency error in DPLLs and input monitors, 1ppt resolution
- Numerically controlled oscillator (NCO) behavior allows system software to steer DPLL frequency or fractional output divider frequency with resolution better than 0.005ppt
- Spread-spectrum modulation available in each fractional output divider (PCIe compliant)
- Seven general-purpose I/O pins each with many possible status and control options
- SPI or I²C serial microprocessor interface

3.8 Evaluation Software
- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the device quick and easy
- Generates configuration scripts to be stored in internal Flash memory
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without an evaluation board

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