NHD-3.12-25664UMY3

OLED Display Module

NHD-	Newhaven Display
3.12-	3.12” Diagonal Size
25664-	256 x 64 Pixel Resolution
UM-	Model – Includes Multi-Font Chip
Y-	Emitting Color: Yellow
3-	+3V Power Supply

Functions and Features

- **256 x 64 pixel resolution**
- **Built-in SSD1322 controller**
- **Parallel or serial MPU interface**
- **Single, low voltage power supply**
- **RoHS compliant**
- **Multi-Language Fonts built-in**

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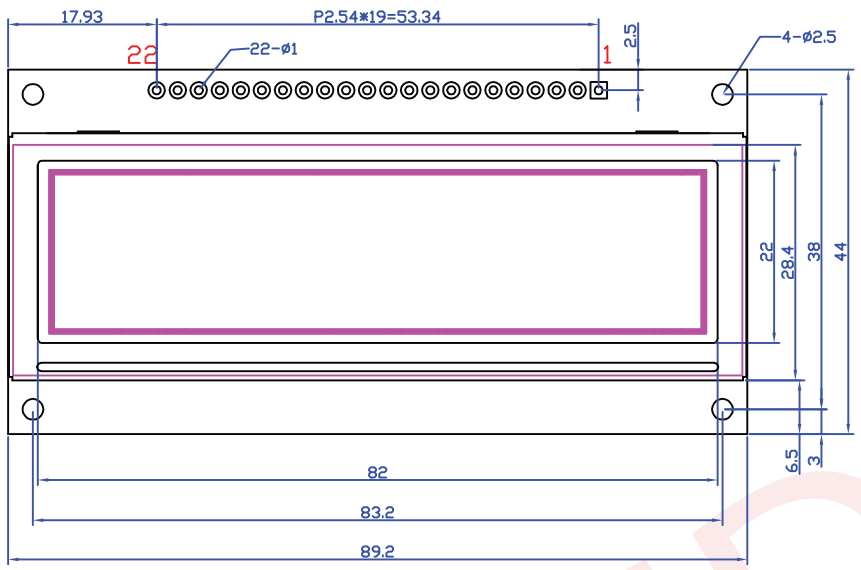
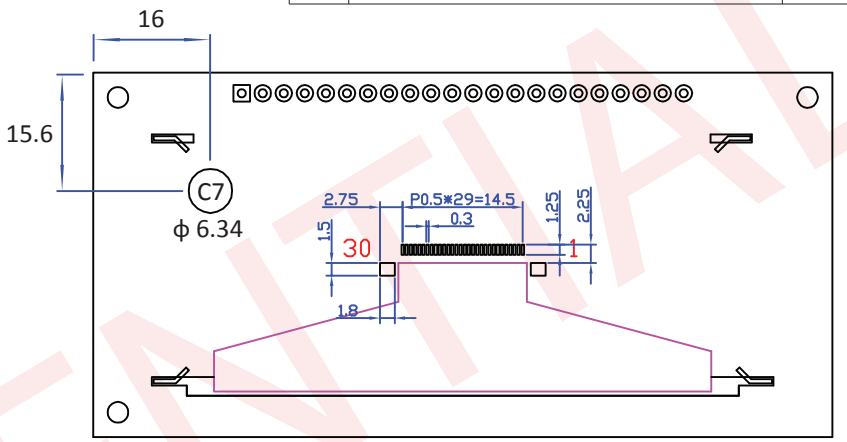
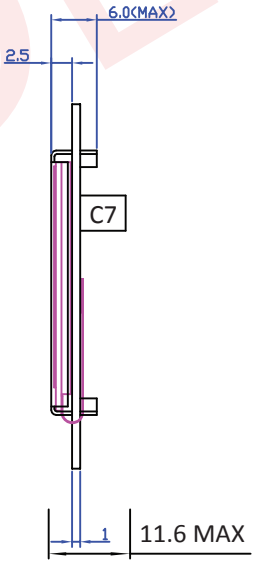
1. Document Revision History

Revision	Date	Description	Changed by
0	10/15/2012	Preliminary Release	-
1	11/5/2012	Initial Product Release	-
2	9/12/2014	Electrical Characteristics updated	ML

2. Mechanical Drawing







PIN ASSIGNMENT

1	VSS
2	VDD
3	NC
4	D/C
5	R/W (/WR)
6	E (/RD)
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	/RES
16	/CS
17	BS1
18	BS0
19	MF_SCLK
20	MF_SI
21	/MF_CS2
22	MF_SO

Notes:

1. Color: Yellow
2. Controller IC: SSD1322
3. Interface: 8-bit 68xx/80xx Parallel, 4-wire SPI
4. RoHS Compliant

Rev	Description	Date

	Date	
	11/21/12	NEWHAVEN DISPLAY INTERNATIONAL
Gen. Tolerance	Unit	Model:
±0.3mm	mm	NHD-3.12-25664UMY3

3. Interface Description

3.1. Parallel Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5	R/W or /WR	MPU	**6800-interface:** Read/Write select signal, R/W=1: Read R/W: =0: Write **8080-interface:** Active LOW Write signal.
6	E or /RD	MPU	**6800-interface:** Operation enable signal. Falling edge triggered. **8080-interface:** Active LOW Read signal.
7-14	DB0 – DB7	MPU	8-bit Bi-directional data bus lines.
15	/RES	MPU	Active LOW Reset signal.
16	/CS	MPU	Active LOW Chip Enable signal.
17	BS1	MPU	MPU Interface Select signal.
18	BS0	MPU	MPU Interface Select signal.
19	MF_SCLK	MPU	Multi-font IC Serial Clock Input
20	MF_SI	MPU	Multi-font IC Serial Data Input
21	/MF_CS2	MPU	Multi-font IC Active LOW Chip Enable signal.
22	MF_SO	MPU	Multi-font IC Serial Data Output

3.2. Serial Interface:

Pin No.	Symbol	External Connection	Function Description
1	VSS	Power Supply	Ground
2	VDD	Power Supply	Supply Voltage for OLED and logic.
3	NC	-	No Connect
4	D/C	MPU	Register select signal. D/C=0: Command, D/C=1: Data
5-6	VSS	Power Supply	Ground
7	SCLK	MPU	Serial Clock signal.
8	SDIN	MPU	Serial Data Input signal.
9	NC	-	No Connect
10-14	VSS	Power Supply	Ground
15	/RES	MPU	Active LOW Reset signal.
16	/CS	MPU	Active LOW Chip Enable signal.
17	BS1	MPU	MPU Interface Select signal.
18	BS0	MPU	MPU Interface Select signal.
19	MF_SCLK	MPU	Multi-font IC Serial Clock Input
20	MF_SI	MPU	Multi-font IC Serial Data Input
21	/MF_CS2	MPU	Multi-font IC Active LOW Chip Enable signal.
22	MF_SO	MPU	Multi-font IC Serial Data Output

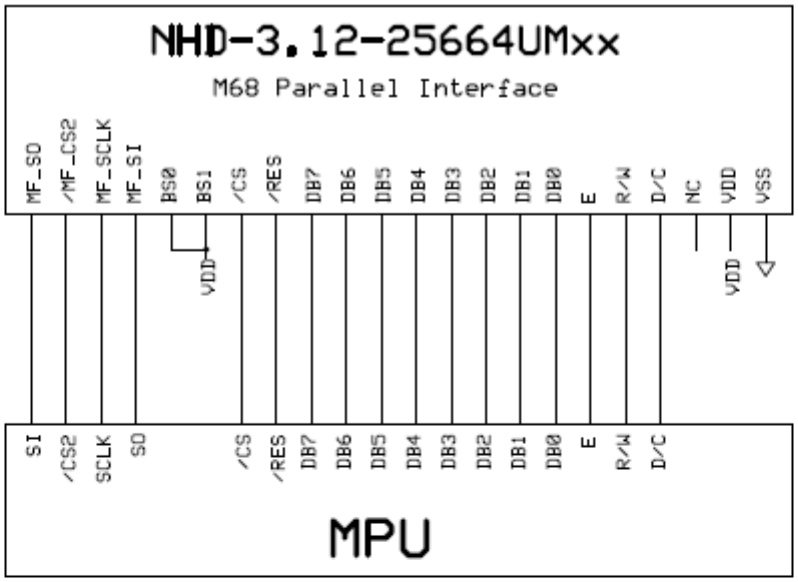
3.3. MPU Interface Pin Selections

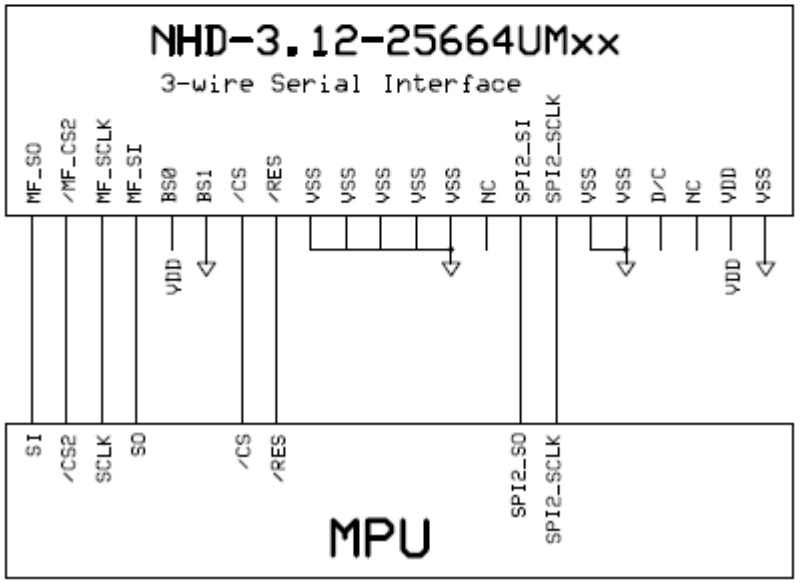
Pin Name	6800 Parallel 8-bit interface	8080 Parallel 8-bit interface	3-wire Serial Interface	4-wire Serial Interface
BS1	1	1	0	0
BS0	1	0	1	0

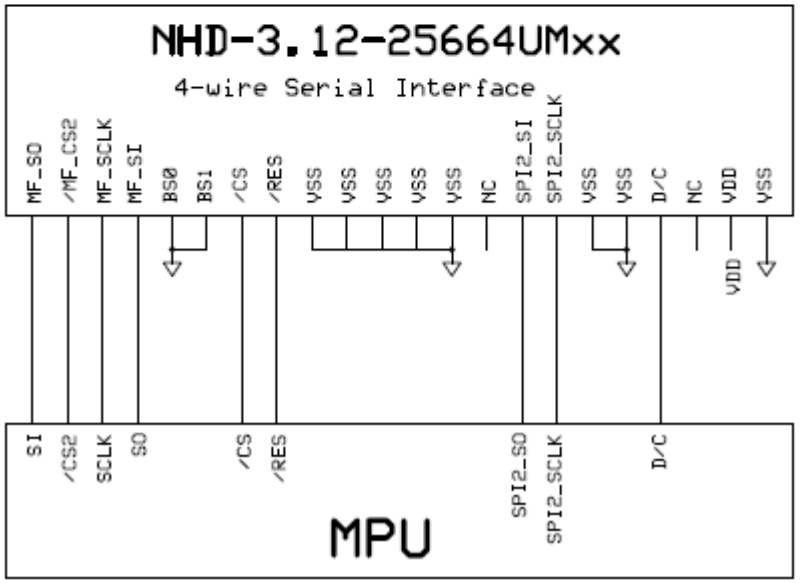
3.4. MPU Interface Pin Assignment Summary

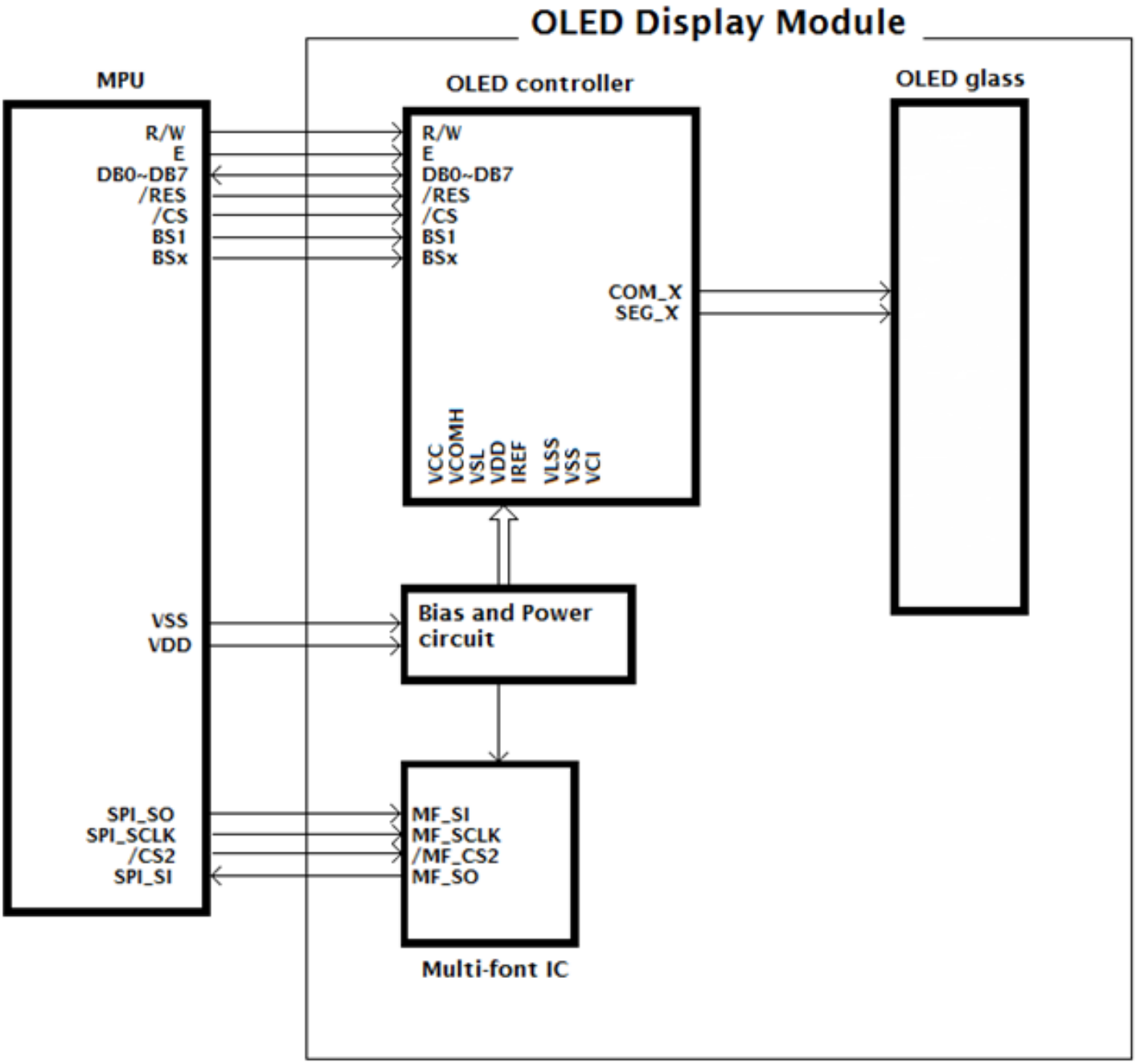
Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W	/CS	D/C	/RES
8-bit 6800	D[7:0]								E	R/W	/CS	D/C	/RES
8-bit 8080	D[7:0]								/RD	/WR	/CS	D/C	/RES
3-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	Tie LOW	/RES
4-wire SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		/CS	D/C	/RES

4. Wiring Diagrams








OLED Display Module
MPU
OLED controller
OLED glass
R/W
E
DB0~DB7
/RES
/CS
BS1
BSx
R/W
E
DB0~DB7
/RES
/CS
BS1
BSx
COM_X
SEG_X
VCC
VCOMH
VSL
VDD
IREF
VLSS
VSS
VCI
VSS
VDD
Bias and Power circuit
SPI_SO
SPI_SCLK
/CS2
SPI_SI
MF_SI
MF_SCLK
/MF_CS2
MF_SO
Multi-font IC

5. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	Top	Absolute Max	-20	-	+70	°C
Storage Temperature Range	Tst	Absolute Max	-40	-	+90	°C
Supply Voltage	VDD		-	3.0	3.3	V
Supply Current	IDD	VDD=3.0V, 50% ON	-	165	180	mA
		VDD=3.0V, 100% ON	-	260	280	mA
Sleep Mode Current	IDD_{SLEEP}		-	3	12	µA
"H" Level input	Vih		0.8*VDD	-	VDD	V
"L" Level input	Vil		VSS	-	0.2*VDD	V
"H" Level output	Voh		0.9*VDD	-	VDD	V
"L" Level output	Vol		VSS	-	0.1*VDD	V

6. Optical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing Angle – Vertical (top)	AV		80	-	-	º
Viewing Angle – Vertical (bottom)	AV		80	-	-	º
Viewing Angle – Horizontal (left)	AH		80	-	-	º
Viewing Angle – Horizontal (right)	AH		80	-	-	º
Contrast Ratio	Cr		2000:1	-	-	-
Response Time (rise)	Tr	-	-	10	-	us
Response Time (fall)	Tf	-	-	10	-	us
Brightness		50% checkerboard	60	80	-	cd/m^2
Lifetime		Ta=25°C, 50% checkerboard	40,000	-	-	Hrs

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

7. Font Content Address Table

#	Type	Font Content	Character Set	Number of Characters	Base Address (decimal)	Base Address (hex)
1	ASCII	5x7 ASCII	ASCII	96	0	000000
2		7x8 ASCII	ASCII	96	768	000300
3		8x16 **BOLD** ASCII	ASCII	96	1,536	000600
4		Width-adjusted Arial ASCII	ASCII	96	3,072	000C00
5		8x16 Latin	Basic	96	6,336	0018C0
6		8x16 Latin	Supplement	96	7,872	001EC0
7		8x16 Latin	Extended A	128	9,408	0024C0
8		8x16 Latin	Extended B	80	11,456	002CC0
9		8x16 Latin	Extended Additional	96	12,736	0031C0
10		8x16 Greek	Basic	96	14,272	0037C0
11	UNICODE	8x16 Cyrillic	Basic	208	15,808	003DC0
12		8x16 Hebrew	Basic	112	19,136	004AC0
13		8x16 Thai	Basic	128	20,928	0051C0
14		Width-adjusted Latin	Basic	96	22,976	0059C0
15		Width-adjusted Latin	Supplement	96	26,240	006680
16		Width-adjusted Latin	Extended A	128	29,504	007340
17		Width-adjusted Latin	Extended B	80	33,856	008440
18		Width-adjusted Latin	Extended Additional	96	36,576	008EE0
19		Width-adjusted Greek	Basic	96	39,840	009BA0
20		Width-adjusted Cyrillic	Basic	208	43,104	00A860
21		Width-adjusted Arabic	Basic	576	50,176	00C400
22	CJK	GB2312		7,614	69,760	011080
23		KSC5605		6,500	379,744	05CB60
24		JIS0208		7,999	490,624	077C80
25	LCM	5x7 ISO8859		1,792	946,992	0E7330
26		LCM 5x10		1,792	961,328	0EAB30

8. Supported Languages

Language Family	Area	Country	Language
Latin (English)	Europe	United Kingdom	English
		Ireland	
	North America	USA	English
		Canada	English, French
		Belize	English
		Jamaica	
		Trinidad and Tobago	
		Bahamas	
		Antigua and Barbuda	
		Dominica	
		St. Vincent	
		St. Lucia	
		Grenada	
		St. Kitts-Nevis	
	South Africa	Guyana	English
	Australia	Australia	English
		New Zealand	
		Tonga	
		Fiji	
		Palau	
		Solomon	
		Vanuatu	
		Kiribati	
		Nauru	
		Marshall Islands	
	Africa	South Africa	English, Dutch
		Zimbabwe	English
		Gambia	
		Sierra Leone	
		Liberia	
		Ghana	
		Nigeria	
		Uganda	
		Zambia	
		Malawi	
		Seychelles	
		Mauritius	
		Botswana	
		Namibia	
		Lesotho	
Latin (Portuguese)	Europe	Portugal	Portuguese
	South America	Brazil	
	Africa	Cape Verde	
		Guinea-Bissau	
		Sao Tome and Principe	
		Angola	
		Mozambique	
Latin (German)	Europe	Germany	German
		Switzerland	German, French
		Austria	German
		Luxembourg	German,

Language Family	Area	Country	Language
Latin (French)	Europe	France	French
		Belgium	French, Dutch
		Monaco	French, Italian
	North America	Haiti	French
	Africa	Senegal	French
		Mali	
		Burkina Faso	
		Guinea	
		Cote d'Ivoire	
		Togo	
		Benin	
		Niger	
		Cameroon	
		Chad	
		Central African Republic	
		Djibouti	
		Burundi	
		Republic of Democratic Congo	
		Congo	
		Gabon	
		Comoros	
		Madagascar	
Latin (Spanish)	Europe	Spain	Spanish, Catalan
		Andorra	Spanish
	North America	Mexico	Spanish
		Guatemala	
		Costa Rica	
		Panama	
		Dominican Republic	
		El Salvador	
		Honduras	
		Nicaragua	
		Puerto Rico	
		Cuba	
	South America	Venezuela	Spanish
		Colombia	
		Peru	
		Argentina	
		Ecuador	
		Chile	
		Uruguay	
		Paraguay	
		Bolivia	
	Africa	New Guinea	Spanish
		Ceuta and Melilla	
Latin (Nordic Europe)	Europe	Denmark	Danish
		Norway	Norwegian
		Sweden	Swedish
		Faroes	Faroese
		Greenland	Greenlandic
		Iceland	Icelandic

			French
		Liechtenstein	German
Latin (Dutch)	Europe	Holland	Dutch
	South America	Surinam	
Latin (Central Europe)	Europe	Czech	Czech
		Slovakia	Slovak
		Poland	Polish
		Hungary	Hungarian
		Romania	Romanian
		Slovenia	Slovenian
		Croatia	Crotian
Latin (Southern Europe)	Europe	Italy	Italian
		San Marino	
		Vatican	
		Turkey	Turkish
		Malta	Maltese
		Albania	Albanian
Latin (Southeast Asia)	Asia	Vietnam	Vietnamese
		Malaysia	Malaysian
		Brunei	
		Indonesia	Indonesian
		East Timor	
		Philippines	English, Tagalog
Arabic (Africa)	Africa	Egypt	Arabic
		Tunisia	
		Libya	
		Morocco	
		Algeria	
		Sudan	
		Somalia	
		Djibouti	
		Mauritania	
Arabic (Asia)	Asia	Syria	Arabic
		United Arab Emirates	
		Lebanon	
		Yemen	
		Kuwait	
		Qatar	
		Bahrain	
		Oman	
		Jordan	
		Iraq	
		Saudi Arabia	
		Palestine	
		Iran	Farsi
		Pakistan	Urdu, Arabic
		Afghanistan	Pashto
		Finland	Finnish, Swedish
		Estonia	Estonian
		Latvia	Latvian
		Lithuania	Lithuanian
Cyrillic (Eastern Europe)	Europe	Russia	Russian
		Belarus	
		Ukraine	Russian Ukrainian
		Bulgaria	Bulgarian
		Moldova	Russian
		Yugoslavia	Serbian
		Barbados	
		Macedonia	Macedonian
Cyrillic (Asia)	Asia	Azerbaijan	Azeri
		Kirghizstan	Kyrgyz
		Tajikistan	Tajik
		Turkmenistan	Turkmen
		Uzbekistan	Uzbek
		Kazakhstan	Kazakh
		Mongolia	Mongolian
Greek	Europe	Greece	Greek
		Cyprus	
Latin (Africa)	Africa	Kenya	Kiswahili
		Tanzania	
Hebrew	Asia	Israel	Hebrew
Thai	Asia	Thailand	Thai
Japan	Asia	Japan	Japanese
Korea	Asia	Korea	Korean
China	Asia	China	Chinese
		Singapore	

9. OLED controller Instruction Table (Built-In SSD1322 Controller/Driver)

Instruction	Code										Description	RESET value
	D/C	HEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Enable Grayscale Table	0	**00**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Enable the Grayscale table settings. (see command 0xB8)	
Set Column Address	0	**15**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	Set column start and end address	
	1	**A[6:0]**	*	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	A[6:0]: Column start address. Range: 0-119d	0
	1	**B[6:0]**	*	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	B[6:0]: Column end address. Range: 0-119d	119d
Write RAM Command	0	**5C**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	Enable MCU to write Data into RAM	
Read RAM Command	0	**5D**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	Enable MCU to read Data from RAM	
Set Row Address	0	**75**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**1**	Set row start and end address	
	1	**A[6:0]**	*	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	A[6:0]: Row start address. Range: 0-127d	0
	1	**B[6:0]**	*	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	B[6:0]: Row end address. Range: 0-127d	127d
Set Remap	0	**A0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	A[0] = 0; Horizontal Address Increment	0
	1	**A[5:0]**	**0**	**0**	**A5**	**A4**	**0**	**A2**	**A1**	**A0**	A[0] = 1; Vertical Address Increment	
	1	**B[4]**	*	*	**0**	**B4**	**0**	**0**	**0**	**1**	A[1] = 0; Disable Column Address remap	0
											A[1] = 1; Enable Column Address remap	
											A[2] = 0; Disable Nibble remap	0
											A[2] = 1; Enable Nibble remap	
											A[4] = 0; Scan from COM0 to COM[N-1]	0
											A[4] = 1; Scan from COM[N-1] to COM0	
											A[5] = 0; Disable COM split Odd/Even	0
											A[5] = 1; Enable COM split Odd/Even	
											B[4] = 0; Disable Dual COM mode	0
											B[4] = 1; Enable Dual COM mode	
											Note: A[5] must be 0 if B[4] is 1.	
Set Display Start Line	0	**A1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	Set display RAM display start line register from 0-127.	0
	1	**A[6:0]**	*	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
Set Display Offset	0	**A2**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	Set vertical shift by COM from 0~127.	0
	1	**A[6:0]**	*	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
Display Mode	0	**A4/A7**	**1**	**0**	**1**	**0**	**0**	**X2**	**X1**	**X0**	0xA4 = Entire display OFF	0xA6
											0xA5 = Entire display ON, all pixels Grayscale level 15	
											0xA6 = Normal display	
											0xA7 = Inverse display	
Enable Partial Display	0	**A8**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	Turns ON partial mode.	
	1	**A[6:0]**	**0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	A[6:0] = Address of start row	
	1	**B[6:0]**	**0**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**	B[6:0] = Address of end row (B[6:0] > A[6:0])	
Exit Partial Display	0	**A9**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	Exit Partial Display mode	
Function Selection	0	**AB**	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	A[0] = 0; External VDD	

	1	**A[0]**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**A0**	A[0] = 1; Internal VDD regulator	1
Set Sleep Mode ON/OFF	0	**AE~AF**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**X0**	0xAE = Sleep Mode ON (display OFF) 0xAF = Sleep Mode OFF (display ON)	
Set Phase Length	0 1	**B1** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	A[3:0] = P1. Phase 1 period of 5-31 DCLK clocks A[7:4] = P2. Phase 2 period of 3-15 DCLK clocks	9 7
Set Display Clock Divide Ratio / Oscillator Frequency	0 1	**B3** **A[7:0]**	**1** **A7**	**0** **A6**	**1** **A5**	**1** **A4**	**0** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0000; divide by 1 A[3:0] = 0001; divide by 2 A[3:0] = 0010; divide by 4 A[3:0] = 0011; divide by 8 A[3:0] = 0100; divide by 16 A[3:0] = 0101; divide by 32 A[3:0] = 0110; divide by 64 A[3:0] = 0111; divide by 128 A[3:0] = 1000; divide by 256 A[3:0] = 1001; divide by 512 A[3:0] = 1010; divide by 1024 A[3:0] >= 1011; invalid A[7:4] = Set the Oscillator Frequency. Frequency increases with the value of A[7:4]. Range 0000b~1111b.	0 1100b
Set GPIO	0 1	**B5** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**0** **A1**	**1** **A0**	A[1:0] = 00; GPIO0 input disabled A[1:0] = 01; GPIO0 input enabled A[1:0] = 10; GPIO0 output LOW A[1:0] = 11; GPIO0 output HIGH A[3:2] = 00; GPIO1 input disabled A[3:2] = 01; GPIO1 input enabled A[3:2] = 10; GPIO1 output LOW A[3:2] = 11; GPIO1 output HIGH	 10b 10b
Set Second Precharge Period	0 1	**B6** **A[3:0]**	**1** *	**0** *	**1** *	**1** *	**0** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the second precharge period A[3:0] = DCLKs	1000b
Set Grayscale Table	0 1 1 1 1 1 1 1	**B8** **A1[7:0]** **A2[7:0]** **.** **.** **.** **A14[7:0]** **A15[7:0]**	**1** $A1_7$ $A2_7$ . . . $A14_7$ $A15_7$	**0** $A1_6$ $A2_6$ . . . $A14_6$ $A15_6$	**1** $A1_5$ $A2_5$ . . . $A14_5$ $A15_5$	**1** $A1_4$ $A2_4$ . . . $A14_4$ $A15_4$	**1** $A1_3$ $A2_3$ . . . $A14_3$ $A15_3$	**0** $A1_2$ $A2_2$ . . . $A14_2$ $A15_2$	**0** $A1_1$ $A2_1$ . . . $A14_1$ $A15_1$	**0** $A1_0$ $A2_0$ . . . $A14_0$ $A15_0$	Sets the gray scale pulse width in units of DCLK. Range 0-180d. A1[7:0] = Gamma Setting for GS1 A2[7:0] = Gamma Setting for GS2 . . . A14[7:0] = Gamma Setting for GS14 A15[7:0] = Gamma Setting for GS15 Note: 0 < GS1 < GS2 < GS3 … < GS14 < GS15 The setting must be followed by command 0x00.	
Select Default Linear Gray Scale Table	0	**B9**	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	Sets Linear Grayscale table GS0 pulse width = 0 GS0 pulse width = 0	

											GS0 pulse width = 8 GS0 pulse width = 16 . . . GS0 pulse width = 104 GS0 pulse width = 112	
Set Precharge Voltage	0 1	**BB** **A[4:0]**	**1** *****	**0** *****	**1** *****	**1** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**1** **A0**	Set precharge voltage level. A[4:0] = 0x00; 0.20*VCC . . A[4:0] = 0x3E; 0.60*VCC	0x17
Set VCOMH Voltage	0 1	**BE** **A[3:0]**	**1** *****	**0** *****	**1** *****	**1** *****	**1** **A3**	**1** **A2**	**1** **A1**	**0** **A0**	Sets the VCOMH voltage level A[3:0] = 0x00; 0.72*VCC . . A[3:0] = 0x04; 0.8*VCC . . A[3:0] = 0x07; 0.86*VCC	0x04
Set Contrast Control	0 1	**C1** **A[7:0]**	**1** **A7**	**1** **A6**	**0** **A5**	**0** **A4**	**0** **A3**	**0** **A2**	**0** **A1**	**1** **A0**	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases.	0x7F
Master Contrast Control	0 1	**C7** **A[3:0]**	**1** *****	**1** *****	**0** *****	**0** *****	**0** **A3**	**1** **A2**	**1** **A1**	**1** **A0**	A[3:0] = 0x00; Reduce output for all colors to 1/16 A[3:0] = 0x01; Reduce output for all colors to 2/16 . . A[3:0] = 0x0E; Reduce output for all colors to 15/16 A[3:0] = 0x0F; no change	0x0f
Set Multiplex Ratio	0 1	**CA** **A[6:0]**	**1** *****	**1** **A6**	**0** **A5**	**0** **A4**	**1** **A3**	**0** **A2**	**1** **A1**	**0** **A0**	Set MUX ratio to N+1 MUX N=A[6:0]; from 16MUX to 128MUX (0 to 14 are invalid)	127d
Set Command Lock	0 1	**FD** **A[2]**	**1** **0**	**1** **0**	**1** **0**	**1** **1**	**1** **0**	**1** **A2**	**0** **1**	**1** **0**	A[2] = 0; Unlock OLED to enable commands A[2] = 1; Lock OLED from entering commands	0x12

For detailed instruction information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

10. OLED Controller -> MPU Interface

For detailed timing information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

10.1. 6800-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, R/W, D/C, E, and /CS.
A LOW on R/W indicates write operation, and HIGH on R/W indicates read operation.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
The E input serves as data latch signal, while /CS is LOW. Data is latched at the falling edge of E signal.

Function	E	R/W	/CS	D/C
Write Command	↓	0	0	0
Read Status	↓	1	0	0
Write Data	↓	0	0	1
Read Data	↓	1	0	1

10.2. 8080-MPU Parallel Interface

The parallel interface consists of 8 bi-directional data pins, /RD, /WR, D/C, and /CS.
A LOW on D/C indicates "Command" read or write, and HIGH on D/C indicates "Data" read or write.
A rising edge of /RS input serves as a data read latch signal while /CS is LOW.
A rising edge of /WR input serves as a data/command write latch signal while /CS is LOW.

Function	/RD	/WR	/CS	D/C
Write Command	1	↑	0	0
Read Status	↑	1	0	0
Write Data	1	↑	0	1
Read Data	↑	1	0	1

Alternatively, /RD and /WR can be kept stable while /CS serves as the data/command latch signal.

Function	/RD	/WR	/CS	D/C
Write Command	1	0	↑	0
Read Status	0	1	↑	0
Write Data	1	0	↑	1
Read Data	0	1	↑	1

10.3. Serial Interface (4-wire)

The 4-wire serial interface consists of serial clock SCLK, serial data SDIN, D/C, and /CS.
D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, and R/W should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	0	↑
Write Data	Tie LOW	Tie LOW	0	1	↑

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6,…D0.
D/C is sampled on every eighth clock and the data byte in the shift register is written to the GDRAM or command register in the same clock.
Note: Read is not available in serial mode.

10.4. Serial Interface (3-wire)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN, and /CS.
D0 acts as SCLK and D1 acts as SDIN. D2 should be left open. D3~D7, E, R/W, and D/C should be connected to GND.

Function	/RD	/WR	/CS	D/C	D0
Write Command	Tie LOW	Tie LOW	0	Tie LOW	↑
Write Data	Tie LOW	Tie LOW	0	Tie LOW	↑

SDIN is shifted into an 9-bit shift register on every rising edge of SCLK in the order of D/C, D7, D6,…D0.
D/C (first bit of the sequential data) will determine if the following data byte is written to the Display Data RAM (D/C = 1) or the command register (D/C = 0).
Note: Read is not available in serial mode.

For detailed protocol information, see datasheet: http://www.newhavendisplay.com/app_notes/SSD1322.pdf

11. Example Initialization Sequence:

```
Set_Command_Lock(0x12);                 // Unlock Basic Commands (0x12/0x16)
Set_Display_On_Off(0x00);               // Display Off (0x00/0x01)
Set_Column_Address(0x1C,0x5B);
Set_Row_Address(0x00,0x3F);
Set_Display_Clock(0x91);                // Set Clock as 80 Frames/Sec
Set_Multiplex_Ratio(0x3F);              // 1/64 Duty (0x0F~0x3F)
Set_Display_Offset(0x00);               // Shift Mapping RAM Counter (0x00~0x3F)
Set_Start_Line(0x00);                   // Set Mapping RAM Display Start Line (0x00~0x7F)
Set_Remap_Format(0x14);                 // Set Horizontal Address Increment
                                        //    Column Address 0 Mapped to SEG0
                                        //    Disable Nibble Remap
                                        //    Scan from COM[N-1] to COM0
                                        //    Disable COM Split Odd Even
                                        //    Enable Dual COM Line Mode
Set_GPIO(0x00);                         // Disable GPIO Pins Input
Set_Function_Selection(0x01);           // Enable Internal VDD Regulator
Set_Display_Enhancement_A(0xA0,0xFD);   // Enable External VSL
Set_Contrast_Current(0x9F);             // Set Segment Output Current
Set_Master_Current(0x0F);               // Set Scale Factor of Segment Output Current Control
//Set_Gray_Scale_Table();               // Set Pulse Width for Gray Scale Table
Set_Linear_Gray_Scale_Table();          //set default linear gray scale table
Set_Phase_Length(0xE2);                 // Set Phase 1 as 5 Clocks & Phase 2 as 14 Clocks
Set_Display_Enhancement_B(0x20);        // Enhance Driving Scheme Capability (0x00/0x20)
Set_Precharge_Voltage(0x1F);            // Set Pre-Charge Voltage Level as 0.60*VCC
Set_Precharge_Period(0x08);             // Set Second Pre-Charge Period as 8 Clocks
Set_VCOMH(0x07);                        // Set Common Pins Deselect Voltage Level as 0.86*VCC
Set_Display_Mode(0x02);                 // Normal Display Mode (0x00/0x01/0x02/0x03)
Set_Partial_Display(0x01,0x00,0x00);    // Disable Partial Display
Set_Display_On_Off(0x01);
```

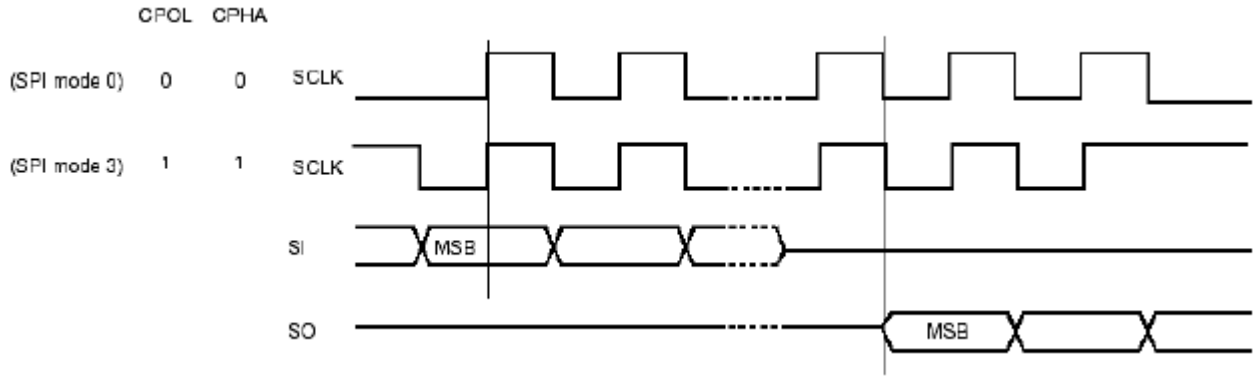
12.Multi-Font IC -> MPU Interface

12.1. Serial Interface

The serial interface consists of serial clock MF_SCLK, serial data in MF_SI, serial data out MF_SO, chip enable /MF_CS2.

Function	MF_SCLK	MF_SI	MF_SO	/MF_CS2
Send Font Address	↑	DATA	X	0
Read Font Data	↓	X	DATA	0

The Multi-Font device is enabled by a high-to-low transition on /MF_CS2. /MF_CS2 must remain LOW for the duration of any command-in or data-out sequence.
The Font Address is shifted in on the MF_SI line on the rising edge of MF_SCLK.
The Font Data is shifted out on the MF_SO line on the falling edge of MF_SCLK.

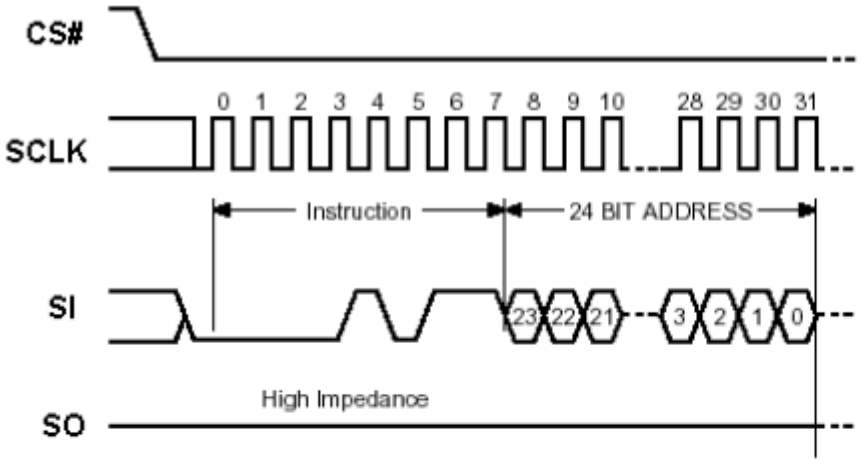


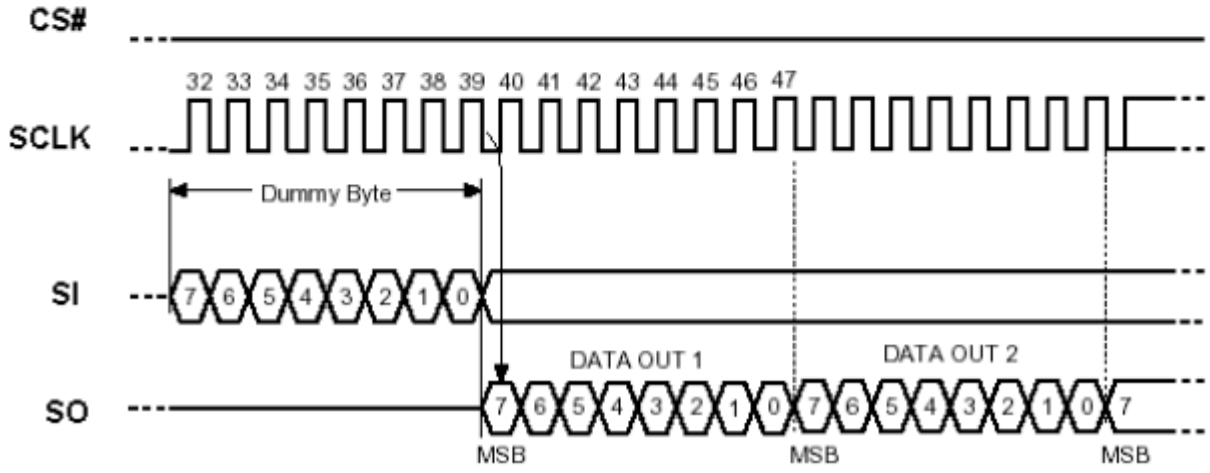
12.2. Communication Protocol

Font data can be accessed and read by using the READ command instruction.

Instruction	Description	Instruction Code	Address Bytes	Dummy Bytes	Data Bytes
READ	Read Data (30MHz MAX)	0Bh	3	1	1 ~ ∞

READ mode supports up to 30MHz frequency on MF_SCLK.
READ mode outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low-to-high transition on /MF_CS2. The internal address pointer will automatically increment after each byte is read.
READ instruction is initiated by executing an 8-bit command [0x0B] on the MF_SI line, followed by the desired font address bits [A23-A0], and followed by an 8-bit dummy write [0x00]. The font data will then be output on MF_SO line, MSB first.
/MF_CS2 must remain active LOW for the duration of the read cycle.





12.3. Timing Characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
Fc	Clock Frequency		-	30	MHz
tCH	Clock High Time		15	-	ns
tCL	Clock Low Time		15	-	ns
tCLCH	Clock Rise Time	peak to peak	0.1	-	V/ns
tCHCL	Clock Fall Time	peak to peak	0.1	-	V/ns
tSLCH	/MF_CS2 Active Setup Time	relative to MF_SCLK	5	-	ns
tCHSL	/MF_CS2 Not Active Hold Time	relative to MF_SCLK	5	-	ns
tDVCH	Data IN Setup Time		2	-	ns
tCHDX	Data IN Hold Time		5	-	ns
tCHSH	/MF_CS2 Active Hold Time	relative to MF_SCLK	5	-	ns
tSHCH	/MF_CS2 Not Active Setup Time	relative to MF_SCLK	5	-	ns
tSHSL	/MF_CS2 Deselect Time		100	-	ns
tSHQZ	Output Disable Time		-	9	ns
tCLQV	Clock Low to Output Valid		-	9	ns
tCLQX	Output Hold Time		0	-	ns

13. Font Tables

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

14. Font Data Arrangement

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

15. Calculation of Font Addresses

See file: www.newhavendisplay.com/app_notes/MultiFont.pdf

16. Multi-Font program code example

17. Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+90°C , 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C , 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+70°C 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-20°C , 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 100 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz , 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value

Precautions for using OLEDs/LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms