

## MOSFET

Metal Oxide Semiconductor Field Effect Transistor

# Bare Die

OptiMOS™3 Power MOS Transistor Chip IPC302N20N3

# **Data Sheet**

Rev. 2.6 Final

# Industrial & Multimarket



## IPC302N20N3

### **Description** 1

- N-channel enhancement mode
- · For additional characteristic and max ratings refer to the datasheet of IPP110N20N3 G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
  Die bond: soldered or glued
  Backside metallization: NiV system

- Frontside metallization: AICu system
- Passivation: nitride (only on edge structure)

#### Table 1 **Key Performance Parameters**

Parameter	Value	Unit
V <sub>(BR)DSS</sub>	200	V
R <sub>DS(on)</sub>	12 <sup>1)</sup>	mΩ
Die size	6.7 x 4.5	mm <sup>2</sup>
Thickness	250	μm









Type / Ordering Code	Package	Marking	Related Links
IPC302N20N3	Chip	not defined	-

### **Electrical Characteristics on Wafer Level** 2

at  $T_i = 25^{\circ}$ C, unless otherwise specified

## Table 2

Parameter	Symbol	Values		11	Note (Test Condition	
		Min.	Тур.	Max.	Unit	Note / Test Condition
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	200	-	-	V	V <sub>GS</sub> =0 V , <i>I</i> <sub>D</sub> =1 mA
Gate threshold voltage	V <sub>GS(th)</sub>	2	3	4	V	<i>V</i> <sub>DS</sub> = <i>V</i> <sub>GS</sub> , <i>I</i> <sub>D</sub> =260 μA
Zero gate voltage drain current	I <sub>DSS</sub>	-	0.1	1	μA	V <sub>GS</sub> =0 V , V <sub>DS</sub> =160 V
Gate-source leakage current	I <sub>GSS</sub>	-	1	100	nA	V <sub>GS</sub> =20 V , V <sub>DS</sub> =0 V
Drain-source on- resistance	R <sub>DS(on)</sub>	-	9.2 <sup>2)</sup>	100 <sup>3)</sup>	mΩ	V <sub>GS</sub> =10 V , <i>I</i> <sub>D</sub> =2.0 A
Reverse diode forward on-voltage	V <sub>SD</sub>	-	1.0	1.2	V	V <sub>GS</sub> =0 V , <i>I</i> <sub>F</sub> =1A
Avalanche energy, single pulse	EAS	-	47 <sup>4)</sup>	-	mJ	I <sub>D</sub> =30 A, R <sub>GS</sub> =25 Ω

 $^{1)}$  packaged in a P-TO220-3 (see ref. product)  $^{2)}$  typical bare die  $R_{\rm DS(on)}; V_{\rm GS}$ =10 V

<sup>&</sup>lt;sup>3)</sup> limited by wafer test-equipment

<sup>&</sup>lt;sup>4)</sup> Wafer tested. For general avalanche capability refer to the datasheet of IPP110N20N3 G



IPC302N20N3

## 3 Package Outlines



Figure 1 Outline Chip, dimensions in µm



### **Revision History**

### IPC302N20N3

### Revision: 2015-04-08, Rev. 2.6

Previous F	Revision	
Revision	Date	Subjects (major changes since last revision)
2.6	-	Release Final Version

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