1.8V 20Gbps USB4/TBT4/DP2.0 DP-Alt Linear ReDriver with AUX-SBU Switch

Features

- 4-to-4 linear ReDriver™ channel configuration with CTLE gain compensation up to 16dB @20Gbps
- Configurable for USB4 Gen 3 (20Gbps single port or dual port), TBT4 (20.625Gbps single port or dual port), USB4 Gen 2 (10Gbps x1 or x2), 1-port USB4 Gen 3/2-lane DP2.0 (UHBR20/UHBR13, UHBR10), 4-lane DP2.0(UHBR20/ UHBR13/UHBR10)
- Default Hi-Z for high speed channels and SBU pins compliant to USB-C® Safe State
- Ultra low latency (< 300ps) for better interoperability and data throughput
- Individual controls on CTLE gain(6 to 16dB @10Ghz), Flat Gain(-4 to +2dB)
- Integrated AUX channel crossbar switch for side band signal
- Type-C connector flip and non-flip plug support
- I2C Slave support with speed up to 1MHz
- Low Power - USB and DisplayPort active U0 (300mW), and USB Deep Slumber mode U1/U2/U3 (3mW), Modern Standby (1.8mW)
- Single Power Supply: 1.8V +/-5%
- Industrial Temperature Support: -40°C to +85°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - Tiny 32-pin WLGA 2.85mm x 4.5mm (0.4 mm pitch)

Applications

- Laptop, Desktop and AIO PCs
- Workstation and Server
- Docking Station
- Display Monitor
- Gaming Console
- Active Cable

Description

The DIODES™ PI2DPX2020 is a 20Gbps non-blocking USB Type-C DP-Alt mode linear ReDriver in a 4-to-4 configuration operated by a 1.8V power supply. It supports multiple operation modes through I2C bus settings for single-port USB4 Gen 3, dual-port USB4 Gen 3x2, 1-port USB4 Gen 3/2-lane DP2.0 (UHBR20) and 4-lane DP2.0 (UHBR20). It swaps the high speed channels under the flip and non-flip plug connection in compliance to Type-C connector with the integrated AUX crossbar switch for SBU pins.

The non-blocking linear ReDriver design ensures that the differential signals conveying pre-shoot and de-emphasis equalization waveforms from the transmitter side to the receiver side help optimize the overall channel link adjustment conducted by the system transmitter and receiver that has been equipped with DFE. The CTLE equalizers are implemented at the inputs of the ReDriver to compensate the channel loss and reduce the ISI jitters. The programmable flat gain adjustments support the eye diagram opening.

The CTLE EQ gains and flat gains are individually programmable on each channel for flexible tuning via the I2C register settings. The on-chip signal detector and DP AUX Listener enable the ReDriver to enter the USB power saving mode or the DP D3 power down mode to further reduce standby power consumption.

Ordering Information

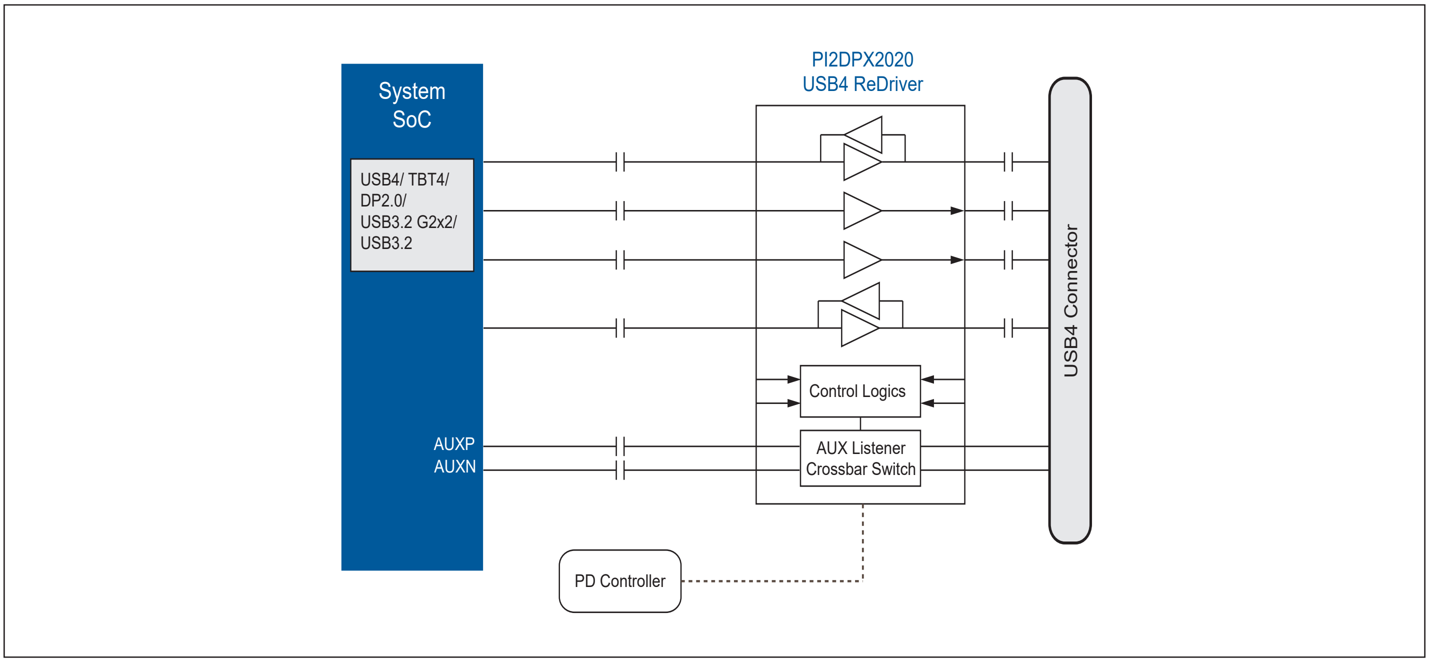
Ordering Number	Package Code	Description
PI2DPX2020FLAEX	FLA	32-Pin, W-LGA4528-32

Notes:

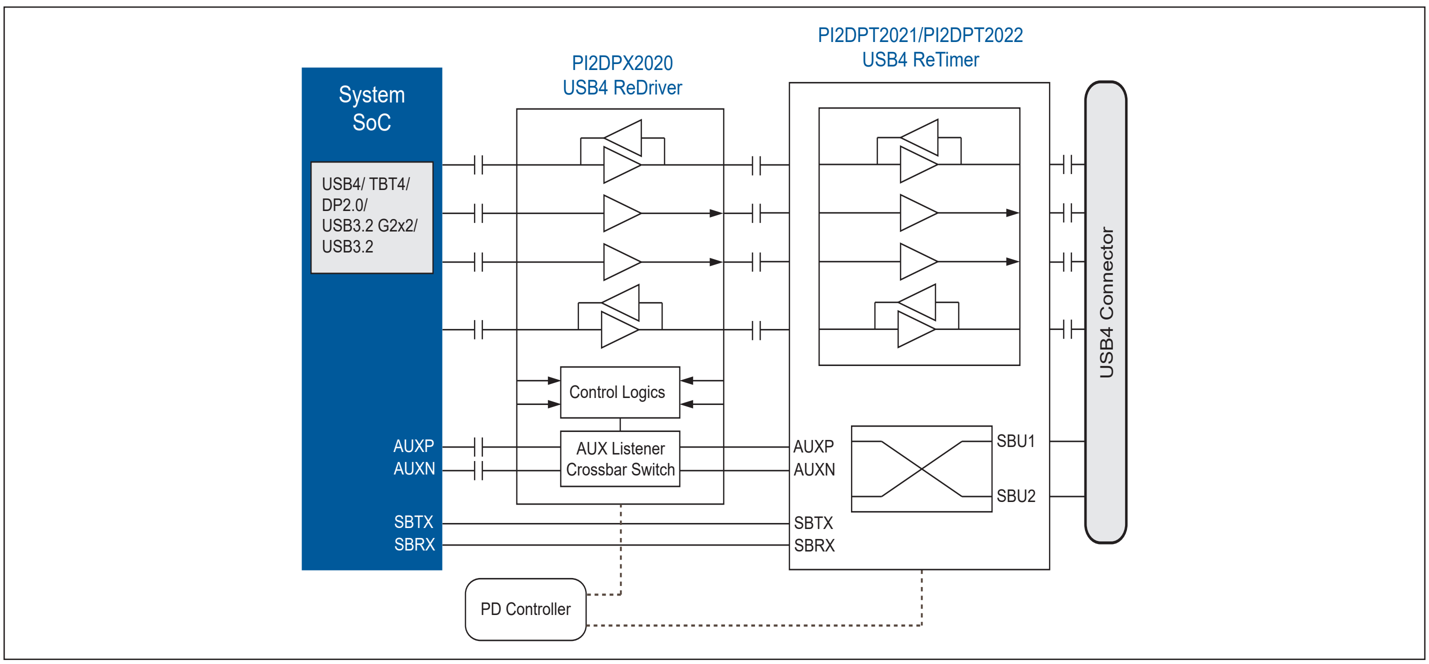
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

Revision History

Date	Revision	Description
December 2020	1	Preliminary Datasheet Release Updated DC/AC specs, Description and Package Drawing
February 2021	2	Updated Package Drawing
October 2021	3	Updated Power Consumption Updated Feature, Description, Power Configuration, Return Loss, and Crosstalk
April 2022	4	Updated Maximum Ratings Datasheet Released Removed Figure 8 Noise Test Configuration
June 2022	5	Updated Part Marking

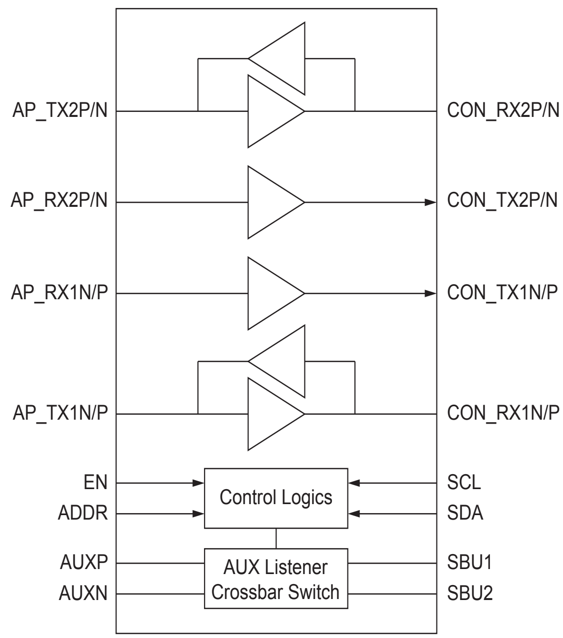


Short Channel System with USB Type-C Connector Application – USB3.2 G2/DP2.0(UHBR20)

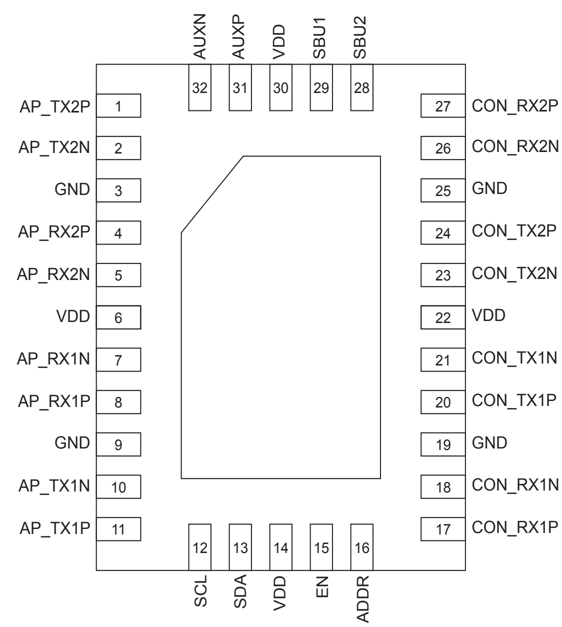


Long Channel System with USB Type-C Connector Application

Block Diagram



Pin Configuration (Top-Side View)



Pin Description

Pin #	Pin Name	Type	Description
Power and GND			
6, 14, 22, 30	VDD18	Power	1.8V power supply, ±5%
3, 9, 19, 25, Center Pad	GND	Ground	Supply ground
Control Pins			
12	SCL	I	SCL is I2C control bus clock. Open-drain structure.
13	SDA	I/O	SDA is I2C control bus data. Open-drain structure.
15	EN	I	Chip Enable. With internal 300kΩ pull-up resistor. "Low": Chip Power Down "High": Normal Operation (Default)
16	ADDR	I	The I2C address select. 4-level input pin. With internal 100KΩ pull-up and 200KΩ pull-down resistors. External Pulldown resistor value is 68KΩ.
High Speed I/O Pins			
18, 17 27, 26	CON_RX1N, CON_RX1P CON_RX2P, CON_RX2N	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to internal VbiasRx, 78kΩ to internal VbiasRx or 78kΩ to GND. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z

Pin Description Cont.

Pin #	Pin Name	Type	Description
21, 20 24, 23	CON_TX1N, CON_TX1P CON_TX2P, CON_TX2N	O	CML output terminals. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z
1, 2 10, 11	AP_TX2P, AP_TX2N, AP_TX1N, AP_TX1P	I/O	Type-C receptacle RX/TX Channel CML input/output terminals. With selectable input termination between 50Ω to VDD, 78kΩ to internal VbiasRx or 78kΩ to GND. With selectable output termination between 50Ω, 6kΩ to internal VbiasTx or Hi-Z
4, 5 7, 8	AP_RX2P, AP_RX2N AP_RX1N, AP_RX1P	I	CML input terminals. With selectable input termination between 50Ω to internal VbiasRx, 78kΩ to internal VbiasRx or 78kΩ to GND.
Side Band Signal Pins			
29, 28	SBU1, SBU2	I/O	Type-C connector SBU signal connections
31, 32	AUXP, AUXN	I/O	DisplayPort AUX CH differential signal connections

Operation Mode

Table 1. Configuration Table

OP_MODE<3:0>	AP_TX2	AP_RX2	AP_RX1	AP_TX1	AUXP	AUXN	Mode
0000	X	X	X	X	X	X	Safe State (Hi-Z)
0001	X	X	X	X	X	X	Safe State (Hi-Z)
0010	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (DP2)	CON_RX1 (DP3)	SBU1	SBU2	4-lane DP + AUX
0011	CON_RX2 (DP3)	CON_TX2 (DP2)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU2	SBU1	4-lane DP + AUX (flipped)
0100	X	X	CON_TX1	CON_RX1	X	X	Single port USB4
0101	CON_RX2	CON_TX2	X	X	X	X	Single port USB4 (flipped)
0110	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (USB4)	CON_RX1 (USB4)	SBU1	SBU2	2-lane DP + USB4 + AUX
0111	CON_RX2 (USB4)	CON_TX2 (USB4)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU2	SBU1	2-lane DP + USB4 + AUX (flipped)
1000	CON_RX2 (USB4)	CON_TX2 (USB4)	CON_TX1 (DP1)	CON_RX1 (DP0)	SBU1	SBU2	USB4 + 2-lane DP + AUX
1001	CON_RX2 (DP0)	CON_TX2 (DP1)	CON_TX1 (USB4)	CON_RX1 (USB4)	SBU2	SBU1	USB4 + 2-lane DP +AUX (flipped)
<1010> ~ <1011>	-	-	-	-	-	-	Reserved
1100	CON_RX2	CON_TX2	CON_TX1	CON_RX1	X	X	Dual-port USB4 or USB3.2 Gen2x2
<1101> ~ <1111>	-	-	-	-	-	-	Reserved

Notes: 1) <0000> default at power on.

I/O Termination Resistance under Different Conditions

Symbol	Parameter	Resistance	Units
RX Terminal			
$R_{in\text{-}pd}$	Input res at EN=0	78k to VbiasRx	Ω
$R_{in\text{-}ch\_pd}$	Input res at channel PD/safe mode (EN=1)	78k to VbiasRx	Ω
$R_{in\text{-}Active}$	Input res at active mode condition	50 to VbiasRx1	Ω
$R_{in\text{-}Slumber}$	Input res in slumber mode 1)	50 to VbiasRx1	Ω
$R_{in\text{-}DeepSlumber}$	Input res in Deep slumber mode 1)	50 to VbiasRx1	Ω
$R_{in\text{-}RxDet}$	Input res in Unplug mode 1)	78k to VbiasRx2	Ω
$R_{in\text{-}DP\text{-}standby}$	Input res in DP standby mode	78k to VbiasRx	Ω
$R_{in\text{-}DP\text{-}active}$	Input res in DP active mode	50 to VbiasRx1	Ω
$R_{in\text{-}DP\text{-}D3}$	Input res in DP D3 mode	78k to VbiasRx	Ω
TX Terminal			
$R_{out\text{-}pd}$	Output res at EN=0	78k to VbiasTx	Ω

Symbol	Parameter	Resistance	Units
$R_{in\text{-}ch\_pd}$	Output res at channel PD/safe mode (EN=1)	78k to VbiasTx	Ω
$R_{out\text{-}Active}$	Output res at active mode condition	50 to VDD	Ω
$R_{out\text{-}Slumber}$	Output res in slumber mode 2)	6k to VbiasTx1	Ω
$R_{out\text{-}DeepSlumber}$	Output res in Deep slumber mode 2)	6k to VbiasTx2	Ω
$R_{out\text{-}RxDet}$	Output res in Unplug mode 2)	6k to VbiasTx2	Ω
$R_{out\text{-}DP\text{-}standby}$	Output res in DP standby mode	78k to VbiasTx	Ω
$R_{out\text{-}DP\text{-}active}$	Output res in DP active mode	50 to VDD	Ω
$R_{out\text{-}DP\text{-}D3}$	Output res in DP D3 mode	78k to VbiasTx	Ω

Notes:
1) The value of Rin will be updated only after the receiver evaluation. Thus, the value can be 50Ω or 78kΩ.
2) The value of Rout will be updated only after the receiver evaluation. Thus, the value can be 50Ω or 6kΩ.

USB Mode

In the low power mode, the signal detector will still be monitoring the input channel. If a channel is in low power mode and the input signal is detected, the corresponding channel will wake-up immediately. If a channel is in low power mode and the signal detector is idle longer than 6ms, the receiver detection loop will be active again. If a load is not detected, then the Channel will move to Device Unplug Mode and monitor the load continuously. If a load is detected, it will return to Low Power Mode, and the receiver detection will be active again in 6ms.

DisplayPort Mode

By default, all channels will go to active mode if HPD bit = 1. The ON/OFF of each DP channel is controlled by the Aux lane count.

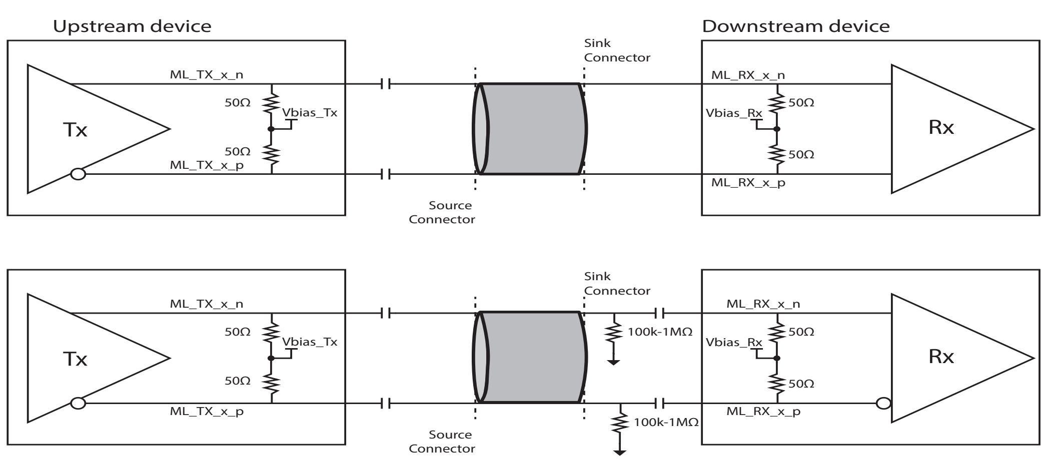


Figure 1. DisplayPort Main Link Connection Diagram

DisplayPort Main Link

The electrical sub-block of a DP Main-Link consists of up to four differential pairs. The DP TX drives doubly terminated, AC-coupled differential pairs in a manner compliant with the Main-Link Transmitter electrical specification.

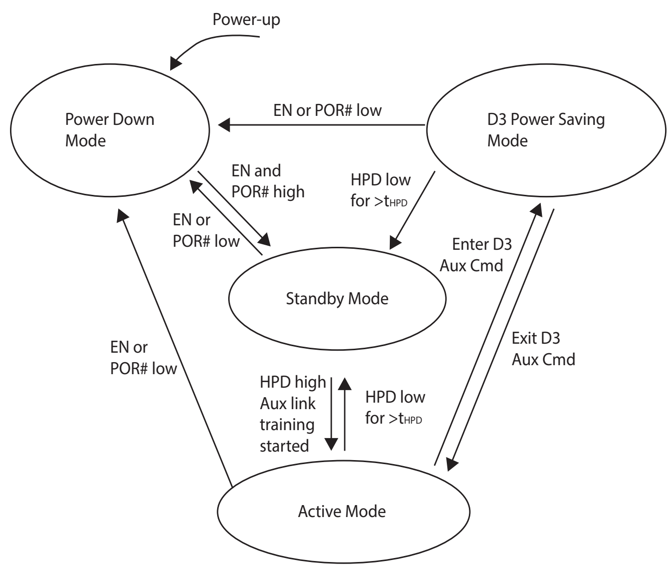


Figure 2. DisplayPort Operation Modes

Table 2. Description of DP Operating Mode

PM_State	Mode	Description
1	Power Down Mode	Lowest power consumption (most circuitries are off); all outputs are high-impedance; All inputs are ignored. AUX listener is turned OFF.
2	Standby Mode	Low power consumption (AUX listener is OFF); Main Link outputs are disabled
3	Active Mode	Data transfer (normal operation); AUX listener is active. The AUX listener is actively monitoring for Link Training unless it is disabled through I2C interface. After power-up and in active mode, all Main Link outputs are enabled.
4	D3 Power Saving Mode	Low power consumption(AUX listener is active); Main Link outputs are disabled

DisplayPort AUX Channel

The AUX CH of DP is a half-duplex, bidirectional channel. The DP device with DPTX such as a Source device is the master of the AUX CH (called AUX CH Requester), while the device with DPRX such as a Sink device is the slave (AUX CH Replier). As the master, the Source device must initiate a Request Transaction, to which the Sink device responds with a Reply Transaction. The system design of a DFP_D on a USB Type-C connector connected to a UFP_D on a USB Type-C connector using a USB Type-C to USB Type-C Cable. The 2MΩ pull-down resistors on SBU1 and SBU2 are representative of the leakage of ESD and EMI/RFI components including termination to ensure no floating nodes, and are intended to show compliance with SBU Termination in USB Type-C r1.1. The plug orientation switch may be replaced by AUX polarity inversion logic in the DisplayPort transmitter or receiver, controlled by the plug orientation detection mechanism associated with the USB Type-C Receptacle. Note: The 3.3V levels in the Adapters are derived from VCONN because not all DisplayPort UFP_D devices provide DP_PWR.

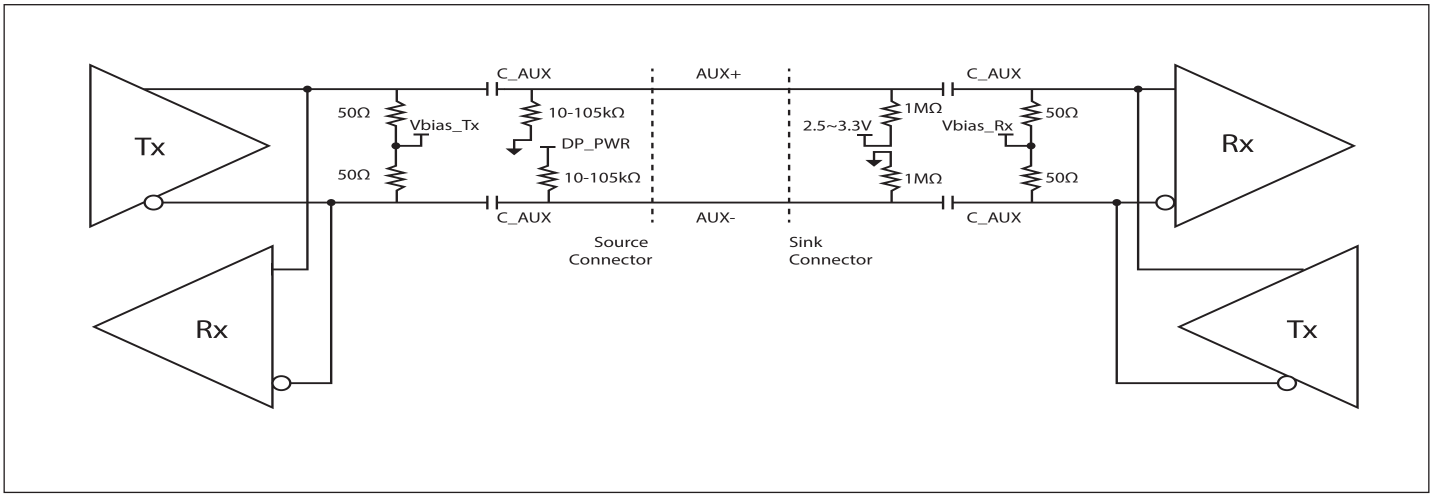


Figure 3. DisplayPort AUX Channel Connection

CTLE Equalization, Flat Gain and Chip Enable Controls

Table 3. CTLE Equalization Gain (Typical Values at FG = 0dB)

EQ<2:0>	Equalizer Setting (dB)							
HEX	@0.81GHz	@1.35GHz	@2.7GHz	@4.05GHz	@5.0GHz	@6.75GHz	@8.5GHz	@10.0GHz
000	-0.1	-0.1	0.1	0.7	1.3	2.7	4.4	6.0
001	0	0	0.6	1.6	2.5	4.5	6.7	8.5
010	0.1	0.2	1.3	2.8	4.1	6.5	8.9	10.8
011	0.2	0.6	2.2	4.3	5.8	8.5	11.0	12.7
100	0.4	1.1	3.5	6.0	7.7	10.4	12.7	14.2
101	0.7	1.7	4.8	7.6	9.3	11.9	13.9	15.2
110	1.2	2.6	6.3	9.2	10.8	13.1	14.8	15.8
111	1.6	3.5	7.5	10.4	11.8	13.9	15.3	16.2

Note: F: Floating, R: External resistor to ground.

Table 4. Flat Gain Setting (FG)

I2C Register FG[1:0]		Flat Gain Setting
0	0	-4 dB
0	1	-2 dB
1	0	+0 dB (Default)
1	1	+2 dB

Table 5. Chip Enable Control

I2C Register Setting or EN Pin (pin #15)	Channel Operation
0	Disabled
1	Enabled (Default)

Table 6. Device Slave Address Settings

Quad-Level Input Pin ADDR	I²C 7 Bit Slave Address						
L	1	0	1	0	0	0	0
R	1	0	1	0	0	0	1
F	1	0	1	0	0	1	0
H	1	0	1	0	0	1	1

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . –65°C to +150°C
Junction Temperature . . . . +125°C
Supply Voltage to Ground Potential . . . . –0.5V to VDD+0.3V
Voltage Input to High Speed Differential Pins . . . . . . –0.5V to VDD
Voltage Input to Low Speed Pins (SCL, SDA) . . . . . . –0.5V to +3.3V
Voltage Input to Low Speed Pins
(AUXP/N, SBU1, SBU2) . . . . –0.5V to 3.3V
Voltage Input to Low Speed Pins (EN) . . . . –0.5V to VDD+0.3V
ESD, HBM . . . . ±3000V
ESD CDM . . . . ±1000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Parameter	32-Pin X2QFN Package	Units
Theta JA	Junction to Ambient Thermal Resistance	49.7	°C/W

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	1.71	1.8	1.89	V
V_{DD_Noise}	Power Supply Noise Up to 50MHz	—	—	50	mVpp
V_{RX_CM}	Input Source Common-Mode Noise	—	—	150	mVpp
$C_{ac\_coupling}$	System AC Coupling Capacitance	75	—	265	nF
T_A	Ambient Temperature	-40(1)	—	+85	°C

Note:
1. The minimum temperature -40°C guaranteed by design

Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Units
$I_{ON\_U3\_2DP}$	1-port USB4 Gen 2.0/3.0 & 2-lane DPI 1.4/2.0		160	220	mA
I_{ON_4DP}	4-lane DP2.0		160	220	mA
I_{ON_USBx1}	1-port USB4 Gen 2.0/3.0 x1		80	110	mA
I_{ON_USBx2}	2-port USB Gen 2.0/3.0 x2		160	220	mA
I_{U1_U2}	USB U1/U2 power saving mode (per channel)		4	6	mA
I_{U3}	USB U3 power saving mode (per channel)		0.3	0.4	mA
I_{D3}	Display Port D3 power down mode		1	1.6	mA
I_{RxDet}	No connection		250	350	uA
I_{MStdby}	Modern standby mode, all Channels powered down thru I^2C		200	300	uA
I_{ENB}	Disabled mode (EN= Low)		8	30	uA

AC/DC Characteristics
(VDD = 1.8 ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	—	1.71	1.8	1.89	V
Receiver (RX) (100 Ω differential) Electrical Specification						
$R_{RX-DIFF-DC}$	DC Differential Input Impedance		72		120	Ω
$R_{RX-SINGLE-DC}$	DC single ended input impedance to guarantee RxDet	Measured with respect to GND over a voltage of 500mV max	18		30	Ω
$Z_{RX-HIZ-DC-PD}$	DC input CM input impedance for V>0 during reset or power down	(Vcm=0 to 500mV)	25			kΩ
$C_{ac\_coupling}$	AC coupling capacitance		75		265	nF
Transmitter (TX) Electrical Specification						
$V_{TX-DIFF-PP}$	Output differential p-p voltage Swing	Differential Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$			1	Vppd
$R_{TX-DIFF-DC}$	DC Differential TX Impedance		72		120	Ω
$V_{TX-RCV-DET}$	The amount of Voltage change allowed during RxDet	Type-C Tx Spec +/-60mA			600	mV
$C_{ac-coupling}$	AC coupling capacitance		75		265	nF
$R_{TX-DC-CM}$	Common mode DC output Impedance		18		30	Ω
$I_{TX-SHORT}$	Transmitter short circuit current limit				60	mA
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	VDD-1V		VDD	V
$V_{TX-DC-CM}$	Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\lvert V_{TX-D+} + V_{TX-D-} \rvert /2$	0		VDD	V
$V_{TX-CM-AC-PP-Active}$	Active mode TX AC common mode voltage	$V_{TX-D+} + V_{TX-D-}$ for amplitude			100	mVpp
V_ELEC_IDLE	Peak voltage during transmit electrical idle (one-side voltage opening of the differential signal)				20	mV
Channel Performance						
T_{pd}	Latency	From input to output		60	150	ps

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
G_{P_USB}	Peaking gain (Compensation at 10GHz, relative to 100MHz, 100mV$_{p-p}$ sine wave input)	EQ<2:0> = 000		6		dB
		EQ<2:0> = 001		8.5		
		EQ<2:0> = 010		10.8		
		EQ<2:0> = 011		12.7		
		EQ<2:0> = 100		14.2		
		EQ<2:0> = 101		15.2		
		EQ<2:0> = 110		15.8		
		EQ<2:0> = 111		16.2		
		Variation around typical	-2		+2	dB
G_F	Flat gain (100MHz, EQ<2:0>=000)	FG<1:0> = 00		-4		dB
		FG<1:0> = 01		-2		
		FG<1:0> = 10		0		
		FG<1:0> = 11		+2		
		Variation around typical	-2		+2	dB
V_{sw_100M}	Output linear swing (at 100MHz)	EQ<2:0>=000		910		mVppd
V_{sw_10G}	Output linear swing (at 10GHz)	EQ<2:0>=000		1000		mVppd
DDNEXT	Differential near-end crosstalk	100MHz to 10GHz, Fig. 6		-30	-20	dB
DDFEXT (2)	Differential far-end crosstalk	100MHz to 10GHz, Fig. 7		-30	-20	dB
V_{NOISE_IN}	Input-referred noise	100MHz to 10GHz, EQ<2:0>=000, FG<1:0>=10		0.6		mV_{RMS}
		100MHz to 10GHz, EQ<2:0>=111, FG<1:0>=10		0.3		
V_{NOISE_OUT}	Output-referred noise	100MHz to 10GHz, EQ<2:0>=000, FG<1:0>=10		0.3		mV_{RMS}
		100MHz to 10GHz, EQ<2:0>=111, FG<1:0>=10		0.5		
S11DM	Input differential mode return loss	10MHz to 10GHz differential mode		-11.5	-8.1	dB
S11CM	Input common mode return loss	1GHz to 10GHz common mode		-10	-5	dB
S22DM	Output differential mode return loss	10MHz to 10GHz differential mode		-12.5	-8.1	dB
S22CM	Output common mode return loss	1GHz to 10GHz common mode		-8	-4	dB
LFPS and Unplug Detectors Electrical Specification						
F_{TH}	LFPS frequency detector	Detect the frequency of the input CLK pattern	100		400	MHz

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{RX\text{-}LFPS\text{-}DET\text{-}DIFF\text{-}P}$	Deep Slumber Mode detect threshold	LFPS signal threshold in U1/U2/U3 mode, the input impedance is set to 50Ω	100		300	mVppd
V_{TH_UPLUG}	Unplug Mode detect threshold	LFPS signal threshold in Unplug mode. The input impedance is set to 78KΩ.	200		600	mVppd
V_{TH_AM}	Active Mode Detector Threshold	Signal threshold in Active and Slumber mode	170		270	mVppd
T_{ON_UPLUG}	Turn-on time of Unplug Mode	TX pin to RX pin latency when input signal is LFPS			20	µs
T_{ON_DSM}	Turn-On time of Deep Slumber Mode	TX pin to RX pin latency when input signal is LFPS			5	µs
T_{ON_SM}	Turn-On time of Slumber mode	TX pin to RX pin latency when input signal is LFPS, 5Gbps, 10Gbps data			20	ns
T_{RXDET_ON}	RX_DET response time	RX termination changes from 78KΩ to 50Ω			15	ms
TON_SAVE	Ton from USB power saving mode to active mode (U1/U2/U3 to U0)	Resume time from U1/U2/U3 back to U0 from LFPS detection. The termination resistor remains at 50Ω.			5	µs
$T_{mode\_USB\_DP}$	Configuration transition time from USB mode to DP mode	From register bit written to mode swap.			500	µs
T_{mode_DP}	Configuration time from DP mode to USB mode	From register bit written to mode swap.			500	µs
DisplayPort Electrical Specification						
$V_{TX\text{-}C}$	Common-Mode Voltage	$\mid V_{TX\text{-}D+} + V_{TX\text{-}D-} \mid /2$	VDD-1V		VDD	V
$V_{TX\text{-}AC\text{-}CM\_HBR\_RBR}$	TX AC common mode voltage for HRB and RBR	Measured using an 8b/10b pattern with 50% transition density			20	mVrms
$V_{TX\text{-}AC\text{-}CM\_HBR2}$	TX AC common mode voltage for HBR2				30	mVrms
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level0}$	Differential peak-to-peak output voltage swing Level 0	Tested with Pre-emphasis at Level 0= 0dB Level 1= 3.5dB Level 2= 6.0 dB	0.34	0.4	0.46	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential peak-to-peak output voltage swing Level 1		0.51	0.6	0.68	V
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential peak-to-peak output voltage swing Level 2		0.69	0.8	0.92	V

AC/DC Characteristics Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Tj TX Total Jitter	UHBR20(20Gbps) TP2	Measured at Transmit output. Prechannel loss from 2.5dB to 13dB			0.45	UI
	UHBR13(13.5Gbps) TP2				0.45	UI
	UHBR10(10Gbps) TP2				0.38	UI
	HBR3 (8.1Gbps)				0.27	UI
	HBR2 (5.4Gbps)				0.27	UI
	HBR (2.7Gbps)				0.294	UI
	RBR (1.62Gbps)				0.18	UI
AUX Channel Crossbar Switch and AUX Listener Electrical Specification						
V_{AUXDC}	AUX switch voltage range		0		3.3	V
$V_{AUX\text{-}DIFF\_PEAK}$	AUX switch peak-to-peak voltage		0.29		1.38	V
BW	-3dB bandwidth		100			MHz
R_{on}	The Resistance of AUX On	VCC = 1.8V; VI = 0 to 0.4V for AUXp; VI = 2.4V to 3.3V for AUXn Tests shall be performed in both normal and inverted orientations.			10	Ω
C_{in}	Input capacitance at SBU1, SBU2, AUXP or AUXN				10	pF
I_{leak}	Input leakage current at SBU1, SBU2, AUXP or AUXN	Measured at Vin(max)=3.3V			15	µA
I_{off}	Back current protection limit	When VDD is OFF and input voltage is 3.3V			10	uA
T_{on}	AUX switch turn-on time	From USB mode to DP mode transition			500	µs
T_{off}	AUX switch turn-off time	From DP mode to USB mode transition			500	µs
$VT_{(AUX\_listener)}$	Threshold of the AUX listener	VCC = 1.8V	100		220	mVPPd

Note:
1. Measured using a vector-network analyzer (VNA) with -30dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Subtract the channel gain from the total gain to derive the actual crosstalk

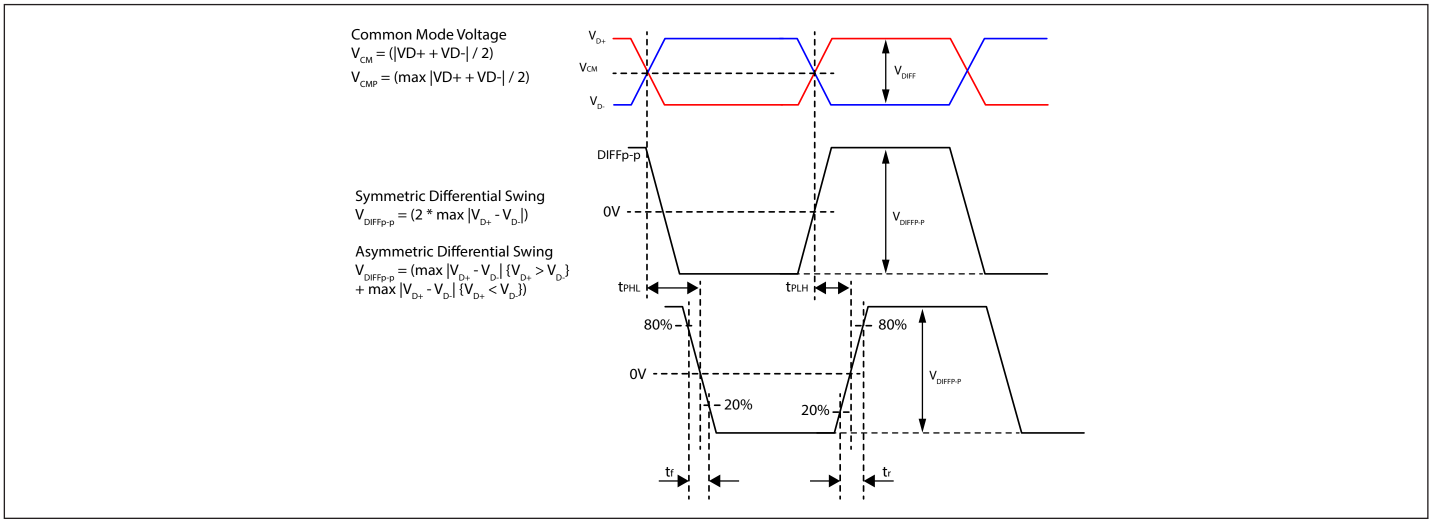


Figure 4. Definition of Peak-to-peak Differential Voltage

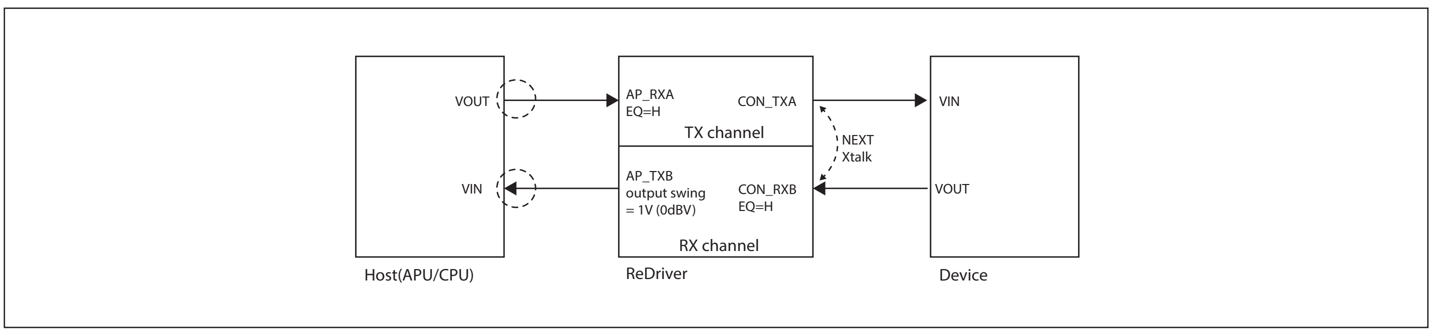


Figure 5. NEXT Crosstalk Definition

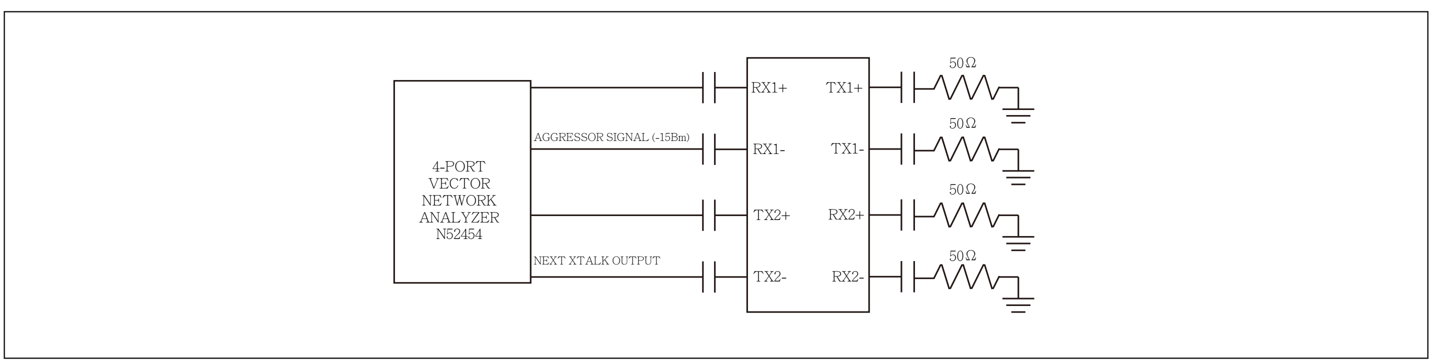


Figure 6. NEXT Channel-isolation Test Configuration

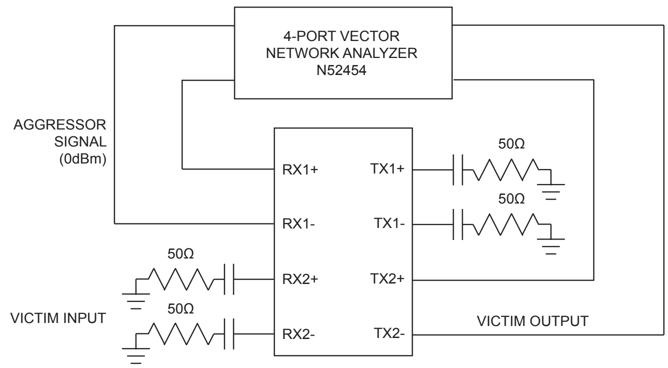
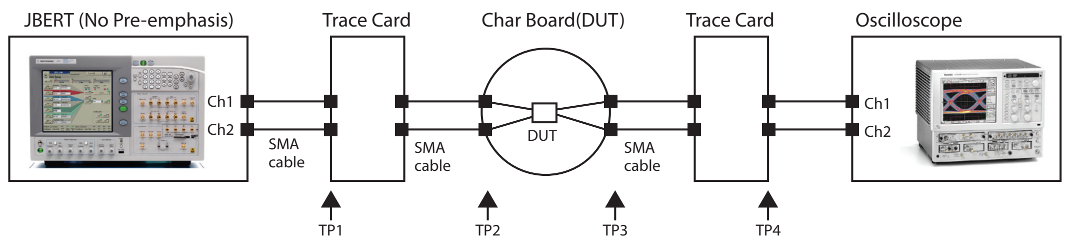


Figure 7. NEXT Channel-isolation Test Configuration



1) Trace card between TP1 and TP2 is designed to emulate 6-48" of FR4. Trace width -4 mils,100Ω differnetial impedance
2) All jitter is measured at a BER of 10-9
3) Residual jitter reflects the total jitter measured at TP4 jitter minus TP1 jitter
4) VDD = 1.8V, RT = 50Ω
5) The input signal from JBERT does not have any pre-emphasis.

Figure 8 Channel Measurement Setup

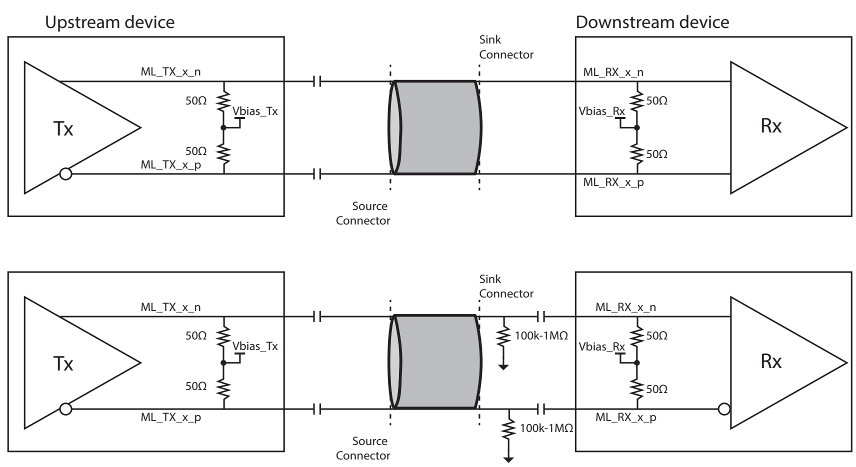


Figure 9. High-speed Channel Test Circuit

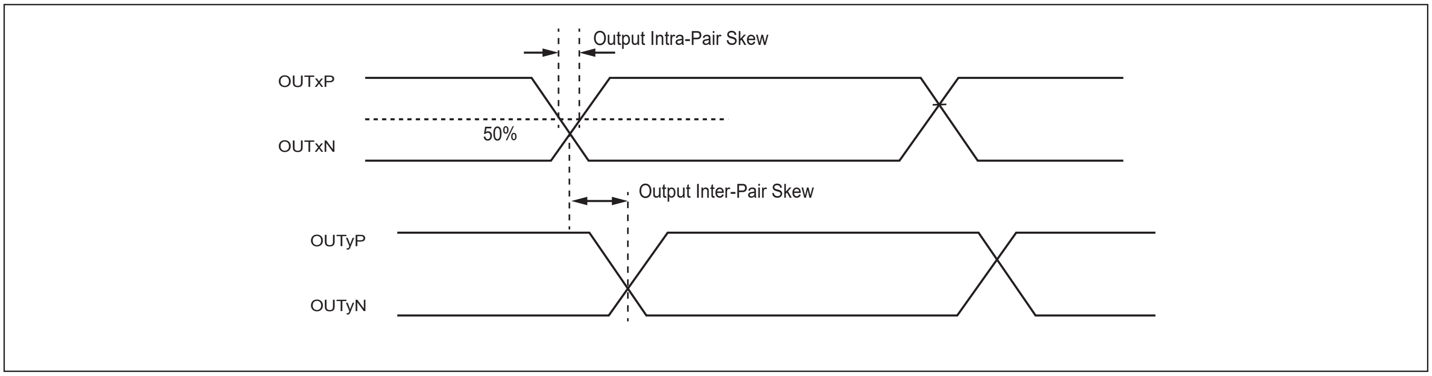


Figure 10. Intra and Inter-pair Differential Skew Definition

I2C Electrical Specification and Timing

Characteristics of the SDA and SCL I/O Stages

Symbol	Parameter	Conditions	This Silicon		Fast-mode Plus Spec		Units
			Min.	Max.	Min.	Max.	
V_{IL}	LOW-level input voltage		–0.5	$0.3V_{DD}$	–0.5	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$		$0.7V_{DD}$		V
V_{hys}	Hysteresis of Schmitt trigger inputs		$0.05V_{DD}$		$0.05V_{DD}$		V
V_{OL1}	LOW-level output voltage 1	Open-drain or open-collector at 3mA sink current; V_{DD} >2V	0	0.4	0	0.4	V
I_{OL}	LOW-level output current	V_{OL} =0.4V	20		20		mA
t_{of}	Output fall time from $V_{IH\text{-}min}$ to V_{ILmax}		12	120	20×(V_{DD} /5.5V)	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	0	50	ns
I_i	Input current each I/O pin	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	–10	+10	–10	+10	uA
C_i	Capacitance for each I/O pin			10		10	pF

Characteristics of the SDA and SCL Bus Lines the Devices

Symbol	Parameter	Conditions	This Silicon		Fast-mode Plus Spec		Units
			Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency		10	1000	0	1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	0.26	-	0.26	-	us
t_{LOW}	LOW period of the SCL clock		0.5	-	0.5	-	us
t_{HIGH}	HIGH period of the SCL clock		0.26	-	0.26	-	us
$t_{SU;STA}$	Set-up time for a repeated START condition		0.26	-	0.26	-	us
$t_{SU;DAT}$	Data set-up time		50		50	-	ns
t_r	Rise time of both SDA and SCL signals			120	-	120	ns
t_f	Fall time of both SDA and SCL signals		12	120	20×(V_{DD} /5.5V)	120	ns
$t_{SU;STO}$	Set-up time for STOP condition		0.26	-	0.26	-	us
t_{BUF}	Bus free time between a STOP and START condition		0.5	-	0.5	-	us

Characteristics of the SDA and SCL Bus Lines the Devices Cont.

Symbol	Parameter	Conditions	This Silicon		Fast-mode Plus Spec		Units
			Min.	Max.	Min.	Max.	
C_b	Capacitive load for each bus line		-	550	-	550	pF
$t_{VD;DAT}$	Data valid time		-	0.45	-	0.45	us
$t_{VD;ACK}$	Data valid acknowledge time		-	0.45	-	0.45	us
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	$0.1V_{DD}$		$0.1V_{DD}$	-	V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)	$0.2V_{DD}$		$0.2V_{DD}$	-	V

Characteristics of the SDA and SCL I/O Stages

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{IL}	LOW-level input voltage[1]		-0.5	$0.3V_{DD}$	-0.5	$0.3V_{DD}$	-0.5	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage[1]		$0.7V_{DD}$	[2]	$0.7V_{DD}$	[2]	$0.7V_{DD}$[1]	[2]	V
V_{hys}	Hysteresis of Schmitt trigger inputs				$0.05V_{DD}$		$0.05V_{DD}$		V
V_{OL1}	LOW-level output voltage 1	Open-drain or open-collector at 3mA sink current; $V_{DD} > 2V$	0	0.4	0	0.4	0	0.4	V
V_{OL2}	LOW-level output voltage 2	Open-drain or open-collector at 2mA sink current[3]; $V_{DD} \leq 2V$			0	$0.2V_{DD}$	0	$0.2V_{DD}$	V
I_{OL}	LOW-level output current	V_{OL} =0.4V	3		3		20		mA
		V_{OL} =0.6V[4]			6				
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}			250[5]	$20\times(V_{DD}/5.5V)$[6]	250[5]	$20\times(V_{DD}/5.5V)$[6]	120[7]	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter				0	50[8]	0	50[8]	ns
I_i	Input current each I/O pin	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	-10	+10	-10[9]	+10[9]	-10[9]	+10[9]	µA
C_i	Capacitance for each I/O pin[10]			10		10		10	pF

Note:
1. Some legacy Standard-mode devices had fixed input levels of V_{IL} = 1.5V and V_{IH} = 3.0V. Refer to component datasheet.
2. Maximum $V_{IH} = V_{DD(max)}$ + 0.5V or 5.5V, which ever is lower. See component datasheet.
3. The same resistor value to drive 3mA at 3.0V V_{DD} provides the same RC time constant when using <2V V_{DD} with a smaller current draw.
4. In order to drive full bus load at 400kHz, 6mA I_{OL} is required at 0.6V V_{OL}. Parts not meeting this specification can still function, but not at 400kHz and 400pF.
5. The maximum t_f for the SDA and SCL bus lines quoted in Table 10 (300ns) is longer than the specified maximum t_{of} for the output stages (250ns). This allows series protection resistors (R_S) to be connected between the SDA/SCL pins and the SDA/SCL bus lines as shown in Figure 45 without exceeding the maximum specified t_f.
6. Necessary to be backwards compatible with Fast-mode.

7. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
8. Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
9. If V_{DD} is switched off, I/O pins of Fast-mode and Fast-mode Plus device must not obstruct the SDA and SCL lines.
10. Special purpose device such as multiplexers and switches may exceed this capacitance because they connect multiple paths together.

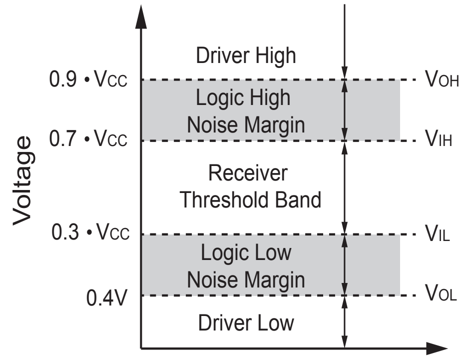


Figure 11. I2C I/O Stage Noise Margin

Characteristics of the SDA and SCL Bus Line for Standard, Fast, and Fast-mode Plus I2C-bus Device (1)

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	KHz
$t_{HD;STA}$	Hold time (repeated) START condition	After this period, the first clock pulse is generated.	4.0		0.6		0.26		µs
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		µs
t_{HIGH}	HIGH period of the SCL clock		4.0		0.6		0.26		µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7		0.6		0.26		µs
$t_{HD;DAT}$	Data hold time(2)	CBUS compatible masters	5.0						µs
		I2C-Bus Devices	0(3)	(4)	0(3)	(4)	0		
$t_{SU;DAT}$	Data set-up time		250		100(5)		50		ns
t_r	Rise time of both SDA and SCL signals			1000	20	300		120	ns
t_f	Fall time of both SDA and SCL signals(3)(6)(7)(8)			300	$20\times(V_{DD}/5.5V)$	300	$20\times(V_{DD}/5.5V)$(9)	120(8)	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0		0.6		0.26		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		µs
C_b	Capacitive load for each bus line(10)			400		400		550	pF
$t_{VD;DAT}$	Data valid time(11)			3.45(4)		0.9(4)		0.45(4)	µs

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{VD;ACK}$	Data valid acknowledge time(12)			3.45(4)		0.9(4)		0.45(4)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	$0.1V_{DD}$		$0.1V_{DD}$		$0.1V_{DD}$		V
V_{nH}	Noise margin at the HIGH level	For each connected device (including hysteresis)	$0.2V_{DD}$		$0.2V_{DD}$		$0.2V_{DD}$		V

Note:
1. All values referred to $V_{IH(min)}$ ($0.3V_{DD}$) and $V_{IL(max)}$ ($0.7V_{DD}$) levels.
2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum $t_{HD:DAT}$ could be 3.45µs and 0.9µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
5. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU:DAT}$ 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU:DAT} = 1000 + 250 = 1250$ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
6. If mixed with Hs-mode device, faster fall times according to Table XX are allowed.
7. The maximum t_f for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_f is specified are 250ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
8. In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
9. Necessary to be backwards compatible to Fast-mode.
10. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application. Section XX discusses techniques for coping with higher bus capacitances.
11. $t_{VS:DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
12. $t_{VS:ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).

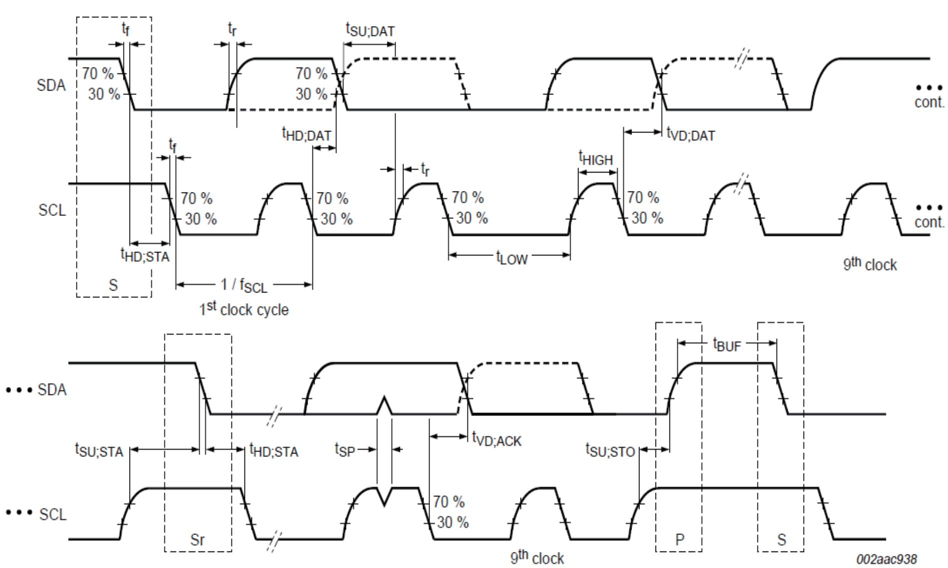
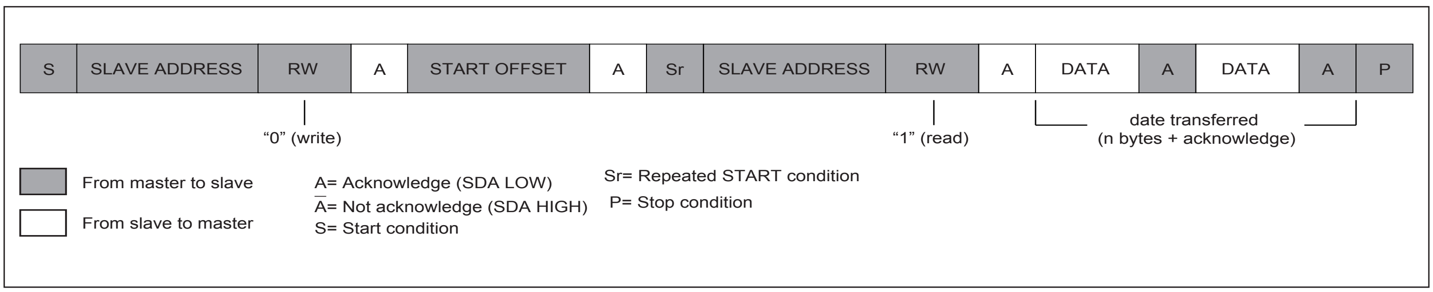


Figure 12. Definition of timing for F/S-mode devices on the I2C bus.

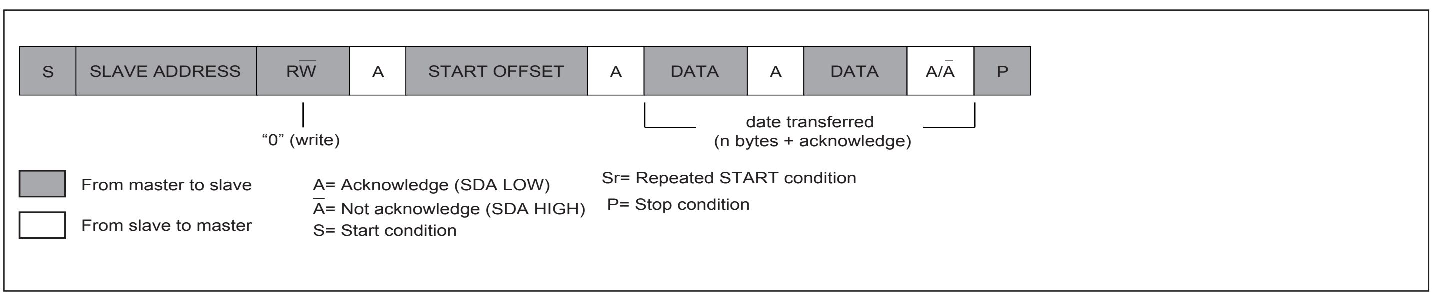
Detailed Programming Registers

I2C Slave Address Selections

I2C Slave Address Assignment							
A6	A5	A4	A3	A2	A1	A0	ADDR (Pin 16)
1	0	1	0	0	0	0	L
1	0	1	0	0	0	1	M
1	0	1	0	0	1	0	F
1	0	1	0	0	1	1	H



Indexed Read



Indexed Write

I2C Register Definitions

BYTE 0 (Revision and Vendor ID Register)			
Bit	Type	Power-up Condition	Comment
7	RO	0	Revision ID = 0000
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	Vendor ID = 0011
2	RO	0	
1	RO	1	
0	RO	1	

BYTE 1 (Device Type/Device ID Register)			
Bit	Type	Power-up Condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	1	
3	RO	0	Device ID = 0011
2	RO	0	
1	RO	1	
0	RO	1	

BYTE 2 (Byte Count Register 32 Bytes)			
Bit	Type	Power-up Condition	Comment
7	RO	0	I2C Register Byte Count = 32 bytes
6	RO	0	
5	RO	1	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	0	

BYTE 3 (Channel assignment of RXDET_EN#)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Operation Mode Setting Refer to Table Configuration Table
6	R/W	0	
5	R/W	0	
4	R/W	0	
3	R/W	0	Reserved
2	R/W	0	Enable/Disable RXDET_EN# 0 – RXDET is Enabled. 1 – RXDET is Disabled.
1	R/W	1	Reserved
0	R/W	1	Reserved

BYTE 4 (Override the Power Down Control)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	R/W	0		CON3 power down override 0 – Do not force the CON3 to power down state 1 – Force the CON3 to power down state
6	R/W	0		CON2 power down override 0 – Do not force the CON2 to power down state 1 – Force the CON2 to power down state
5	R/W	0		CON1 power down override 0 – Do not force the CON1 to power down state 1 – Force the CON1 to power down state
4	R/W	0		CON0 power down override 0 – Do not force the CON0 to power down state 1 – Force the CON0 to power down state
3	R/W	0		Reserved
2	R/W	1	IN_HPD_I2CMODE_EN	Select the HPD feature is controlled by either I2C register or IN_HPD pin 0 – PIN mode. The HPD feature is controlled by the IN_HPD pin. 1 – I2C mode. The HPD feature is controlled by the I2C register byte4<1>.
1	R/W	0	IN_HPD_ActiveHigh_EN# or IN_HPD_I2CMODE	When IN_HPD_I2CMODE_EN=0. This feature bit control the relationship between the HPD status and the setting of the IN_HPD pin. 0 – The HPD is asserted when IN_HPD pin is HIGH. 1 – The HPD is asserted when IN_HPD pin is LOW. When IN_HPD_I2CMODE_EN=1. This feature bit controls the HPD status by the I2C method 0 - HPD is de-asserted. 1 - HPD is asserted.
0	R/W	0		Reserved

BYTE 5 (Equalization and Flat Gain Setting of CON0)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON0_EQ<2> Equalizer setting
5	R/W	0	CON0_EQ<1> Equalizer setting
4	R/W	0	CON0_EQ<0> Equalizer setting
3	R/W	1	CON0_FG<1> Flat gain setting
2	R/W	0	CON0_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 6 (Equalization and Flat Gain Setting of CON1)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON1_EQ<2> Equalizer setting
5	R/W	0	CON1_EQ<1> Equalizer setting
4	R/W	0	CON1_EQ<0> Equalizer setting
3	R/W	1	CON1_FG<1> Flat gain setting
2	R/W	0	CON1_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 7 (Equalization and Flat Gain Setting of CON2)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON2_EQ<2> Equalizer setting
5	R/W	0	CON2_EQ<1> Equalizer setting
4	R/W	0	CON2_EQ<0> Equalizer setting
3	R/W	1	CON2_FG<1> Flat gain setting
2	R/W	0	CON2_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 8 (Equalization and Flat Gain Setting of CON3)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	0	CON3_EQ<2> Equalizer setting
5	R/W	0	CON3_EQ<1> Equalizer setting
4	R/W	0	CON3_EQ<0> Equalizer setting
3	R/W	1	CON3_FG<1> Flat gain setting
2	R/W	0	CON3_FG<0> Flat gain setting
1	R/W	0	Reserved
0	R/W	0	Reserved

BYTE 9 (AUX Flip Control)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	1	Reserved
5	R/W	1	Reserved
4	R/W	0	Reserved
3	R/W	0	Reserved
2	R/W	0	Reserved
1	R/W	0	AUX flip for CON_AUXP/N and AUXP/N 0 – Flip is disabled 1 – Flip is enabled
0	R/W	0	DP FLIP DP flip for ALL CONx channels 0 – DP Flip is Disabled 1 – DP Flip is Enabled

BYTE 10 (Reserved)			
Bit	Type	Power-up Condition	Comment
7	R/W	1	Reserved
6	R/W	1	
5	R/W	1	
4	R/W	1	
3	R/W	1	
2	R/W	1	
1	R/W	0	
0	R/W	0	

BYTE 11 (Reserved)			
Bit	Type	Power-up Condition	Comment
7	R/W	1	Reserved
6	R/W	1	
5	R/W	1	
4	R/W	1	
3	R/W	1	
2	R/W	1	
1	R/W	0	
0	R/W	0	

BYTE 12 (Reserved)			
Bit	Type	Power-up Condition	Comment
7	R/W	0	Reserved
6	R/W	0	
5	R/W	1	
4	R/W	1	
3	R/W	0	
2	R/W	0	
1	R/W	0	
0	R/W	1	

BYTE 13 (Power State of the Channel CON0/1)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	RO	0	CON0_State<2>	For the channel operating mode 000 – PD (Power down mode) 001 – PowerON (Power on ramping mode) 010 – UPM_Short (UPM less than 328ms) 011 – UPM_Long (UPM more than 328ms) 100 - UPM_Active (Unplug active mode) 101 - DSM (U1/U2/U3 power saving mode) 110 – SM (Slumber Mode) 111 - AM (active mode)
6	RO	0	CON0_State<1>	
5	RO	0	CON0_State<0>	
4	RO	0	Reserved	
3	RO	0	CON1_State<2>	
2	RO	0	CON1_State<1>	
1	RO	0	CON1_State<0>	
0	RO	0	Reserved	

BYTE 14 (Power State of the Channel CON2/3)				
Bit	Type	Power-up Condition	Control Affected	Comment
7	RO	0	CON2_State<2>	For the channel operating mode 000 – PD (Power down mode) 001 – PowerON (Power on ramping mode) 010 – UPM_Short (UPM less than 328ms) 011 – UPM_Long (UPM more than 328ms) 100 - UPM_Active (Unplug active mode) 101 - DSM (U1/U2/U3 power saving mode) 110 – SM (Slumber Mode) 111 - AM (active mode)
6	RO	0	CON2_State<1>	
5	RO	0	CON2_State<0>	
4	RO	0	Reserved	
3	RO	0	CON3_State<2>	
2	RO	0	CON3_State<1>	
1	RO	0	CON3_State<0>	
0	RO	0	Reserved	

BYTE 15 (LFPS Detector Monitor and Channel Power Down Monitor)				
Bit	Type	Power-up Condition	Comment	
7	RO	1	CON3_USB_LFPS#	Has meaning for USB3.x application only. CONx_USB_LFPS# 0-LFPS data 1-5/10Gbps USB3.x data
6	RO	1	CON2_USB_LFPS#	
5	RO	1	CON1_USB_LFPS#	
4	RO	1	CON0_USB_LFPS#	
3	RO	1	PD_CON3_MON	Monitors the PD condition of each channel.
2	RO	1	PD_CON2_MON	
1	RO	1	PD_CON1_MON	
0	RO	1	PD_CON0_MON	

BYTE 16 (AUX and HPD Monitor)			
Bit	Type	Power-up Condition	Comment
7	RO	1	Reserved
6	RO	1	Reserved
5	RO	0	AUX_IDLE_DET# Detect the AUX activities "0" – Idle "1" – has activities
4	RO	1	DP_HPD The condition of IN_HPD 0 – De-asserted 1 – Asserted Notes: When DP_HPD_PIN_EN#=1, then, this value is 1 always.
3	RO	1	AP0_RX_SEL "0" AP0 is TX terminal. "1" AP0 is RX terminal
2	RO	1	AP3_RX_SEL "0" AP3 is TX terminal. "1" AP3 is RX terminal
1	RO	0	CON0_RX_SEL "0" CON0 is TX terminal. "1" CON0 is RX terminal
0	RO	0	CON3_RX_SEL "0" CON3 is TX terminal. "1" CON3 is RX terminal

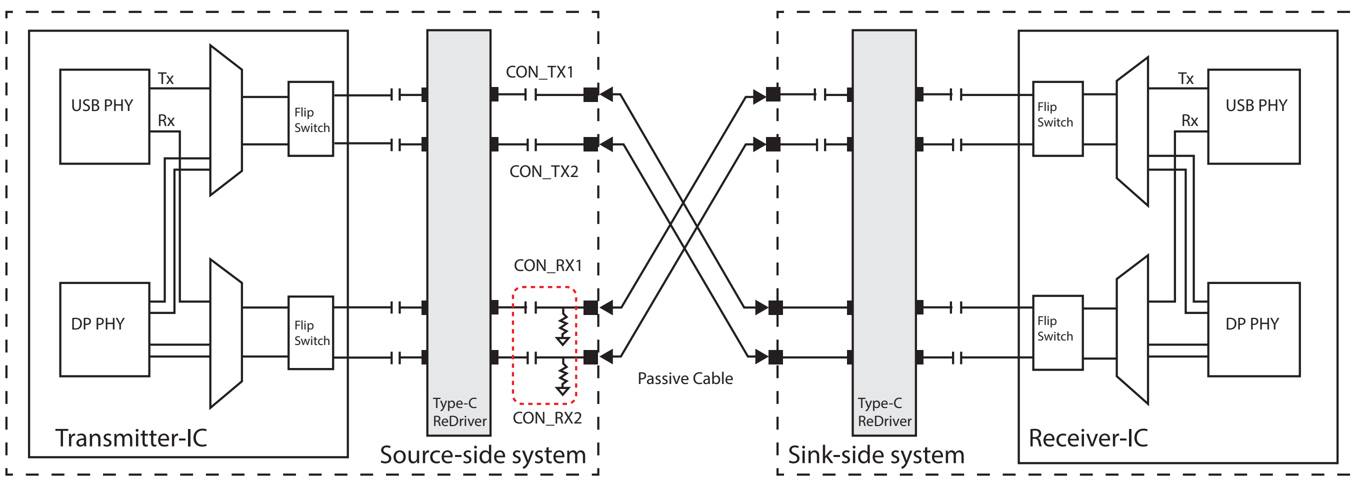
BYTE 17			
Bit	Type	Power-up Condition	Comment
7	RO	0	Reserved
6	RO	0	
5	RO	0	
4	RO	1	
3	RO	0	
2	RO	1	
1	RO	0	
0	RO	0	

BYTE 18 (DPCD Address 00101h: Lane Count Set)			
Bit	**Type**	**Power-up Condition**	**Comment**
7	RO	0	LANE_COUNT_SET Main-Link Lane Count = Value. Bit<4:0>LANE_COUNT_SET Three values are supported. All other values are RESERVED. Note: Because the upstream device is required to set this value within the MAX_LINK_RATE register (DPCD Address 00001h), there is no power-on reset default value for this field. It is suggested to program this field to 1h. (See the Note within the description for the LINK_BW_SET register (DPCD Address 00100h.) 1h = 1 lane (Lane 0 only) 2h = 2 lanes (Lanes 0 and 1 only) 4h = 4 lanes A Source device may choose any lane count as long as it does not exceed the capability of the DPRX. For DPCD Ver.1.0: Bits <7:5> = RESERVED. Read all 0's. For DPCD Ver.1.1: Bits <6:5> = RESERVED. Read all 0's. Bit 7 = ENHANCED_FRAME_EN 0 = Enhanced Framing symbol sequence is not enabled. 1 = Enhanced Framing symbol sequence for BS and SR is enabled. Applicable to SST-only mode. A DPTX must set this bit to 1 when the DPRX has the ENHANCED_FRAME_CAP bit in the MAX_LANE_COUNT register (DPCD Address 00002h, bit 7) set to 1.
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	
2	RO	1	
1	RO	0	
0	RO	0	

BYTE 19 - 30 (Reserved)

BYTE 31 (DPCD Address 00600h: SET DP Power)			
Bit	**Type**	**Power-up Condition**	**Comment**
7	RO	0	SET_POWER_STATE Bit 2:0 001 = Set local Sink device and all downstream Sink devices to D0 (normal operation mode). 010 = Set local Sink device and all downstream Sink devices to D3 (power-down mode). 101 = Set Main-Link for local Sink device and all downstream Sink devices to D3 (power-down mode), keep AUX block fully powered, ready to reply within a Response Timeout period of 300us. All other values are RESERVED.
6	RO	0	
5	RO	0	
4	RO	0	
3	RO	0	
2	RO	0	
1	RO	0	
0	RO	1	

Application Schematics



Note: AC-cap is recommended for potential Type-C Sink Device compatibility (interoperability) issues because of the different Type-C legacy implementation, not latest Type-C Logo compiant devices.

Figure 13. Type-C Coupling Capacitor Connection Diagram

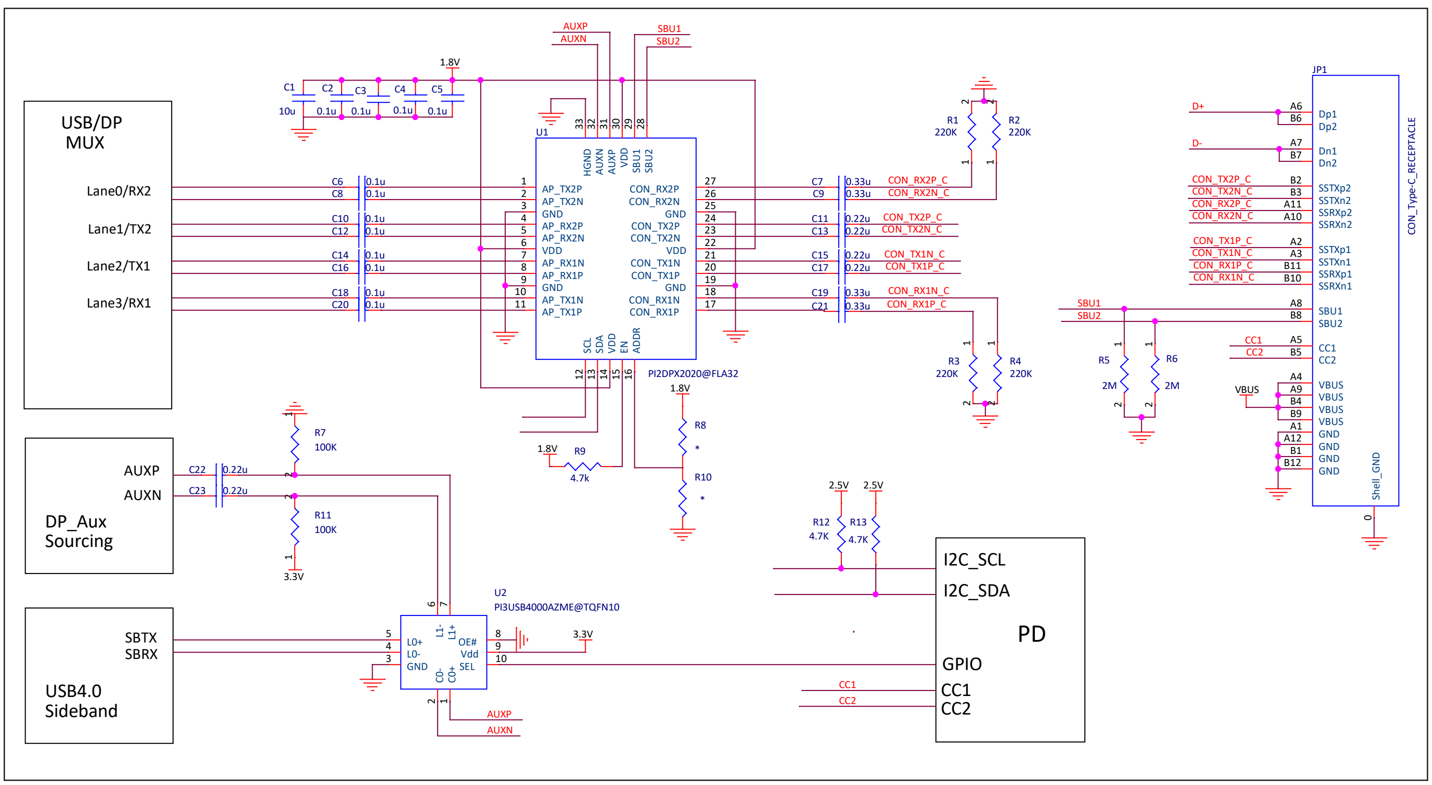
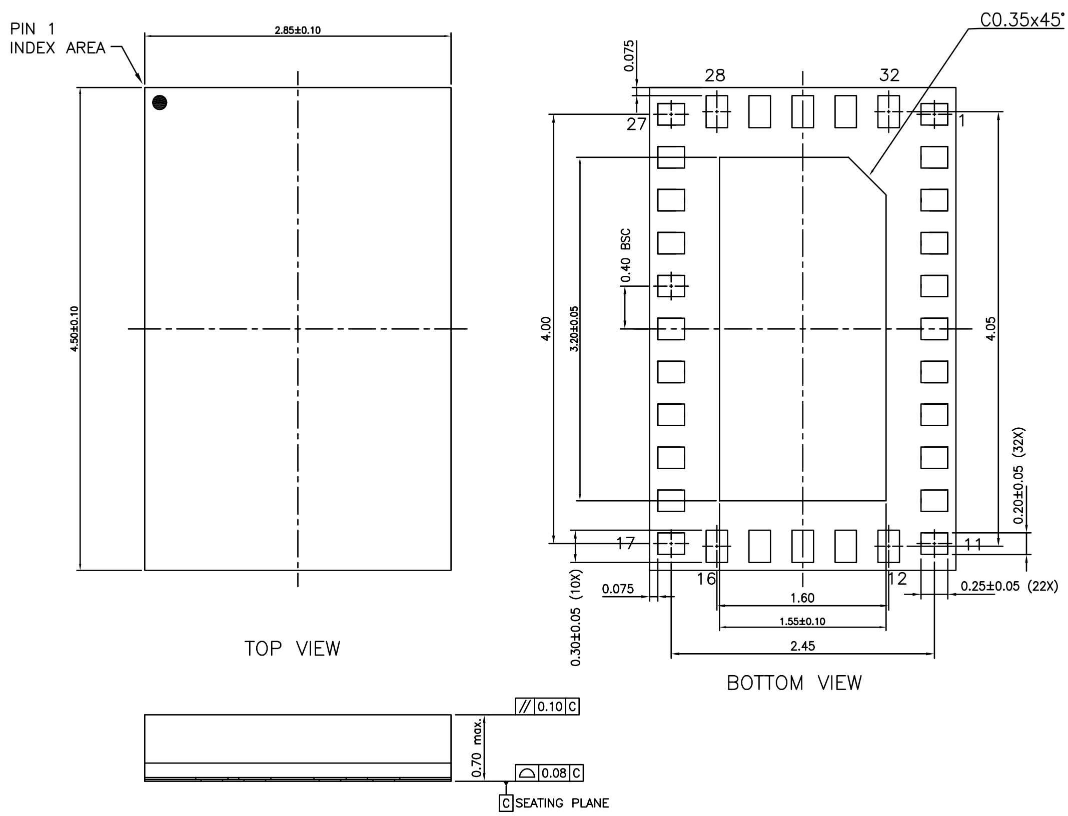


Figure 14. Type-C DFP Application Schematic

Packaging Mechanical

32-WLGA (FLA)



DIODES INCORPORATED — PERICOM A PRODUCT LINE OF DIODES INCORPORATED — ENABLING SERIAL CONNECTIVITY

DATE: 06/21/21

DESCRIPTION: 32-Pin, W-LGA4528-32

PACKAGE CODE: FLA (FLA32)

DOCUMENT CONTROL #: PD-2268 **REVISION: --**

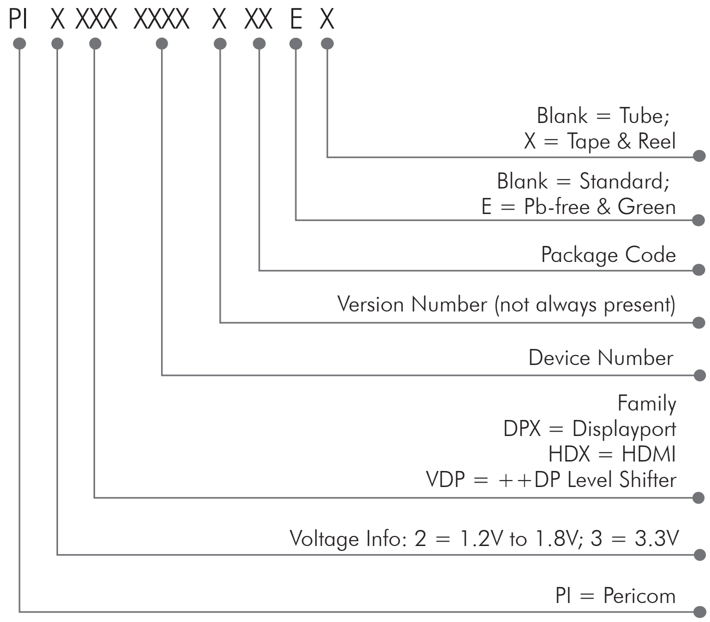
NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES

22-0634

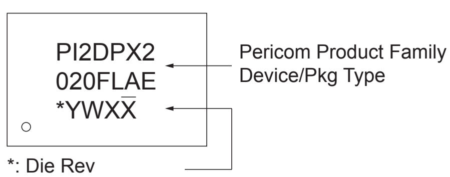
For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Device Naming Information



Part Marking



*: Die Rev
Y: Year
W: Week
1st X: Assembly Code
2nd X: Fab Code
Note: Date Code per MA-1251

Tape & Reel Materials and Design

Carrier Tape

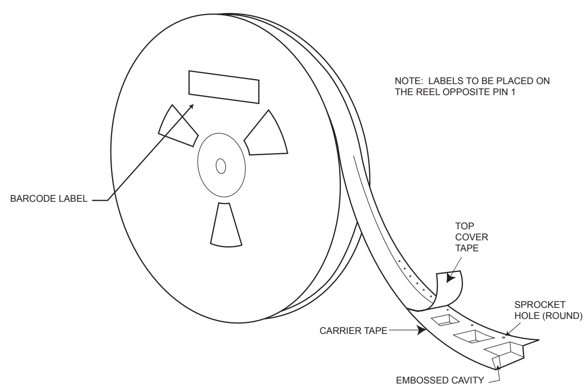
The pocketed carrier tape is made of conductive polystyrene plus carbon material (or equivalent). The surface resistivity is 106Ω/sq. maximum. Pocket tapes are designed so that the component remains in position for automatic handling after cover tape is removed. Each pocket has a hole in the center for automated sensing if the pocket is occupied or not, thus facilitating device removal. Sprocket holes along the edge of the center tape enable direct feeding into automated board assembly equipment. See figures 3 and 4 for carrier tape dimensions.

Cover Tape

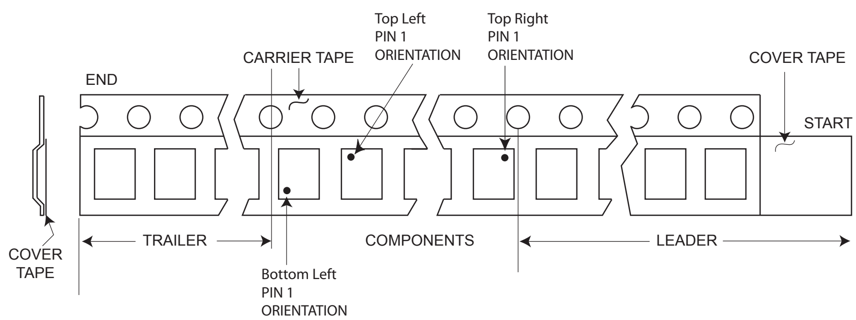
Cover tape is made of anti-static transparent polyester film. The surface resistivity is 107Ω/sq. Minimum to 1011Ω/sq. maximum. The cover tape is heat-sealed to the edges of the carrier tape to encase the devices in the pockets. The force to peel back the cover tape from the carrier tape shall be a MEAN value of 20gm to 80gm (2N to 0.8N).

Reel

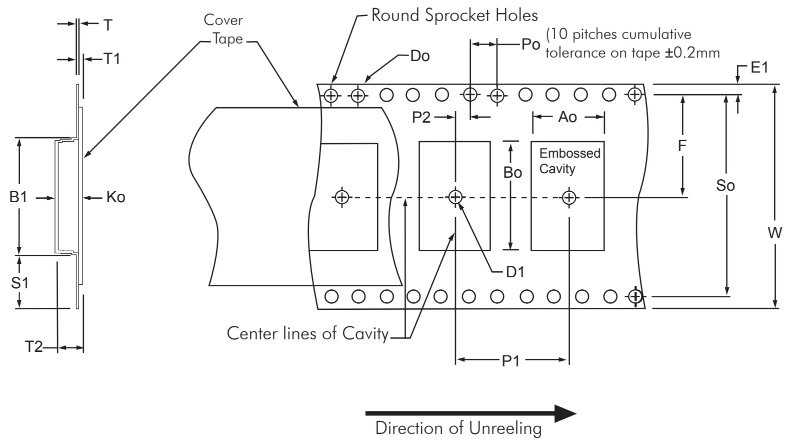
The device loading orientation is in compliance with EIA-481, current version (Figure 2). The loaded carrier tape is wound onto either a 13-inch reel (Figure 4) or 7-inch reel. The reel is made of Antistatic High-Impact Polystyrene. The surface resistivity 107Ω/sq. minimum to 1011Ω/sq. maximum.



Tape & Reel Label Information



Tape Leader and Trailer Pin 1 Orientations



Standard Embossed Carrier Tape Dimensions

Tape & Reel Dimensions

Constant Dimensions

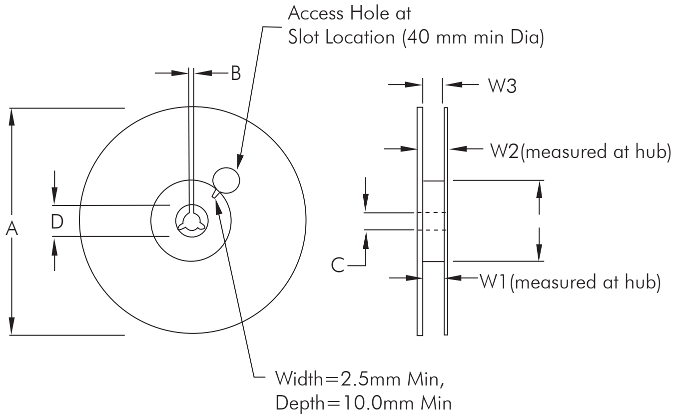
<table>
<tr><th>TAPE SIZE</th><th>D_0</th><th>D_1 (Min)</th><th>E_1</th><th>P_0</th><th>P_2</th><th>R [2]</th><th>S_1 (Min)</th><th>T (Max)</th><th>T_1 (Max)</th></tr>
<tr><td>8mm</td><td rowspan="6">1.5 +0.1-0.0</td><td>1.0</td><td rowspan="6">1.75 ± 0.1</td><td rowspan="6">4.0 ± 0.1</td><td rowspan="2">2.0 ± 0.05</td><td>25</td><td rowspan="4">0.6</td><td rowspan="6">0.6</td><td rowspan="6">0.1</td></tr>
<tr><td>12mm</td><td rowspan="3">1.5</td><td rowspan="3">30</td></tr>
<tr><td>16mm</td><td rowspan="3">2.0 ± 0.1</td></tr>
<tr><td>24mm</td></tr>
<tr><td>32mm</td><td rowspan="2">2.0</td><td rowspan="2">50</td><td rowspan="2">N/A [3]</td></tr>
<tr><td>44mm</td><td>2.0 ± 0.15</td></tr>
</table>

Variable Dimensions

<table>
<tr><th>TAPE SIZE</th><th>P_1</th><th>B_1 (Max)</th><th>E_2 (Min)</th><th>F</th><th>So</th><th>T_2 (Max)</th><th>W (Max)</th><th>A_0, B_0 &K_0</th></tr>
<tr><td>8mm</td><td rowspan="6">Specific per package type. Refer to FR-0221 (Tape and Reel Packing Information) or visit www.diodes.com/assets/MediaList-Attachments/Diodes-Tape-Reel-Tube.pdf</td><td>4.35</td><td>6.25</td><td>3.5 ± 0.05</td><td rowspan="4">N/A [4]</td><td>2.5</td><td>8.3</td><td rowspan="6">See Note 1</td></tr>
<tr><td>12mm</td><td>8.2</td><td>10.25</td><td>5.5 ± 0.05</td><td>6.5</td><td>12.3</td></tr>
<tr><td>16mm</td><td>12.1</td><td>14.25</td><td>7.5 ± 0.1</td><td>8.0</td><td>16.3</td></tr>
<tr><td>24mm</td><td>20.1</td><td>22.25</td><td>11.5 ± 0.1</td><td rowspan="2">12.0</td><td>24.3</td></tr>
<tr><td>32mm</td><td>23.0</td><td>N/A</td><td>14.2 ± 0.1</td><td>28.4 ± 0.1</td><td>32.3</td></tr>
<tr><td>44mm</td><td>35.0</td><td>N/A</td><td>20.2 ± 0.15</td><td>40.4 ± 0.1</td><td>16.0</td><td>44.3</td></tr>
</table>

NOTES:

1. A_0, B_0, and K_0 are determined by component size. The cavity must restrict lateral movement of component to 0.5mm maximum for 8mm and 12mm wide tape and to 1.0mm maximum for 16mm, 24mm, 32mm, and 44mm wide carrier. The maximum component rotation within the cavity must be limited to 20o maximum for 8 and 12 mm carrier tapes and 10o maximum for 16mm through 44mm.
2. Tape and components will pass around reel with radius "R" without damage.
3. S_1 does not apply to carrier width ≥32mm because carrier has sprocket holes on both sides of carrier where $D_o \geq S_1$.
4. S_o does not exist for carrier ≤32mm because carrier does not have sprocket hole on both side of carrier.



Reel Dimensions By Tape Size

TAPE SIZE	A	N (Min) [1]	W_1	W_2 (Max)	W_3	B (Min)	C	D (Min)
8mm	178 ± 2.0mm or 330 ± 2.0mm	60 ± 2.0mm or 100 ± 2.0mm	8.4 +1.5/-0.0mm	14.4mm	Shall Accommodate Tape Width Without Interference	1.5mm	13.0 +0.5/-0.2 mm	20.2mm
12mm			12.4 +2.0/-0.0mm	18.4mm				
16mm	330 ± 2.0mm	100 ± 2.0mm	16.4 +2.0/-0.0mm	22.4mm				
24mm			24.4 +2.0/-0.0mm	30.4mm				
32mm			32.4 +2.0/-0.0mm	38.4mm				
44mm			44.4 +2.0/-0.0mm	50.4mm				

NOTE:
1. If reel diameter A=178 ±2.0mm, then the corresponding hub diameter (N(min) will by 60 ±2.0mm. If reel diameter A=330±2.0mm, then the corresponding hub diameter (N(min)) will by 100±2.0mm.

IMPORTANT NOTICE