

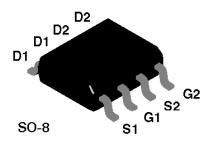
# NDS8961 Dual N-Channel Enhancement Mode Field Effect Transistor

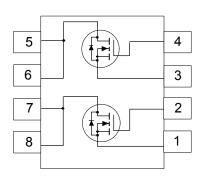
## **General Description**

SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

## **Features**

- High density cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		NDS8961	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
$V_{GSS}$	Gate-Source Voltage		±20	V
D	Drain Current - Continuous (N	Note 1a)	3.1	А
	- Pulsed		10	
<b>)</b> D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation (N	Note 1a)	1.6	
	7)	Note 1b)	1	
	(N	lote 1c)	0.9	
$\Gamma_{J}$ , $T_{STG}$	Operating and Storage Temperature Range		-55 to 150	°C
THERMA	L CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (No	ote 1a)	78	°C/W
R <sub>euc</sub>	Thermal Resistance, Junction-to-Case (No	ote 1)	40	°C/W

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
OFF CHA	RACTERISTICS						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V				1	μA
			T <sub>J</sub> = 55°C			10	μA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAR	ACTERISTICS (Note 2)			3	•		•
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.6	3	V
			T <sub>J</sub> = 125°C	0.7	1.2	2	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 3.1 \text{ A}$	•		0.072	0.1	Ω
			T <sub>J</sub> = 125°C		0.107	0.18	
		$V_{GS} = 4.5 \text{ V}, I_{D} = 2.6 \text{ A}$	•		0.116	0.15	
On-State Drain Current		$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	10			Α	
		$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		4			
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 3.1 \text{ A}$		4.3		S	
DYNAMIC	CHARACTERISTICS						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V},$	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V},$		190		pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz			120		pF
C <sub>rss</sub>	Reverse Transfer Capacitance				40		pF
SWITCHIN	IG CHARACTERISTICS (Note 2)						
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 10 \text{ V}, I_{D} = 1 \text{ A},$			7	15	ns
ţ	Turn - On Rise Time	$V_{GS}$ = 10 V, $R_{GEN}$ = 6 $\Omega$			15	30	ns
D(off)	Turn - Off Delay Time				14	28	ns
t <sub>f</sub>	Turn - Off Fall Time				3	6	ns
$Q_g$	Total Gate Charge	V <sub>DS</sub> = 10 V,			7.1	10	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 3.1 \text{ A}, V_{GS} = 10 \text{ V}$			1.2		nC
$Q_{gd}$	Gate-Drain Charge				1.9		nC

ELECTRIC	ELECTRICAL CHARACTERISTICS (T <sub>A</sub> = 25°C unless otherwise noted)									
Symbol	Parameter Conditions Min Typ Max Units									
DRAIN-SO	DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS									
I <sub>s</sub>	Maximum Continuous Drain-Source Diode Forward Current 1.3 A									
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)		0.79	1.2	V				

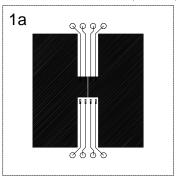
#### Notes

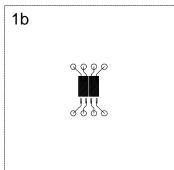
1. R<sub>BA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BA</sub> is guaranteed by design while R<sub>BCA</sub> is determined by the user's board design.

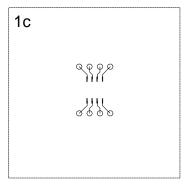
$$P_D(t) = \frac{T_J - T_A}{R_{\theta,JA}(t)} = \frac{T_J - T_A}{R_{\theta,JC} + R_{\theta,CA}(t)} = I_D^2(t) \times R_{DS(ON)} g_{T_J}$$

Typical  $R_{_{BJA}}$  for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



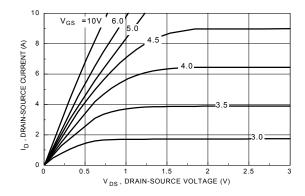




Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width  $\leq$  300 $\mu$ s, Duty Cycle  $\leq$  2.0%.

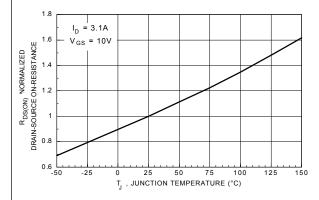
## **Typical Electrical Characteristics**



2.5 V<sub>GS</sub> = 3.5V 4.0 V<sub></sub>

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



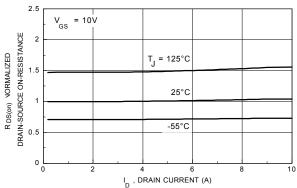
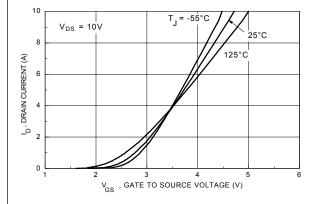


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



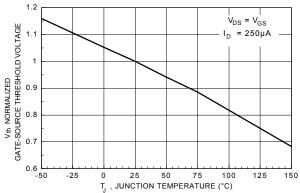


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

## **Typical Electrical Characteristics**

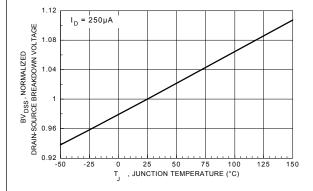


Figure 7. Breakdown Voltage Variation with Temperature.

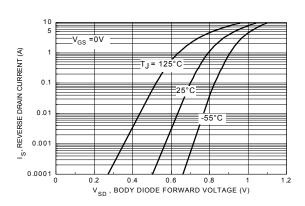


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

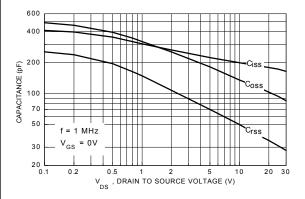


Figure 9. Capacitance Characteristics.

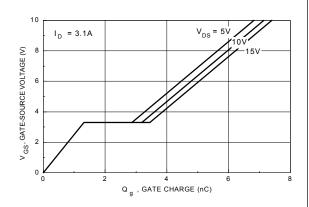


Figure 10. Gate Charge Characteristics.

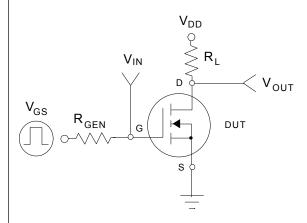


Figure 11. Switching Test Circuit.

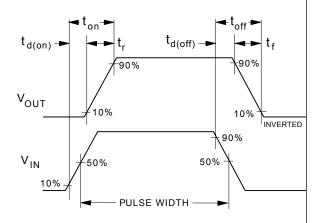


Figure 12. Switching Waveforms.

## **Typical Electrical and Thermal Characteristics**

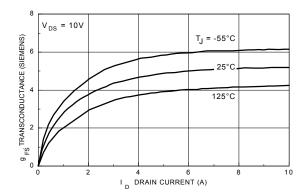


Figure 13. Transconductance Variation with Drain Current and Temperature.

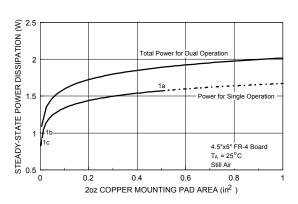


Figure 14. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

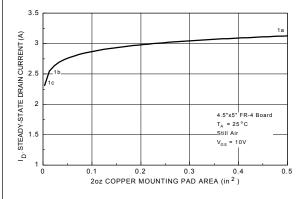


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

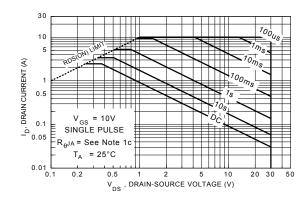


Figure 16. Maximum Safe Operating Area.

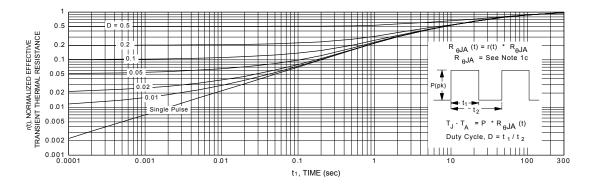
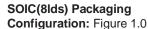


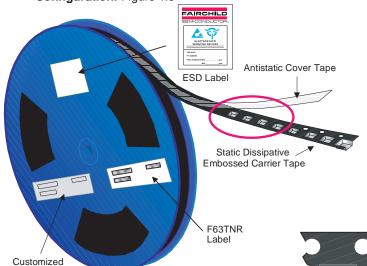
Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

# SO-8 Tape and Reel Data and Package Dimensions





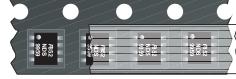


#### Packaging Description:

Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and amit-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13° or 300cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (antistatic coated). Other option comes in 500 units per 7° or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reles are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.





SOIC (8lds) Packaging Information									
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z					
Packaging type	TNR	Rail/Tube	TNR	TNR					
Qty per Reel/Tube/Bag	2,500	95	4,000	500					
Reel Size	13" Dia	-	13" Dia	7" Dia					
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47					
Max qty per Box	5,000	30,000	8,000	1,000					
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774					
Weight per Reel (kg)	0.6060	-	0.9696	0.1182					
Note/Comments									

**SOIC-8 Unit Orientation** 

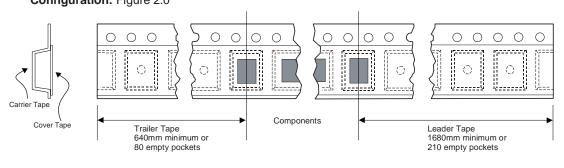


Label



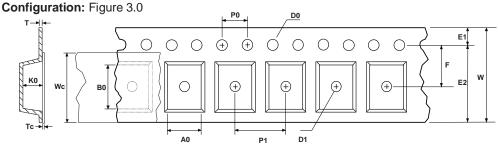
# 343mm x 342mm x 64mm Standard Intermediate box ESD Label F63TNLabel F63TN Label

# **SOIC(8lds) Tape Leader and Trailer Configuration:** Figure 2.0





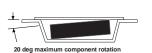
# SOIC(8lds) Embossed Carrier Tape



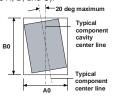


	Dimensions are in millimeter													
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

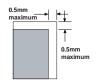


Sketch A (Side or Front Sectional View)
Component Rotation



Sketch B (Top View)

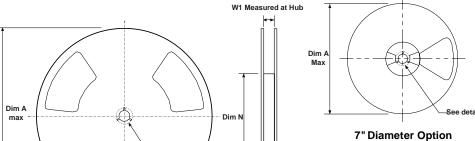
Component Rotation



Sketch C (Top View)

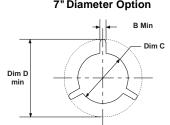
Component lateral movement

## SOIC(8lds) Reel Configuration: Figure 4.0



See detail AA W3

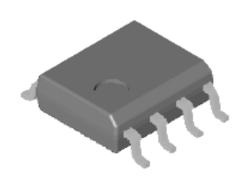
13" Diameter Option W2 max Measured at Hub

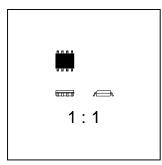


								DETAIL AA	ı
	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

# SO-8 Tape and Reel Data and Package Dimensions, continued

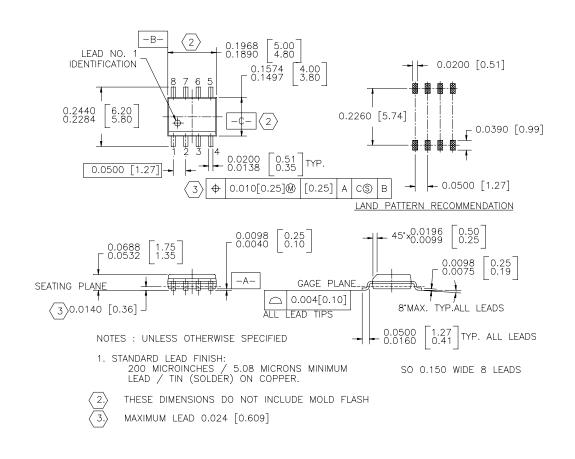
# SOIC-8 (FS PKG Code S1)





Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



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 $\begin{array}{lll} \mathsf{FAST}^{\circledast} & \mathsf{Quiet}\,\mathsf{Series^{\mathsf{TM}}} \\ \mathsf{FASTr^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}3} \\ \mathsf{GTO^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}6} \\ \mathsf{HiSeC^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}8} \\ \end{array}$ 

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

## **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.