

Fact Sheet

Military Semiconductor Products

SMQ320C32 (order as 5962-9679001NXB)

SGYV008D April 2001

SMQ320C32 (5962-9679001NXB) Digital Signal Processor

HIGHLIGHTS

The 320C3x family, can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. The processor also possesses a general-purpose register file, a program cache, dedicated auxiliary register arithmetic units (ARAU), internal dual-access memories, two DMA channels supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

The 320C32 is also an enhanced 32-bit floating-point processor. The enhancements include a variable-width external-memory interface, faster instruction cycle time, power-down modes, two-channel DMA coprocessor with configurable priorities, flexible boot loader, relocatable interrupt-vector table, and edge- or level-triggered interrupts.

PERFORMANCE

50MHz (50 MFLOPS) / 5% power supply (PCM package); QML Processing

DIE SIZE (Approximate)

320C32: 261 x 234 mils (die revision 3.1)

TECHNOLOGY

0.65 micron (Leff), triple-level-metal, EPIC™ G1ZSE CMOS

PACKAGING

PCM — 144-lead plastic quad flat pack with 25 mil lead spacing. Weight: 5.63 grams.

$R_{\theta_{JA}}$ — 39°C/W, $R_{\theta_{JC}}$ — 10°C/W

$R_{\theta_{JA}}$ Thermal resistance of a package without a path for heat dissipation. This is specified at a zero linear feet per minute air flow.

$R_{\theta_{JC}}$ Thermal resistance of a package assuming an infinite path for heat dissipation.

POWER DISSIPATION

Typical ICC: 200 mA

Maximum ICC: 425 mA

Explanation of Typical

vs. Peak power..... For average power and thermal management considerations, the typical value should be used. The peak power of the C32 is highly dependent on the instructions executing. The worst case pattern set occurs when checkerboard patterns are being loaded out both ports from both RAM blocks

TEST VECTORS

The SMQ320C32 has >500,000 test vectors. The actual test vectors are TI proprietary information.

DSCC SMD

TI Parent Device	Package	Speed	Order as: DSCC SMD
SMQ320C32PCMM50	144-Pin Plastic QFP	50 MHz	5962-9679001NXB

EPIC is a trademark of Texas Instruments.



TOOLS

For a complete listing of available development tools and more information on the items listed below, please visit the following TI 320C3x development tool web page: <http://focus.ti.com/docs/tool/matrix.jhtml?FamilyId=44>

ASSEMBLER.....	Converts assembly language to machine language.
LINKER.....	Combines object modules into a single executable object file, performs relocation and resolves external references.
C COMPILER.....	Translates C source code into 320C3X assembly source code.
ADA COMPILER....	Translates ADA source code into 320C3X assembly source code. See TI's C3x Ada Development tools page at the following URL: http://focus.ti.com/docs/tool/toolfolder.jhtml?PartNumber=C3X-ADA-XX&FamilyId=111
SIMULATOR.....	Software debugger tool that simulates the operation of the 320C3X.
XDS510.....	Hardware controller card for in-system emulation.
EVM.....	Evaluation Module. This package includes the TMS320C3X assembler/linker and the C source debugger. A TMS320C30 PC halfcard is also included in this low-cost, rich development environment.
TMS320C3x DSK...	DSP Starter Kit (DSK). The 'C3x DSK is a low-cost, simple, high-performance stand-alone application development board that lets you experiment with and use TMS320C3x DSPs for real-time signal processing.

ARCHITECTURE

The 320C32 uses a highly parallel, pipelined architecture. This is Von Neumann externally (simplifying the programmer's task) but Harvard internally (faster execution). These features are transparent to the user.

INTERNAL MEMORY...Two blocks of 256 x 32 dual access RAM. Each block can provide two accesses to the CPU or the DMA every cycle.

CACHE..... Two segments of 32 words each. Operates on the standard least-recently-used algorithm using a serial load.

DMA..... Two on chip concurrent direct memory access controllers. The DMA is able to off load I/O tasks from the CPU. The DMA acts independently of the CPU unless resources are needed by the CPU and DMA at the same time. To handle this conflict, the DMA has user-configurable priorities: CPU, DMA, or rotating between CPU and DMA.

DESIGN-IN SUPPORT

[TI has the most extensive DSP application support](#)

Product Information Center:	(972) 644-5580 (For general information, availability, etc.)
DSP Developer's Village:	http://dspvillage.ti.com/docs/dspvillagehome.jhtml
DSP Hotline (Technical questions):	http://www-k.ext.ti.com/cgi-bin/webcgi.exe?New.KB=dsp
C3x Information (Commerical)	http://dspvillage.ti.com/docs/catalog/dspplatform/otherdspdps.jhtml?familyID=497
C3x Information (Military)	http://www.ti.com/sc/docs/products/military/processr/320c3x.htm
Military DSP Info:	http://www.ti.com/sc/docs/products/military/processr/index.htm

Product Information Center

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Military Products – <http://www.ti.com/sc/military>
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