Freescale Semiconductor
Technical Data

Document Number: MRF5S9070NR1
Rev. 7, 6/2009

RoHS

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of this device make it ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

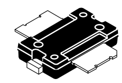
- Typical Single-Carrier N-CDMA Performance @ 880 MHz, V_{DD} = 26 Volts, I_{DQ} = 600 mA, P_{out} = 14 Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13)
  Power Gain — 17.8 dB
  Drain Efficiency — 30%
  ACPR @ 750 kHz Offset — -47 dBc in 30 kHz Bandwidth
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 70 Watts CW Output Power

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Integrated ESD Protection
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.

MRF5S9070NR1

880 MHz, 70 W, 26 V
SINGLE N-CDMA
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 1265-09, STYLE 1
TO-270-2
PLASTIC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	219 1.25	W W/°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 70 W CW Case Temperature 78°C, 14 W CW	$R_{\theta JC}$	 0.80 0.93	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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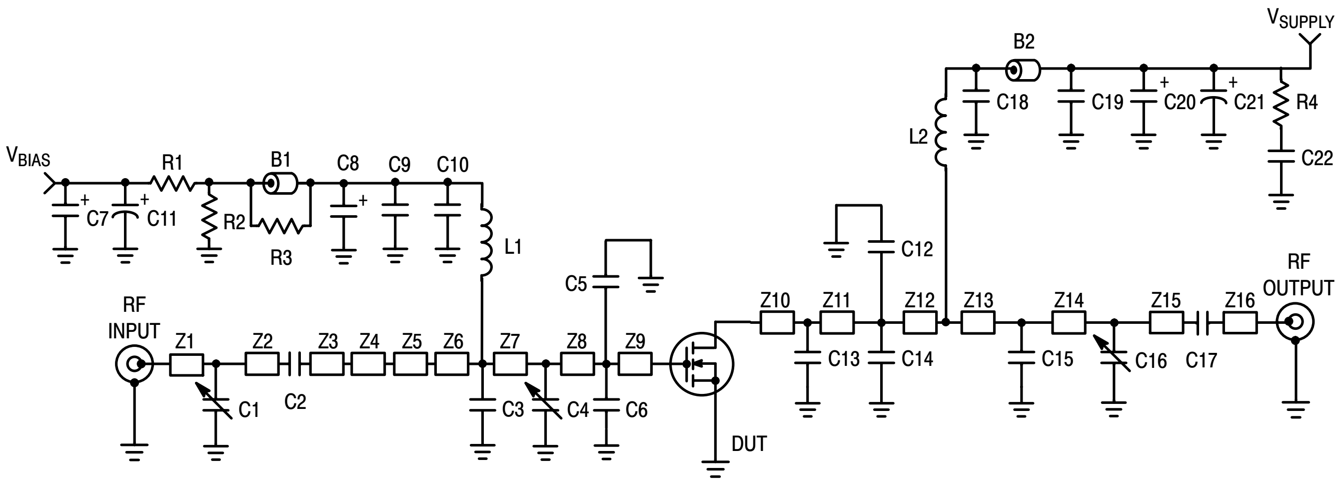
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μA)	$V_{GS(th)}$	2	2.7	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 600 mAdc)	$V_{GS(Q)}$	—	3.7	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	0.18	0.22	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	g_{fs}	—	4.7	—	S
Dynamic Characteristic					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	126	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	34	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.37	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ} = 600 mA, P_{out} = 14 W Avg., f = 880 MHz, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ ±750 kHz Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF					
Power Gain	G_{ps}	17	17.8	—	dB
Drain Efficiency	η_D	29	30	—	%
Adjacent Channel Power Ratio	ACPR	—	-47	-45	dBc
Input Return Loss	IRL	—	-19	-9	dB
Typical GSM CW Performances (In Freescale GSM Test Fixture Optimized for 921-960 MHz, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ} = 400 mA, P_{out} = 60 W, f = 921-960 MHz					
Power Gain	G_{ps}	—	16.4	—	dB
Drain Efficiency	η_D	—	62	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point (f = 940 MHz)	P1dB	—	68	—	W
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture Optimized for 921-960 MHz, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ} = 400 mA, P_{out} = 25 W Avg., f = 921-960 MHz, GSM EDGE Signal					
Power Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	44	—	%
Error Vector Magnitude	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical GSM CW Performances (In Freescale GSM Test Fixture Optimized for 865-895 MHz, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ} = 400 mA, P_{out} = 60 W, f = 865-895 MHz					
Power Gain	G_{ps}	—	16.4	—	dB
Drain Efficiency	η_D	—	59	—	%
Input Return Loss	IRL	—	-15	—	dB
P_{out} @ 1 dB Compression Point (f = 880 MHz)	P1dB	—	71	—	W
Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture Optimized for 865-895 MHz, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ} = 400 mA, P_{out} = 25 W Avg., f = 865-895 MHz, GSM EDGE Signal					
Power Gain	G_{ps}	—	17	—	dB
Drain Efficiency	η_D	—	41	—	%
Error Vector Magnitude	EVM	—	1.35	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-66	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-81	—	dBc

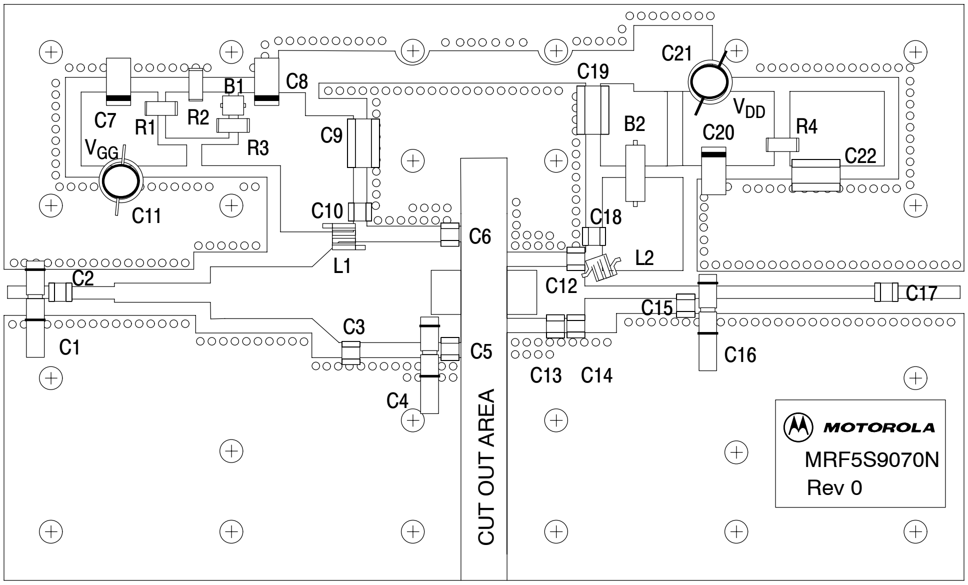


Z1	0.140″ x 0.060″ Microstrip	Z10	0.245″ x 0.270″ Microstrip
Z2	0.141″ x 0.060″ Microstrip	Z11	0.110″ x 0.270″ Microstrip
Z3	0.280″ x 0.060″ Microstrip	Z12	0.055″ x 0.270″ Microstrip
Z4	0.500″ x 0.100″ Microstrip	Z13	0.512″ x 0.060″ Microstrip
Z5	0.530″ x 0.270″ Microstrip	Z14	0.106″ x 0.060″ Microstrip
Z6	0.155″ x 0.270″ x 0.530″ Taper	Z15	0.930″ x 0.060″ Microstrip
Z7	0.376″ x 0.530″ Microstrip	Z16	0.365″ x 0.060″ Microstrip
Z8	0.116″ x 0.530″ Microstrip	PCB	Taconic RF-35, 0.030″, ε_r = 3.5
Z9	0.055″ x 0.530″ Microstrip		

Figure 1. MRF5S9070NR1 Test Circuit Schematic

Table 6. MRF5S9070NR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Small Ferrite Bead, Surface Mount	2743019447	Fair-Rite
B2	Large Ferrite Bead, Surface Mount	2743021447	Fair-Rite
C1	0.6-6.0 pF Variable Capacitor, Gigatrim	272715L	Johanson
C2	16 pF Chip Capacitor	ATC100B160JT500XT	ATC
C3	7.5 pF Chip Capacitor	ATC100B7R5JT500XT	ATC
C4, C16	0.8-8.0 pF Variable Capacitors, Gigatrim	272915L	Johanson
C5, C6	15 pF Chip Capacitors	ATC100B150JT500XT	ATC
C7, C8, C20	10 μF, 35 V Tantalum Capacitors	T491D106K035AT	Kemet
C9, C19, C22	0.58 μF Chip Capacitors	ATC700A561MT150XT	ATC
C10, C18	18 pF Chip Capacitors	ATC100B180JT500XT	ATC
C11	100 μF, 50 V Electrolytic Capacitor	515D107M050BB6AE3	Vishay
C12, C14	13 pF Chip Capacitors	ATC100B130JT500XT	ATC
C13	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
C15	3.9 pF Chip Capacitor	ATC100B3R9JT500XT	ATC
C17	22 pF Chip Capacitor	ATC100B180JT500XT	ATC
C21	470 μF, 63 V Electrolytic Capacitor	ESMG630ELL471MK20S	United Chemi-Con
L1, L2	12.5 nH Surface Mount Inductors	A04TJL	Coilcraft
R1	1 kΩ, 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	560 kΩ, 1/4 W Chip Resistor	CRCW12065600FKEA	Vishay
R3	12 Ω, 1/4 W Chip Resistor	CRCW120612R0FKEA	Vishay
R4	27 Ω, 1/4 W Chip Resistor	CRCW120627R0FKEA	Vishay



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF5S9070NR1 Test Circuit Component Layout

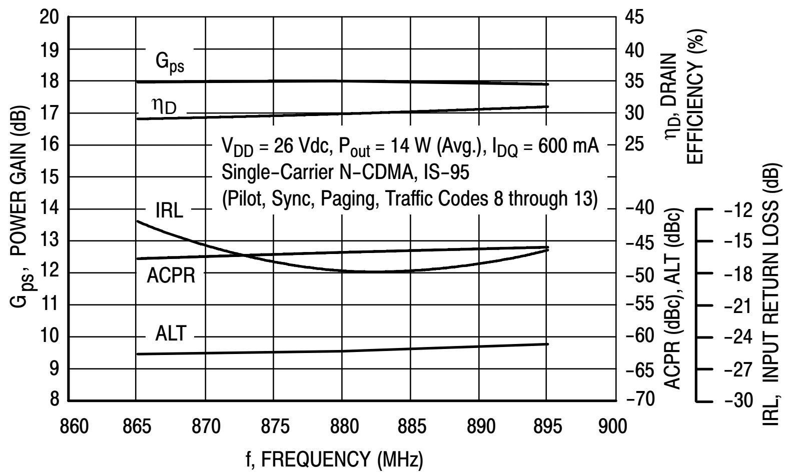


Figure 3. Class AB Broadband Performance

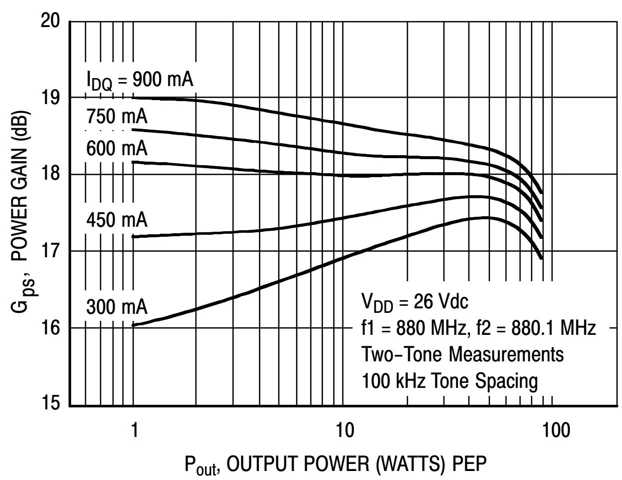


Figure 4. Two-Tone Power Gain versus Output Power

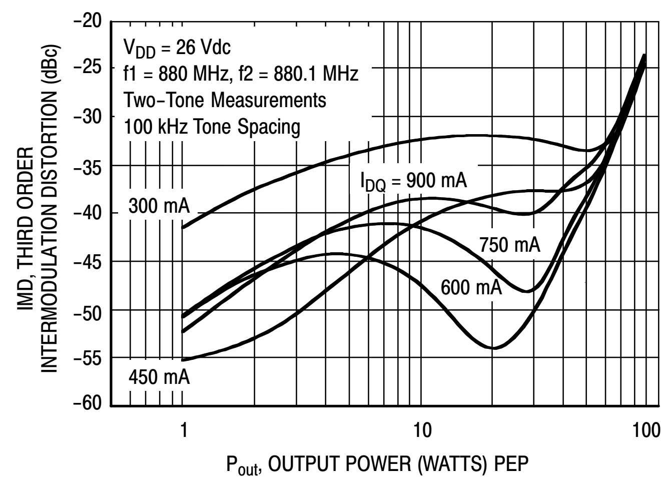


Figure 5. Third Order Intermodulation Distortion versus Output Power

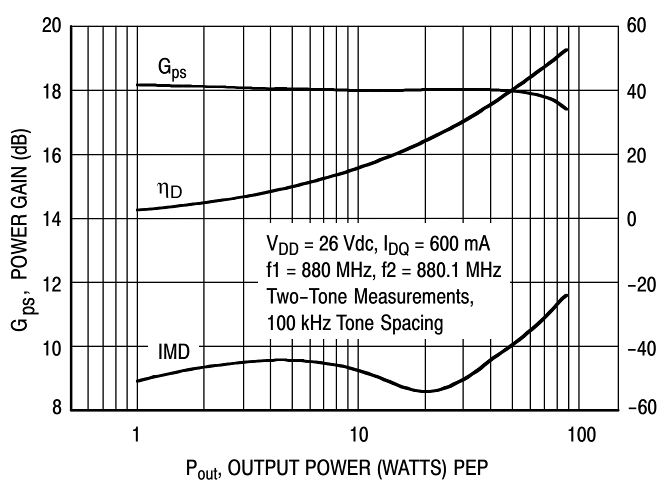


Figure 6. Power Gain, Drain Efficiency and IMD versus Output Power

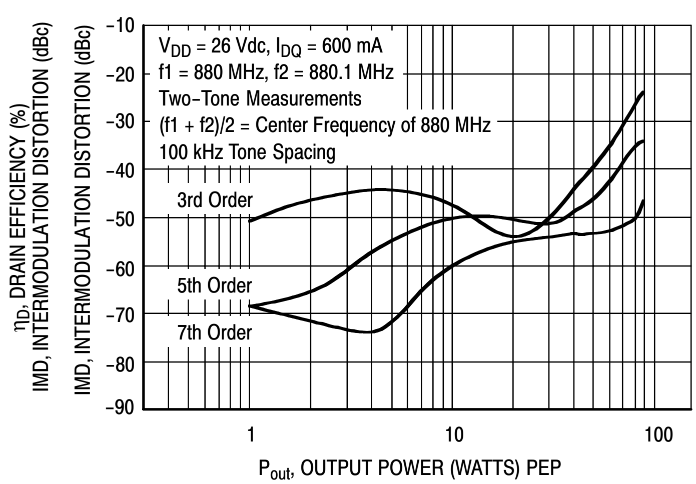


Figure 7. Intermodulation Distortion Products versus Output Power

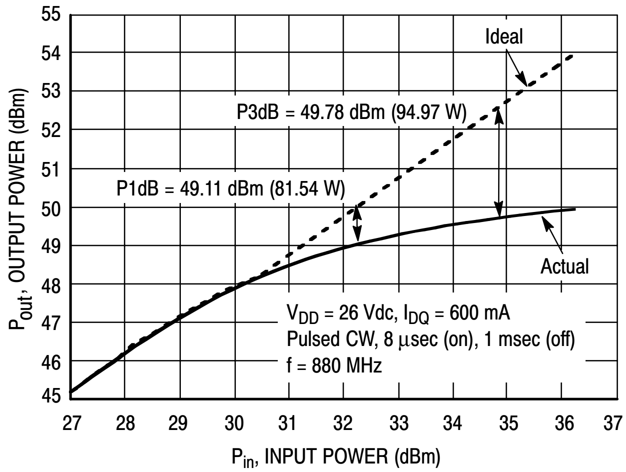


Figure 8. Pulse CW Output Power versus Input Power

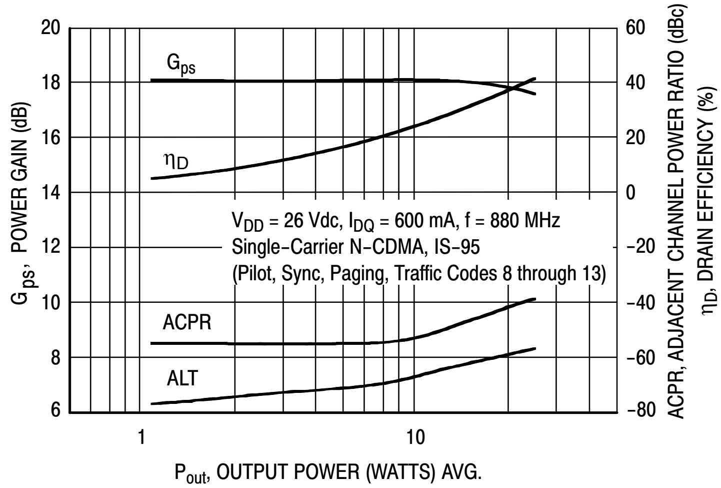


Figure 9. N-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

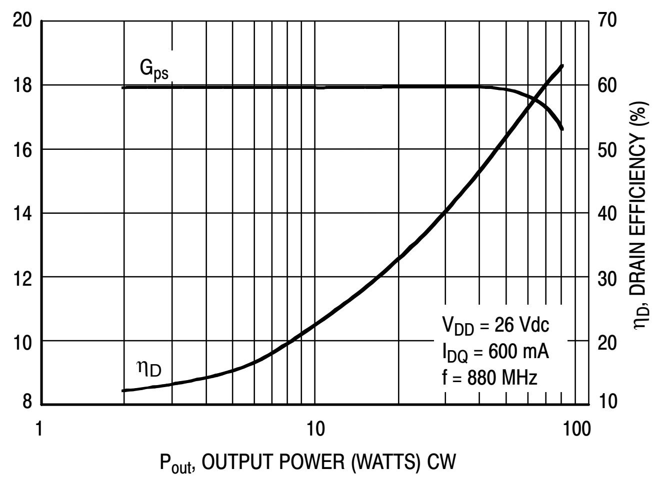
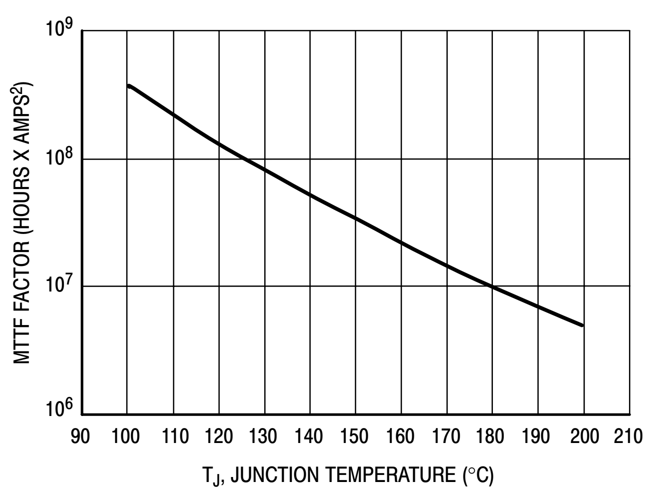


Figure 10. Power Gain and Drain Efficiency versus CW Output Power



This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 11. MTTF Factor versus Junction Temperature

N-CDMA TEST SIGNAL

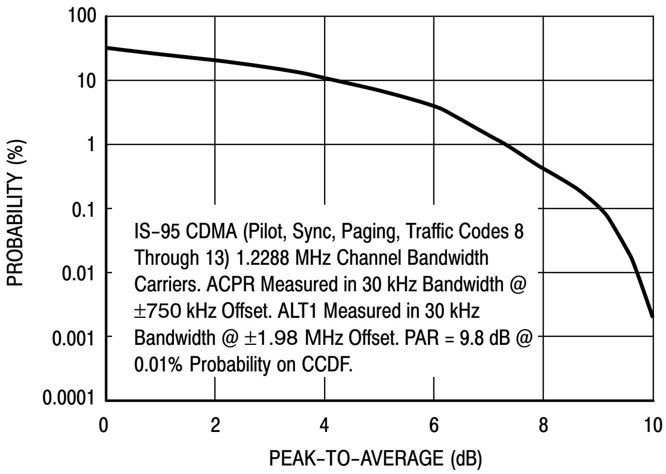


Figure 12. Single-Carrier CCDF N-CDMA

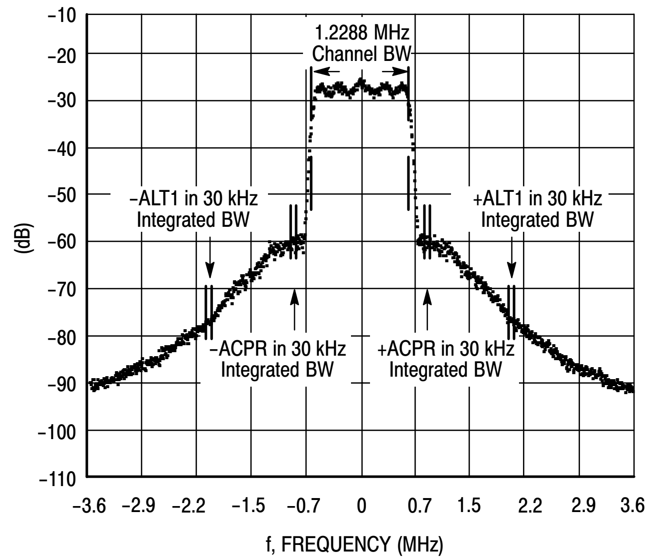
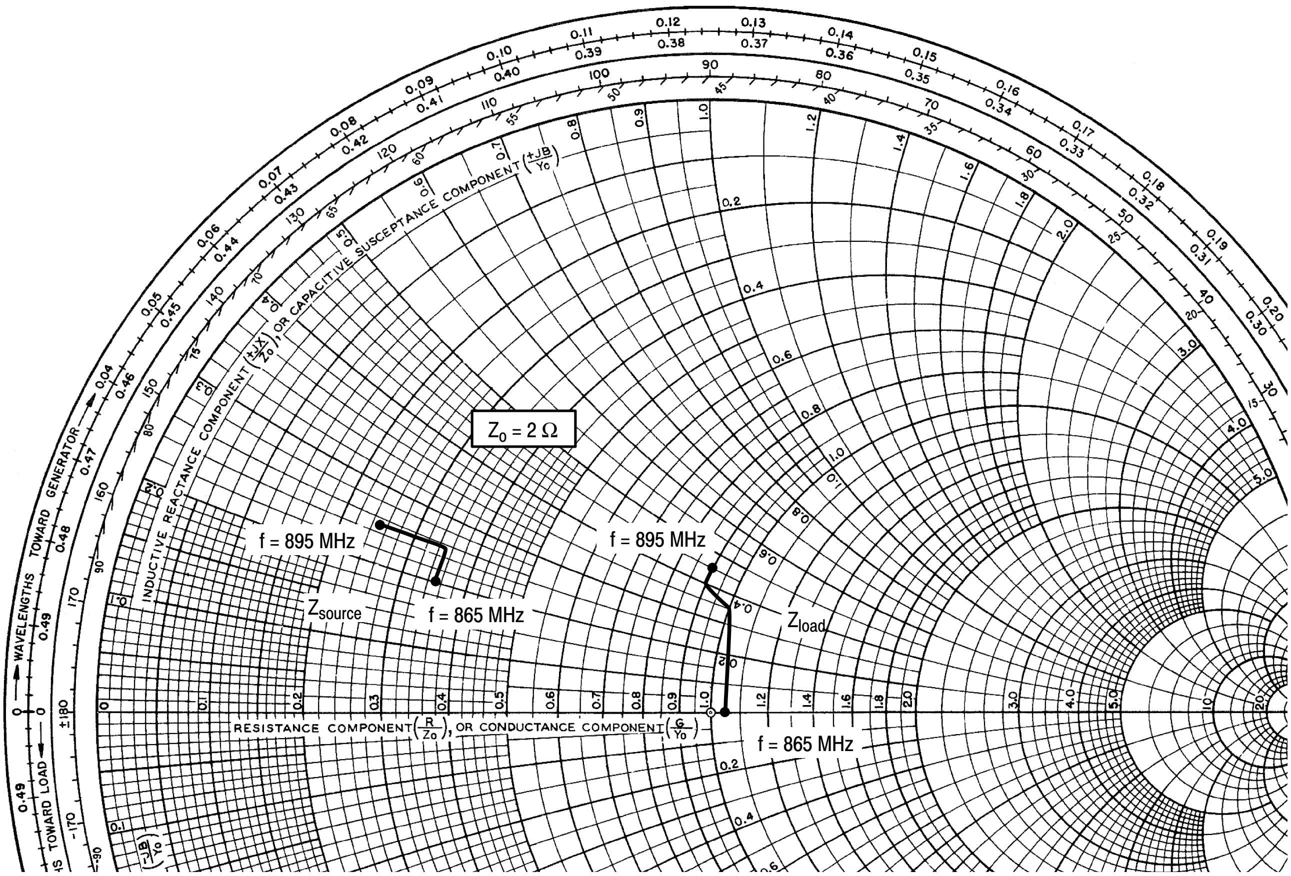


Figure 13. Single-Carrier N-CDMA Spectrum



V_{DD} = 26 Vdc, I_{DQ} = 600 mA, P_{out} = 14 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
865	0.7 + j0.4	2.1 + j0.6
875	0.7 + j0.5	2.0 + j0.7
885	0.6 + j0.5	1.8 + j0.8
895	0.5 + j0.5	1.8 + j0.9

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

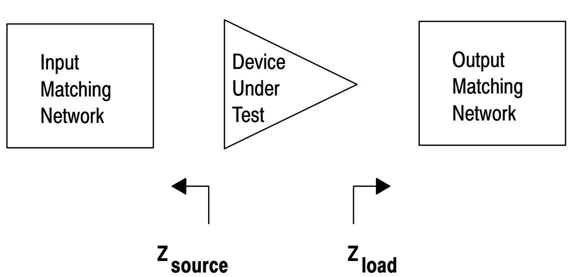
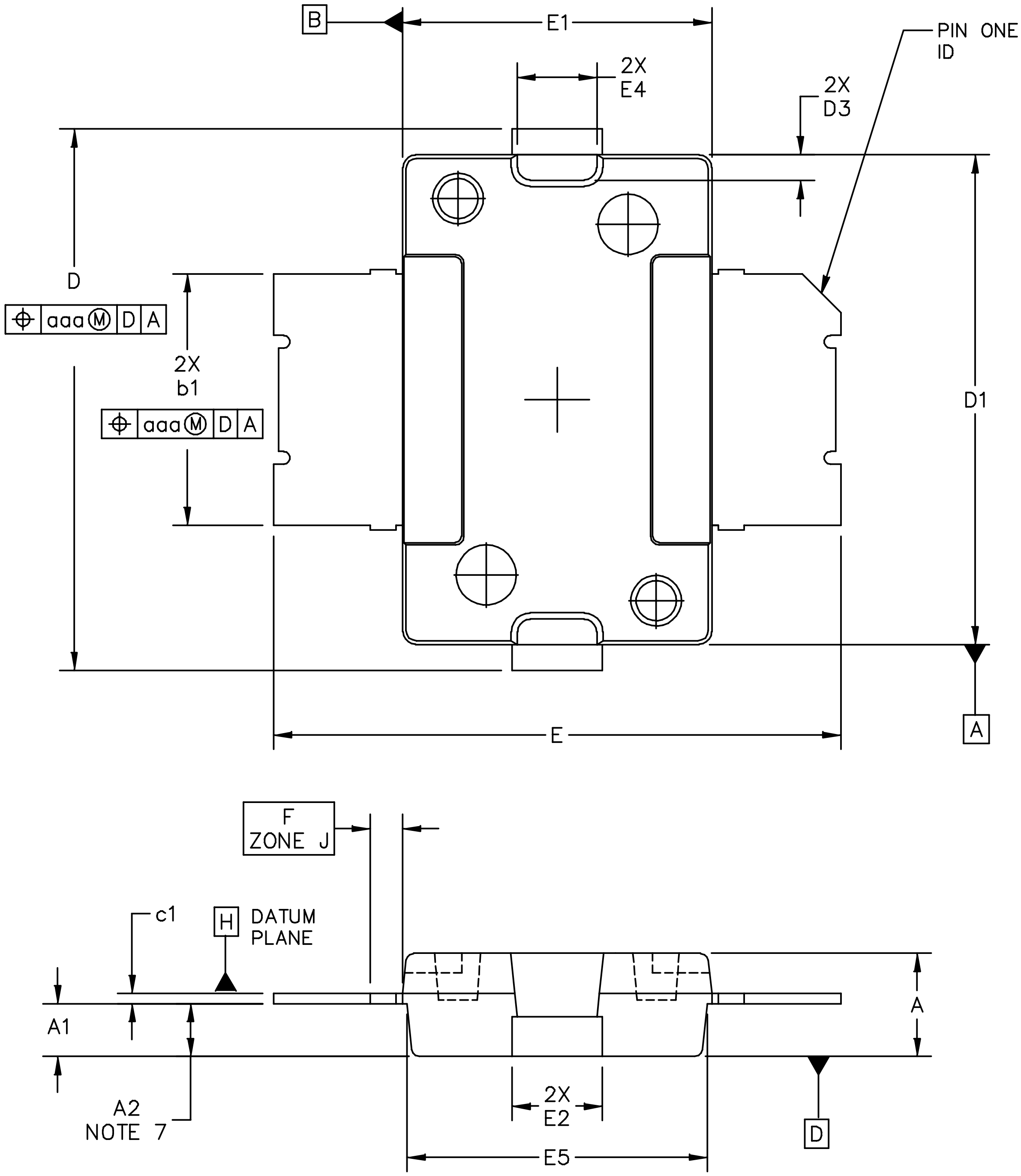


Figure 14. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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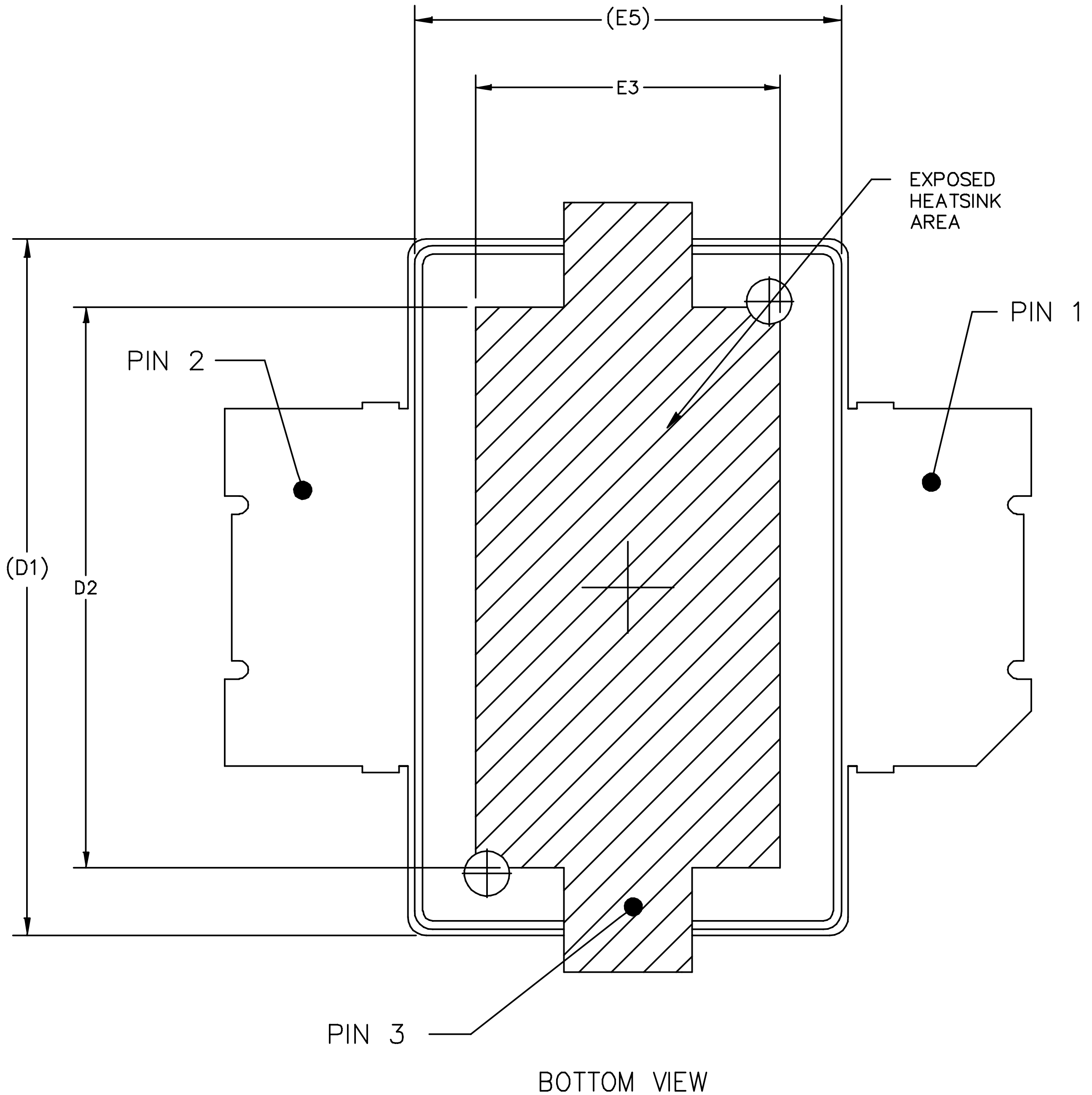
	CASE NUMBER: 1265–09		29 JUN 2007
	STANDARD: JEDEC TO–270 AA		



	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO–270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K
	CASE NUMBER: 1265–09	29 JUN 2007
	STANDARD: JEDEC TO–270 AA	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DATUM PLANE −H− IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1 AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.

7. DIMENSION "A2" APPLIES WITHIN ZONE "J" ONLY.

8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. OVERALL LENGTH INCLUDING MOLD PROTRUSION SHOULD NOT EXCEED 0.430 INCH FOR DIMENSION "D" AND 0.080 INCH FOR DIMENSION "E2". DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −D−.

STYLE 1:
PIN 1 − DRAIN
PIN 2 − GATE
PIN 3 − SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.193	.199	4.90	5.06
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.416	.424	10.57	10.77	aaa	.004		0.10	
D1	.378	.382	9.60	9.70					
D2	.290	----	7.37	----					
D3	.016	.024	0.41	0.61					
E	.436	.444	11.07	11.28					
E1	.238	.242	6.04	6.15					
E2	.066	.074	1.68	1.88					
E3	.150	----	3.81	----					
E4	.058	.066	1.47	1.68					
E5	.231	.235	5.87	5.97					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO−270 SURFACE MOUNT	DOCUMENT NO: 98ASH98117A	REV: K
	CASE NUMBER: 1265−09	29 JUN 2007
	STANDARD: JEDEC TO−270 AA	

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
7	June 2009	• Replaced Case Outline 1265-08 with 1265-09, Issue K, p. 1, 10-12. Corrected cross hatch pattern in bottom view and changed its dimensions (D2 and E3) to minimum value on source contact (D2 changed from Min-Max .290-.320 to .290 Min; E3 changed from Min-Max .150-.180 to .150 Min). Added JEDEC Standard Package Number. • Modified data sheet to reflect MSL rating change from 1 to 3 as a result of the standardization of packing process as described in Product and Process Change Notification number, PCN13516, p. 1 • Updated Part Numbers in Table 6, Component Designations and Values, to RoHS compliant part numbers, p. 4 • Added AN3789, Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages to Product Documentation, Application Notes, p. 13 • Added Electromigration MTTF Calculator and RF High Power Model availability to Product Software, p. 13

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For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

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