nRF7002

Objective Product Specification

v0.7.0

NORDIC® SEMICONDUCTOR

nRF7002 features

Key features	Applications

• Wi-Fi 6 companion IC with integrated RF
• Supports IEEE 802.11 ax and earlier standards (IEEE 802.11 a/b/g/n/ac)
• Supports Target Wake Time (TWT), Orthogonal Frequency Division Multiple Access (OFDMA), BSS Coloring
• Supports Wi-Fi CERTIFIED 6™, Wi-Fi CERTIFIED™, Wi-Fi Enhanced Open™
• Supports WPA3™, WPA2™, WPA™ - Personal and Enterprise, Protected Management Frames
• Supports WMM®, WMM - Power Save, Wi-Fi Agile Multiband™, Wi-Fi Direct®
• Maximum output power 21 dBm
• Dual-band 2.4 GHz and 5 GHz operation
• Single-ended 50 Ω antenna port(s)
• 191 mA @ max output power, 2.4 GHz, MCS7 ; 260 mA @ max output power, 5 GHz, MCS7
• 60 mA RX 2.4 GHz, 56 mA RX 5 GHz
• SPI or QSPI host interface, 3-wire or 4-wire coexistence interface
• Supply voltage range 2.9 – 4.5 V
• Operating temperature range -40° C to 85° C
• 6x6 mm QFN48 package
	• Internet of Things (IoT)
	  • Smart Home applications, including Gateways and Border Routers
	  • Industrial IoT sensors and controllers
	• Sports and Fitness
	• Wireless Payment Terminals
	• Medical

Contents

1 Revision history

Date	Version	Description
December 2022	0.7.0	First release

2 Product overview

nRF7002 is a wireless companion IC that adds low-power Wi-Fi 6 capabilities to another System on Chip (SoC), Microprocessor Unit (MPU), or Microcontroller (MCU) host. It implements the Physical (PHY) and Medium Access Controller (MAC) layers of the 802.11 protocol stack, while the higher layers of the networking stack run on the host.

nRF7002 is compatible with IEEE 802.11ax (also known as Wi-Fi 6) and with earlier standards IEEE 802.11a/b/g/n/ac.

nRF7002 has been designed for Internet of Things (IoT) applications, and is ideal for adding modern Wi-Fi 6 capabilities to existing *Bluetooth*® Low Energy/Thread®/Zigbee® systems.

Nordic Semiconductor provides reference host support implementations for the nRF52840 and nRF5340, but nRF7002 may also be used with other hosts with sufficient processing and memory capacity. It connects to the host SoC/MCU through a SPI or QSPI serial interface (which can optionally be encrypted) and supports co-existence with other radio protocols through a dedicated 3-wire or 4-wire coexistence interface.

nRF7002 supports dual-band 2.4 GHz and 5 GHz band operation. The antenna ports are single-ended 50 Ω.

nRF7002 supports 20 MHz wide channels, 1x1 (SISO) operation and can deliver a PHY data rate of 86 Mbps (MCS7). It supports Station and Wi-Fi Direct operation modes as well as Soft AP (Wi-Fi 4 operation only) and simultaneous Station + Soft AP/Wi-Fi Direct/Station modes.

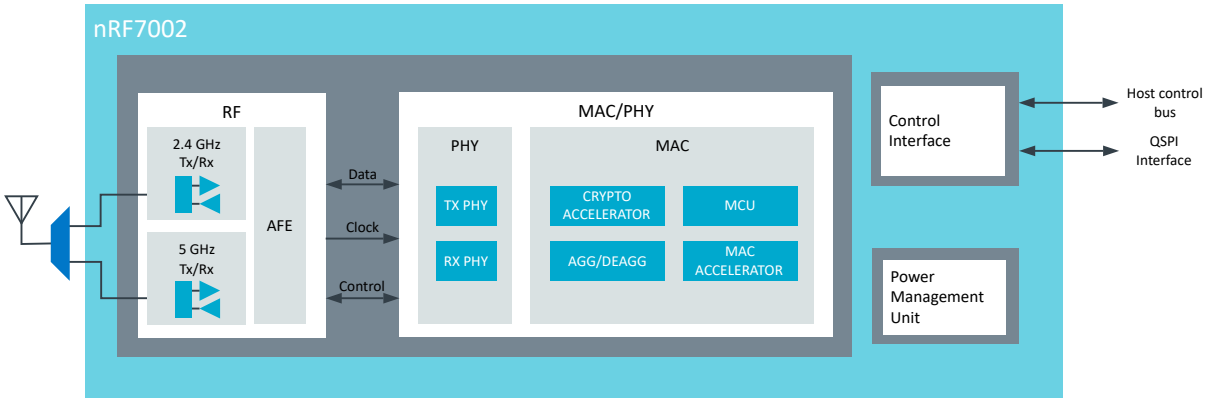


Figure 1: nRF7002 block diagram

3 Functional description

This section describes nRF7002 modules and peripherals.

3.1 Host connection

nRF7002 is a wireless companion device that is connected to a host MCU/application processor. nRF7002 is connected to the host through a QSPI (6-wire) or SPI (4-wire) interface for data and a 3-wire or 4-wire coexistence control interface for hosts that include a radio. In addition, 2 lines (HOST_IRQ and BUCKEN) are required. The user application executes on the host MCU.

The following figure shows a system with nRF7002 and a host MCU.

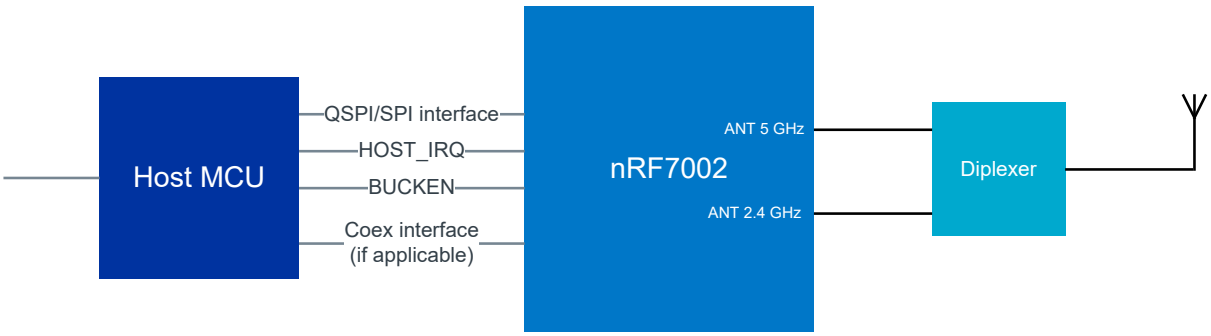


Figure 2: Functional block diagram with generic host MCU

nRF7002 is designed to support radio coexistence and can be used together with another nRF Series device. The following figure shows nRF7002 together with nRF5340 to achieve a combined Bluetooth Low Energy and Wi-Fi® solution. nRF5340 functions as a host and a common interface to the wireless system.

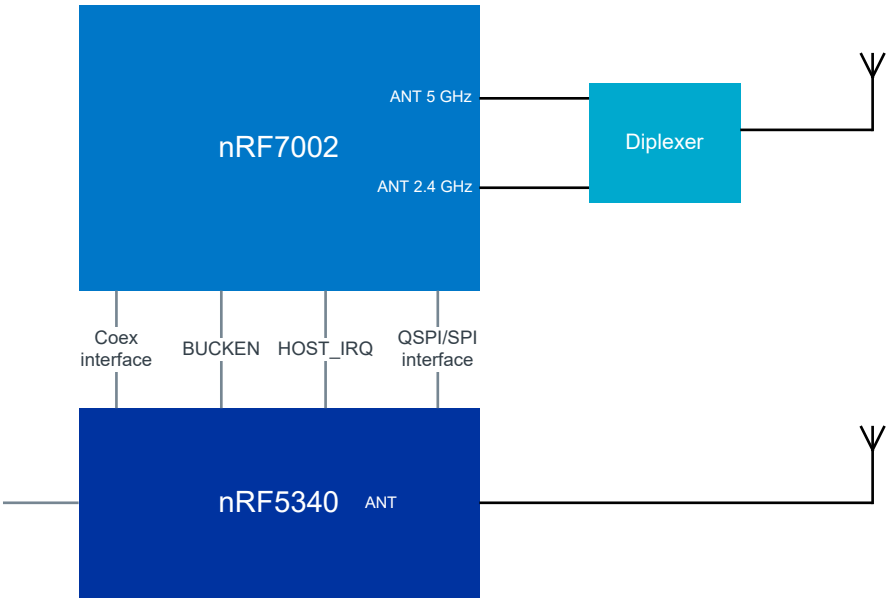


Figure 3: Functional block diagram with nRF host and dual antennas

Using a dual antenna configuration enables simultaneous operation for Wi-Fi and 2.4 GHz short-range radio. For cost or area-sensitive applications that do not need simultaneous operation, a single antenna

configuration is also possible. This requires an antenna switch, which can be controlled from the radio coexistence algorithm.

The following figure shows single antenna operation with nRF7002.

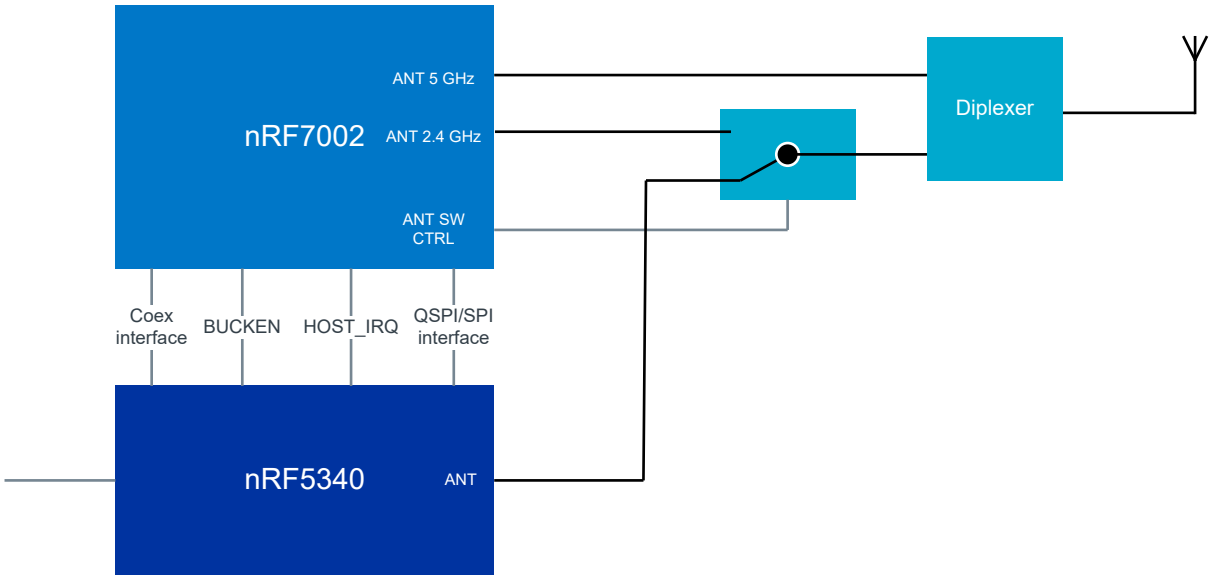


Figure 4: Functional block diagram of nRF7002 with nRF host and single antenna

Note: Introducing a switch in the signal path may give a loss in sensitivity (typically <1dBm) compared to using dual antenna.

3.2 Power and clock management

3.2.1 Power states

nRF7002 has three power states: Shutdown, Sleep, and Active.

Shutdown

The fully inactive state where no state information is retained except for the contents of OTP. nRF7002 will only respond to a BUCKEN assertion (input to PMU).

- PMU: Off
- Analog circuits: All circuits off
- Baseband logic and scratch RAMs: Off
- Retention RAMs: Off
- SPI/QSPI: Off

Sleep

A low-power state where state information is retained and transitioning to Active state can occur rapidly. The device may be in the sleep state during both pre-association (device idle waiting for host command) and post-association period as part of the Wi-Fi powersave mode (that is, maintain association with an Access Point but without data traffic). In this state, the device is clocked via the internal 32 kHz RC oscillator (RTC), and can be awakened via the host interface or the internal sleep timer expiry.

- PMU: Low-power mode (PFM)
- Analog circuits: RTC active, register state retained. All other circuits are powered down.

- Baseband logic and scratch RAMs: Off
- Retention RAMs: Retained
- SPI/QSPI: On

Active

In the Active state, the device will be in one of the Active sub-states: Transmit, Receive, or Idle. The high frequency XO derived clocks are active and the appropriate RF section components are enabled as required. The Idle sub-state is a short term transitory state used when Receive is not required, but Sleep cannot be exploited (for example, upon early termination of an RX packet).

- PMU: High-power mode (PWM)
- Analog circuits: All circuits powered (including XO). The circuits are enabled according to Active sub-state (TX, RX, or IDLE)
- Baseband logic and scratch RAMs: On
- Retention RAMs: Active
- SPI/QSPI: On

3.2.2 Power state operation

Apart from transitions in/out of Shutdown via the BUCKEN pin, all transitions between Sleep and Active states are fully autonomous, and do not require any host control.

Shutdown state is achieved by de-assertion on the BUCKEN pin. Asserting BUCKEN will result in the Active (IDLE sub-state) state being entered. The host will initiate the boot sequence via SPI/QSPI, culminating in the Sleep state being entered. This is the lowest power non-Shutdown state that can be achieved. Transitions from Active to Sleep are fully controlled by nRF7002. Transitions from Sleep to Active are controlled by both the host and nRF7002. In a pre-association condition, Sleep will be entered opportunistically whenever there is no activity initiated from the host (for example, a scan request). In a post-association condition, Sleep opportunities will be determined by the negotiated powersave mode of the Access Point. No host interactions are required to enter Sleep, while the host will force a transition from Sleep to Active as part of any SPI/QSPI command transaction.

The steps involved in transitioning from Shutdown or Sleep into Active are as follows:

- Switch PMU into high power mode (PWM)
- Apply power to digital logic, RAMs and analogue circuits
- Start 40 MHz XO (and allow to settle)
- Start baseband PLL (and allow to settle)
- Boot all processor cores
- Execute baseband initialisations
- Execute RF initialisations and calibrations

The initial steps consume equal duration whether originating in Shutdown or Sleep, while the baseband and RF initialisations are very dependent on the originating state. In particular:

- Full baseband initialisations are required from Shutdown (including transferring the FICR information from OTP into retention RAM), while in Sleep some of the state is retained in retention RAMs.
- Complete RF calibrations are required from Shutdown, including across bands/channels in order to support scanning. From Sleep, only minimal initialisation/calibration on just the operating channel is required.

See Electrical Specification chapter for timing information.

3.2.3 Clock accuracy considerations

The XO is active during normal operation, and is the clock reference for the RF synthesizer, the ADC/DAC sample clocks, and the baseband logic. The RTC is active during sleep state, and is used to run the wakeup timer used as part of Wi-Fi powersave. The XO is inactive during sleep.

The IEEE802.11 specification defines the accuracy of the Wi-Fi carrier frequency to be within ± 20 ppm (in 5 GHz), which in turn defines the required accuracy of the external crystal (XTAL). There is provision to trim the XO via a value programmed into the OTP on the nRF7002 device (or any other available non-volatile memory). This trimming will compensate for the combined frequency offset resulting from the XTAL itself as well as any XO variation at room temperature. The XTAL and XO will both exhibit frequency drift across temperature, and the XTAL will also be subject to aging. The combination of these temperature and aging effects, along with the trimming accuracy, will consume the majority of the ± 20 ppm allowance, assuming a XTAL with ± 10 ppm stability over temperature. The XTAL tolerance (that is, accuracy at room temperature) is less important since this will be trimmed out by the XO trim function (up to ± 20 ppm). The XO/XTAL is typically trimmed by transmitting Wi-Fi packets via the antenna connector and using a Vector Spectrum Analyser (VSA) to measure the frequency offset. Alternatively, a generic spectrum analyser can be used to measure the frequency offset on a transmitted carrier wave (CW).

The RTC is automatically calibrated against the trimmed 40 MHz XO reference at runtime, and as such nothing needs to be done on the production line. During sleep, the RTC clocked wakeup timer is used to time wakeup intervals (since the last DTIM beacon in regular Wi-Fi powersave), and as such any residual inaccuracy is not accumulated.

3.3 Software stack

This section details the partitioning of the TCP/IP networking stack and the IEEE802.11 Wi-Fi stack across the host MCU and the nRF7002 chip. This description is based around the Zephyr™ TCP/IP networking stack and an nRF5340 host MCU, however the partitioning would apply equally to other operating systems and host MCUs supporting a compatible SPI/QSPI interface.

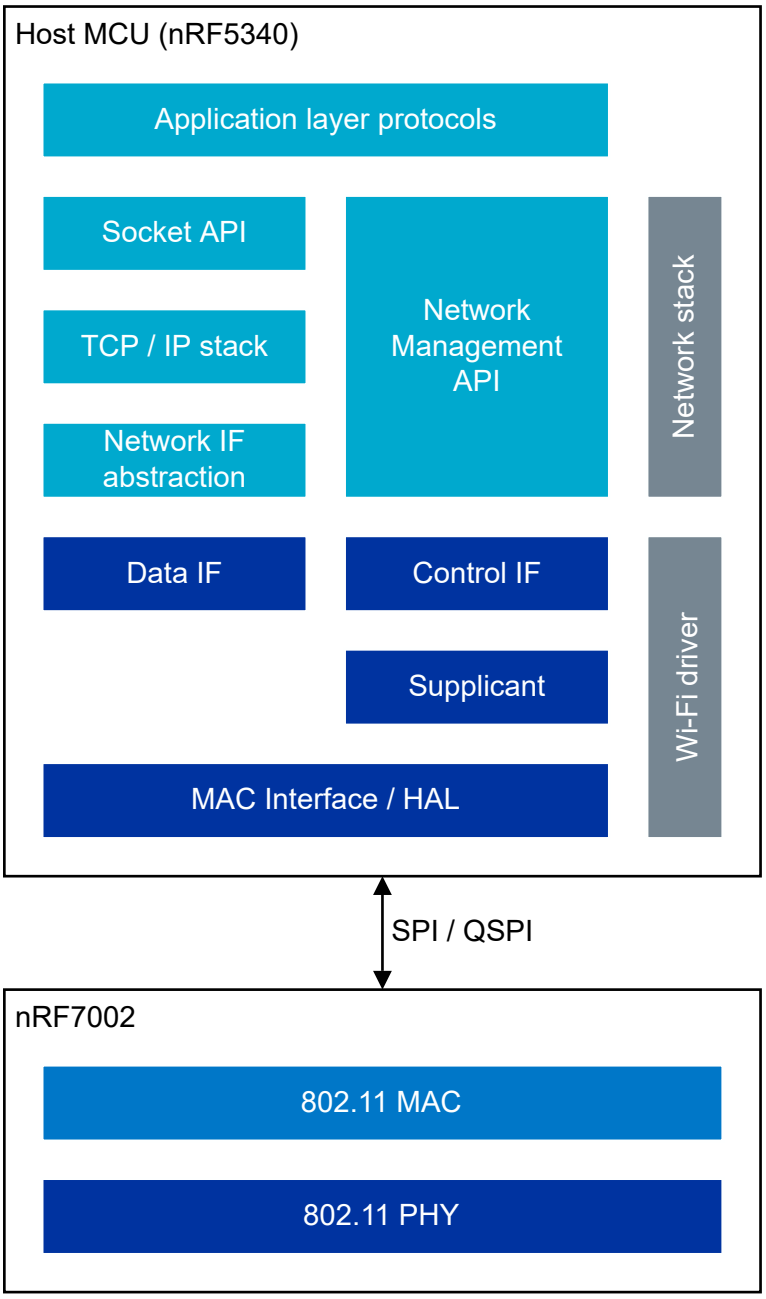


Figure 5: Network stack architecture

The TCP/IP networking stack and Wi-Fi driver execute on the host MCU (for example, nRF5340) and communicate with the MAC layer on the nRF7002 via SPI / QSPI. The Wi-Fi driver presents control and data interfaces (Control IF/Data IF) to the TCP/IP networking stack.

Control IF

The Control IF interfaces with the Network Management API (net_mgmt). Functionality such as scanning, connecting to a SSID, or setting the encryption key is implemented in the Control IF.

Data IF

The Data IF interfaces with the L2 Network Technologies layer of the TCP/IP networking stack. The Wi-Fi driver presents the nRF7002 as an Ethernet device to the data path of the TCP/IP networking stack. In the TX path, it receives Ethernet frames from the upper layers and in the RX path sends Ethernet frames to it. The Wi-Fi driver takes care of converting Wi-Fi frames to Ethernet frames in the RX path.

Supplicant

The supplicant is implemented as part of the Wi-Fi driver and provides the following functionality:

- 802.11 authentication and association
  - The supplicant requests the driver to scan neighbouring BSSes and then requests the driver to associate with a chosen BSS. 802.11 authentication is the first step in network attachment. 802.11 authentication requires a station (STA) to establish its identity with an Access Point (AP). No data encryption or security is available at this stage.
- Wi-Fi Protected Access®(WPA) authentication
  - The supplicant implements the authentication services and port control described in the IEEE802.1X standard.
  - The initial authentication process is carried out either using a
    - Pre-shared key (PSK), or
    - Following an EAP exchange through 802.1X (known as EAPOL, which requires the presence of an authentication server).
  - This process ensures that the client station (STA) is authenticated with the access point (AP).
  - This also results in the generation of a shared Pairwise Master Key (PMK) at both the station and the AP.
- 4-way handshake
  - The 4-way handshake is designed such that the STA and AP can prove to each other their knowledge of the PMK without actually disclosing the key.
  - The 4-way handshake generates the following:
    - Pairwise Transient Key (PTK): This is used to protect unicast data.
    - Group Temporal Key (GTK): This is used to protect multicast and broadcast data
- Roaming
  - When connected to a wireless network with multiple access points, the supplicant is typically responsible for implementing the roaming between access points. The supplicant detects a closer access point (BSSID) in the current network (SSID), in terms of signal strength (RSSI), it will re-associate to the closer access point.
- SoftAP
  - A software access point (SoftAP), enables a device to turn its wireless interface into a Wi-Fi access point.
  - In SoftAP mode the supplicant takes care of station onboarding and management
  - The SoftAP support is limited to PSK (WPA Personal) security.
- P2P
  - The supplicant implements the higher layer functionality for managing P2P groups and takes care of
    - Device Discovery
    - Service Discovery
    - Group Owner Negotiation
    - P2P Invitation.
  - In addition, it maintains information about neighbouring P2P Devices.

3.3.1 Firmware updates

nRF7002 supports device firmware updates for bug fixes, security fixes, or additional functionality.

The updates are performed by patching the firmware. The firmware patches are downloaded from the host to the device for patching the ROM-based firmware. The patch download is fully automatic and handled by the Wi-Fi driver software running on the host device.

Patches are downloaded to the nRF7002 device when powering up the device. Patches are downloaded into the patch memory, which is retained during sleep. The maximum patch size is 128 KB.

Patches are linked to a Wi-Fi driver version and delivered as a binary blob as part of the Wi-Fi driver.

3.4 Quad Serial Peripheral Interface (QSPI) slave

The QSPI slave interface is compatible with the nRF52 and nRF53 Series Quad Serial Peripheral Interface (QSPI) master and Serial Peripheral Interface Master (SPIM).

The main features of the QSPI slave interface are:

- Single/quad SPI input/output
- Supports up to 32 MHz clock frequency
- Single and block mode read/write accesses
- On-the-fly encryption and decryption

3.4.1 QSPI command description

Command (byte)	RDSR (read status register 0)	RDSR1 (read status register 1)	RDSR2 (read status register 2)	WRSR2 (write status register 2)	CIPHER INIT (Initialize cipher)	FAST READ (fast read data)	READ4 (4 x I/O read command)	PP (Page program)	PP4 (Quad page program)
1st byte	05 (hex)	1F (hex)	2F (hex)	3F (hex)	4F (hex)	0B (hex)	EB (hex)	02 (hex)	38 (hex)
2nd byte					NONCE1	AD1	ADD (4) and Dummy (4)	AD1	ADD (4)
3rd byte					NONCE2	AD2	Dummy (4)	AD2	
4th byte					NONCE3	AD3		AD3	
5th byte					NONCE4	Dummy			
Action	To read out the values of status register 0	To read out the values of status register 1	To read out the values of status register 2	To write in the values of status register 2	To enable the steam cipher and initialize the NONCE register	n bytes read out until SS goes high	n bytes read out by 4 x I/O until SS goes high	to program the selected page	Quad input to program the selected page

Table 1: QSPI commands

Note:

- For RDSR, RDSR1, RDSR2, FAST_READ and READ4, the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the SS can be high.
- For CIPHER_INIT, PP and PP4, the SS must go high exactly at the 4th byte (32bits) boundary or the value will not be stored.
- For WRSR2 the SS must go high exactly at the 1st byte (8 bits) boundary;otherwise, the value will not be stored.

3.4.2 Stream cipher

The data transactions between the master and the slave can be protected using stream cipher encryption. Encryption can be configured and enabled with the CIPHER_INIT command.

The following figure shows the stream cipher block with the configuration inputs. The stream cipher uses an AES 128 encryption operation to form the keystream from key, nonce, and external memory address. The keystream then combines each 32-bit plaintext digit one at a time with the corresponding digit of the keystream.

The same nonce and key must be used for both encryption and decryption of the same memory address. Stream ciphers are symmetric. They do not differentiate between encrypting or decrypting, reading or writing.

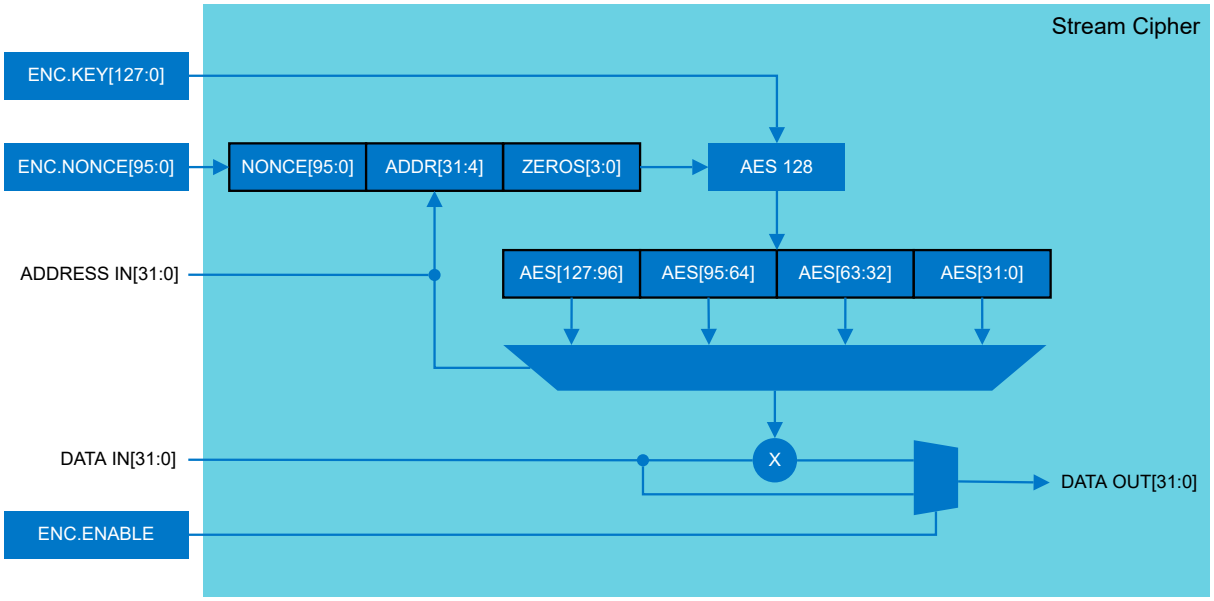


Figure 6: Stream cipher

Stream cipher	Value
ENC.KEY [127:0]	{CIPHER_KEY3[31:0], CIPHER_KEY2[31:0], CIPHER_KEY1[31:0], CIPHER_KEY0[31:0]}
ENC.NONCE [95:0]	{NONCE_CNT[31:0], NONCE_CFG[31:0], CIPHER_NONCE0[31:0]}
ADRESS IN [31:0]	{8'h00, SPI Address [23:0]}
ENC.ENABLE	CIPHER ENABLE

Notes:

- CIPHER_KEY3, CIPHER_KEY2, CIPHER_KEY1, CIPHER_KEY0, CIPHER_NONCE0 : IP parameters (32 bit).
- NONCE_CFG : The NONCE Configuration register. Initialized with the CIPHER_INIT command.
- NONCE_CNT: The NONCE Counter register. Initialized to d0 with the CIPHER_INIT command. A pre-increment is done to the NONCE_CNT register at the start of the QSPI transaction (FAST_READ, READ4, PP, PP4).
  - Single read/write mode : increment always.
  - Multiple read/write mode : increment only if the received SPI address differs from the next expected SPI address (last SPI address +1) or if the last transaction was not in multiple mode.
- CIPHER ENABLE : The Cipher Enable register is 1'b0 by default and it is set to 1'b1 with the CIPHER_INIT command.

Table 2: Stream cipher configuration

3.4.3 QSPI throughput

The table below details the expected peak achievable UDP/TCP throughput numbers for a QSPI/SPIM clock rate of 24 MHz, and where the networking stack executing on the host is not a limiting factor. These numbers are projected using measured raw QSPI/SPIM packet transmission rates.

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$t_{UDP,TX,QSPI}$	Max UDP TX mode throughput over QSPI			56	Mbps	
$t_{UDP,RX,QSPI}$	Max UDP RX mode throughput over QSPI			61	Mbps	
$t_{UDP,TX,SPIM}$	Max UDP TX mode throughput over SPIM			14	Mbps	
$t_{UDP,RX,SPIM}$	Max UDP RX mode throughput over SPIM			14	Mbps	
$t_{TCP,TX,QSPI}$	Max TCP TX mode throughput over QSPI			40	Mbps	
$t_{TCP,RX,QSPI}$	Max TCP RX mode throughput over QSPI			42	Mbps	
$t_{TCP,TX,SPIM}$	Max TCP TX mode throughput over SPIM			12	Mbps	
$t_{TCP,RX,SPIM}$	Max TCP RX mode throughput over SPIM			12	Mbps	

Table 3: UDP/TCP throughputs

3.5 Coexistence

nRF7002 has a highly configurable coexistence hardware (CH) to help mitigate interference between WLAN and Short Range (SR) devices (Bluetooth Low Energy, Thread, Zigbee).

A Packet Traffic Arbiter (PTA), connected to the CH logic function, facilitates the mitigation of various interference scenarios through a highly-programmable fabric. CH enables flexible output signals that support interface configurations like 3-wire and 4-wire. The primary schemes supported are:

- *Shared antenna mode* – The PTA makes priority decisions, controls the external SR/Wi-Fi switch, and grants external SR device TX/RX requests. Only one radio interface (SR or Wi-Fi) is connected to the antenna at any point of time.
- *Separate antenna mode* – The PTA makes priority decisions and grants external SR device TX/RX requests. Both radio interfaces are permanently connected to the antennas.

The following diagram shows the CH architecture including details about the PTA control lines.

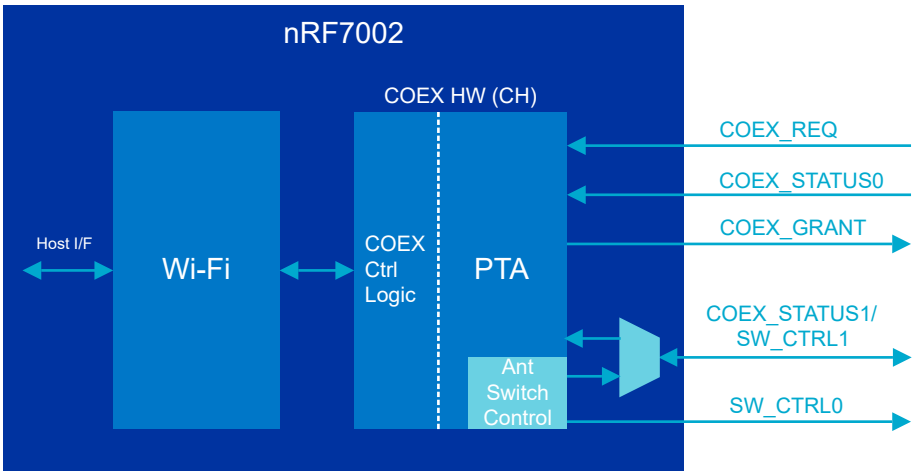


Figure 7: CH architecture

Signal name	I/O	Mandatory/ Optional	SR Signal (3-wire/4-wire)	Description
COEX_REQ	Input	Mandatory for 3-wire and 4-wire	SR_REQUEST	SR device requesting a TX/RX transaction
COEX_STATUS0	Input	Mandatory for 3-wire and 4-wire	SR_STATUS	Indicates if the SR transaction is TX or RX. If the SR device supports a Priority signal, Priority is muxed with TX/RX on this signal based on the timing diagrams.
COEX_GRANT	Output	Mandatory for 3-wire and 4-wire	SR_GRANT	Indicates that the SR device is granted access for this transaction.
COEX_STATUS1/ SW_CTRL1	Input/ Output	Optional for 3-wire	SR_PTI/ RF_SW_CTRL1	In 4-wire mode, this carries the SR 1 bit priority signal. In 3-wire shared antenna mode, this can be optionally used as antenna switch control.
SW_CTRL0	Output	Mandatory for 3-wire and 4-wire shared antenna mode. Optional otherwise	RF_SW_CTRL0	Used for antenna switch control in shared antenna mode.

Table 4: CH signals

Note: SW_CTRL0/1 are fully programmable and can be configured based on the COEX mode selected and the antenna switch used for the shared antenna case.

3.5.1 SR timing

3-wire with multiplexed priority

The following diagram shows external SR timing parameters when SR_STATUS carries both priority and TX/RX information in a time multiplexed manner.

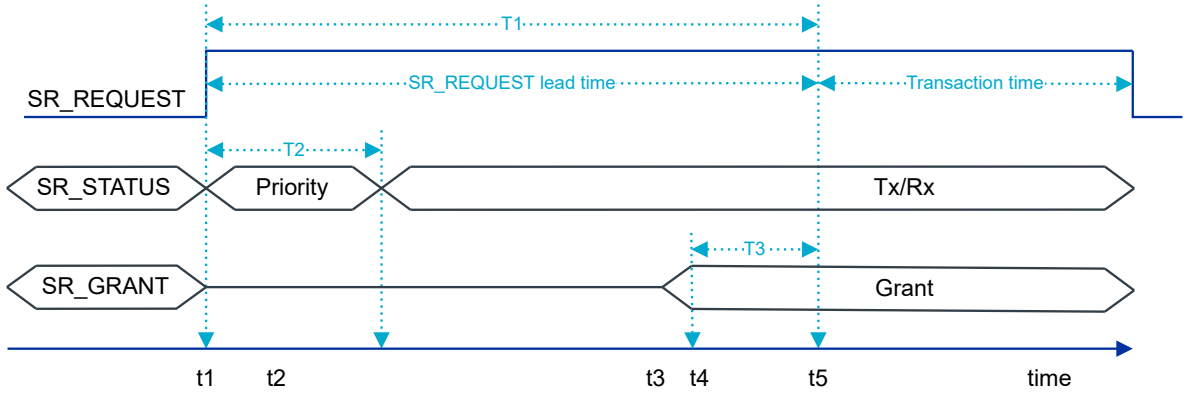


Figure 8: 3-wire timing with priority multiplexing

Parameter	Description
T1: SR_REQUEST lead time period	The time SR_REQUEST is asserted before actual transactions.
T2: SR_STATUS	The time when SR_STATUS is sampled to get SR_PTI information.
T3: SR_GRANT	The time before PTA should post SR_GRANT so that it is stable to be considered by SR.

Table 5: SR timing parameters

These SR timing parameters are used to derive PTA timing parameters and the following table describes the relationship between PTA timing parameters and SR timing parameters.

PTA timing parameter	Relation with SR timing parameter
SR status priority sampling time (t2)	t1 < t2 < (t1+T2)
PTA arbitration decision time (t3)	(t1+T2) < t3 < (T1-T3)

Table 6: PTA and SR timing parameters

Time instance	Description
t1	The time instance when SR_REQUEST is asserted.
t2	The time instance when SR_STATUS is sampled to get SR_PTI information. This can be any time during T2.
t3	The time instance when PTA takes an arbitration decision and posts SR_GRANT to SR. This is chosen a couple of microseconds before the start of the *SR grant lead time period*. This ensures that SR_GRANT is asserted as close to *SR grant lead time period* and is stable by the time SR uses this information to continue or abort the transaction.
t4	The time instance when the *SR grant lead time period* starts. This is the time when SR_GRANT must be stable to be considered by SR.
t5	The time instance when the actual transaction of SR starts. This is the time when the signaling period ends and the transaction period starts. SR Tx and Rx information is provided by changing the SR_STATUS signal level appropriately. PTA should track SR_STATUS if SR_REQUEST is high and update the information SR_TX_RX.

Table 7: Time instances

3-wire without multiplexed priority

If SR_STATUS carries only one parameter information (3-wire, no priority mode), then the default information that it carries is SR_TX_RX. In this case, SR_STATUS is set to TX or RX when SR_REQUEST is HIGH. The following diagram shows SR_STATUS only carrying TX/RX information. The signals are represented as a bus even thought they are single bit ports to indicate transitions happening on the ports.

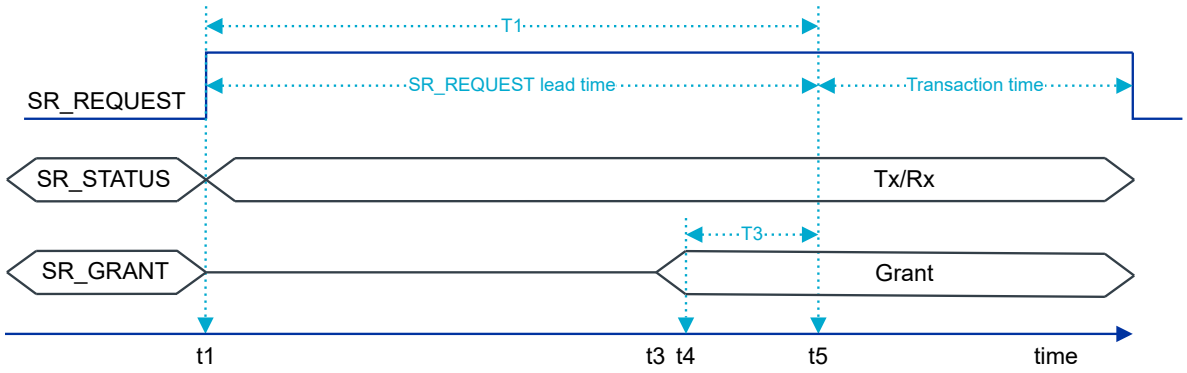


Figure 9: 3-wire timing without priority multiplexing

During the transaction, SR changes SR_STATUS appropriately to indicate TX and RX information. PTA continuously tracks SR_STATUS while SR_REQUEST is high and updates SR_TX_RX status internally for corresponding COEX behavior.

4-wire timing

In the following diagram, SR priority is explicitly signaled on the BT_COEX_STATUS1 pin.

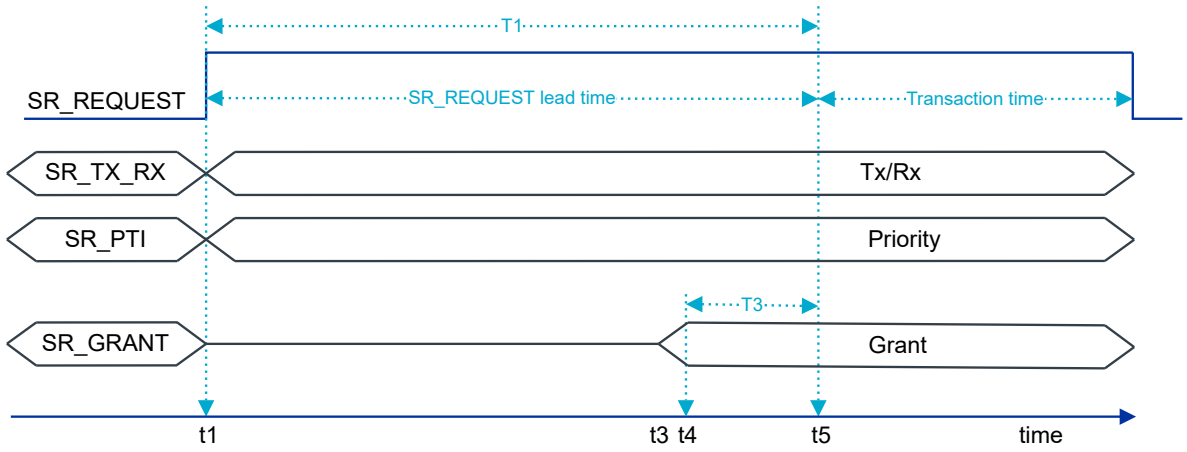


Figure 10: 4-wire timing

3.6 OTP Programming

nRF7002 includes a 128 x 32-bit OTP memory. This memory is partitioned into two regions, a factory programmed region and a customer programmed region, each containing 64 x 32-bit locations.

The factory programmed region contains information related to production and trim values. The customer programmed region contains:

- Encryption key used to protect the QSPI traffic (4 words)
- MAC addresses for VIF0 and VIF1 (4 words)
- Module level calibration coefficients (9 words)
- OTP protection control (4 words)
- Uncommitted region (43 words)

QSPI encryption is optional. This is enabled at runtime via a QSPI command. If this feature is not required, the OTP locations can remain unprogrammed. For security reasons, the encryption key cannot be read once programmed.

The MAC address fields in OTP are accessed by firmware when powering up the device, and presented to the host via a (Q)SPI based event as part of the boot phase. The host driver is responsible for configuring the MAC addresses as part of device configuration. As such, the MAC addresses stored in OTP can be overwritten by the host. Using this mechanism, the MAC addresses in OTP can remain unprogrammed if an alternate host side storage is utilised.

Module level calibration coefficients can be calculated and stored in OTP to enhance some performance characteristics. The use of these are optional, but typically at least the XO trim value will be needed. The procedure for determining these calibration coefficients is beyond the scope of this document.

Although the OTP memory is *one time programmable*, in reality any bit still in a `1` state can be re-programmed into a `0` state. In order to avoid deliberate or inadvertent modification of OTP data, a protection mechanism is provided. The protection registers initially need to be programmed to 0x50FA50FA in order to activate programming of the remaining locations. Once OTP programming is complete, the protection registers should be programmed to 0x00000000, at which point the OTP can never be modified.

In addition to the logical protection mechanism described above, a programming voltage needs to be applied to the OTPVDD pin in order to enable programming. The programming voltage is 2.5 V, while for reads it is 1.8 V. In order to coordinate the OTPVDD supply voltage with read and write operations, it is recommended to drive this supply from the POWERIOVDD output pin on nRF7002. This also ensures there will be no leakage associated with the OTP across sleep cycles, where the digital supply rail is removed.

The OTP memory is indirectly mapped, and as such read and writes are achieved using address, data, and mode registers. The OTP programming utility implements this programming, along with appropriate control of the OTPVDD supply through the POWERIOVDD output.

4 FICR - Factory Information Configuration Registers

The Factory Information Configuration Registers (FICR) are stored in One Time Programmable (OTP) memory.

FICR consists of two regions: a factory programmed region that contains device information and a customer programmable region that contains empty registers for the customer to write data to. The factory programmable region consists of the INFO group registers, while the customer programmable region consists of the QSPI, MAC, and CALIB group registers.

Access to the customer programmable region is controlled using the PROTECTION register.

The PROTECTION scenarios are:

- When PROTECTION is unprogrammed, neither read not write is enabled.
- When PROTECTION is programmed to 0x50FA50FA, full read and write access is enabled.
- When PROTECTION is programmed to 0x00000000, access protection is applied and readout of QSPI.KEY is prevented.

The following table shows the access protection for the different register groups.

Register group	0xFFFFFFFF	0x50FA50FA	0x00000000
QSPI.KEY	-	R/W	-
MAC.ADDRESS	-	R/W	R
CALIB	-	R/W	R

Table 8: PROTECTION register settings for access control to customer programmable region

4.1 Registers

Register overview

Register	Offset	Description
INFO.PART	0x0C0	Part code
INFO.VARIANT	0x0C4	Part variant
INFO.UUID[n]	0x0D0	Universal Uniqe ID
REGION.PROTECT[n]	0x100	Region protection
QSPI.KEY[n]	0x110	QSPI link symmetric encryption key
MAC[n].ADDRESS0	0x120	MAC address for VIFn
MAC[n].ADDRESS1	0x124	MAC address for VIFn
CALIB.XO	0x130	XO adjustment
CALIB.MAXPOW2G4	0x13C	Max output power
CALIB.MAXPOW5G0MCS7	0x140	Max output power for MCS7
CALIB.MAXPOW5G0MCS0	0x144	Max output power for MCS0
REGION_DEFAULTS	0x154	Customer region register usage indicator

4.1.1 INFO.PART

Address offset: 0x0C0

Part code

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	PART																																	
			N7002	0x7002																															
				nRF7002																															

4.1.2 INFO.VARIANT

Address offset: 0x0C4

Part variant

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	VARIANT																																	
				ASCII																															
			B00	0x423030																															
				B00																															

4.1.3 INFO.UUID[n] (n=0..3)

Address offset: 0x0D0 + (n × 0x4)

Universal Uniqe ID

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID				A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	R	UUID																																	
				Universal Uniqe ID																															

4.1.4 REGION.PROTECT[n] (n=0..3)

Address offset: 0x100 + (n × 0x4)

Region protection

Used to set access restrictions for FICR. Refer to description in top of chapter. All 4 registers need to be set to the same value to change protection state.

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	VALUE			Protection value
			Undefined	0xFFFFFFFF	Undefined
			Open	0x50FA50FA	Open
			Restricted	0x00000000	Restricted

4.1.5 QSPI.KEY[n] (n=0..3)

Address offset: 0x110 + (n × 0x4)

QSPI link symmetric encryption key

KEY[0] represent key bits 31:0, KEY[1] is bits 63:32, KEY[2] is bits 95:64, KEY[3] is bits 127:96

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	KEY			QSPI link symmetric encryption key

4.1.6 MAC[n].ADDRESS0 (n=0..1)

Address offset: 0x120 + (n × 0x8)

MAC address for VIFn

Most significant 4 bytes of MAC address b6:b5:b4:b3:b2:b1

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				D D D D D D D D C C C C C C C C B B B B B B B B A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	b6			6th byte (b6) of MAC address
B	R	b5			5th byte (b5) of MAC address
C	R	b4			4th byte (b4) of MAC address
D	R	b3			3rd byte (b3) of MAC address

4.1.7 MAC[n].ADDRESS1 (n=0..1)

Address offset: 0x124 + (n × 0x8)

MAC address for VIFn

Least significant 2 bytes of MAC address b6:b5:b4:b3:b2:b1

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				B B B B B B B B A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	R	b2			2nd byte (b2) of MAC address
B	R	b1			1st byte (b1) of MAC address

4.1.8 CALIB.XO

Address offset: 0x130

XO adjustment

Adjusts capacitor bank, 0 : Lowest capacitance (Highest frequency), 127 : Highest capacitance (Lowest frequency)

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID																														A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	XO																																	
				XO adjustment																															

4.1.9 CALIB.MAXPOW2G4

Address offset: 0x13C

Max output power

Unsigned byte, resolution 0.25 dBm

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID												C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	DSSS																																	
				Max output power for DSSS																															
B	RW	MCS0																																	
				Max output power for MCS0																															
C	RW	MSC7																																	
				Max output power for MSC7																															

4.1.10 CALIB.MAXPOW5G0MCS7

Address offset: 0x140

Max output power for MCS7

Unsigned byte, resolution 0.25 dBm

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID												C	C	C	C	C	C	C	C	B	B	B	B	B	B	B	B	A	A	A	A	A	A	A	A
Reset 0xFFFFFFFF				**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
ID	R/W	Field	Value ID	Value																															
A	RW	LOW																																	
				Max output power for MSC7 in low 5GHz sub-band (channels 36 - 64)																															
B	RW	MID																																	
				Max output power for MSC7 in mid 5GHz sub-band (channels 100 - 132)																															
C	RW	HIGH																																	
				Max output power for MSC7 in high 5GHz sub-band (channels 136 - 177)																															

4.1.11 CALIB.MAXPOW5G0MCS0

Address offset: 0x144

Max output power for MCS0

Unsigned byte, resolution 0.25 dBm

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				C C C C C C C C B B B B B B B B A A A A A A A A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	LOW			Max output power for MSC0 in low 5GHz sub-band (channels 36 - 64)
B	RW	MID			Max output power for MSC0 in mid 5GHz sub-band (channels 100 - 132)
C	RW	HIGH			Max output power for MSC0 in high 5GHz sub-band (channels 136 - 177)

4.1.12 REGION_DEFAULTS

Address offset: 0x154

Customer region register usage indicator

Bit set to '0' indicate corresponding register is programmed

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ID				G F E D C B A
Reset 0xFFFFFFFF				**1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1**
ID	R/W	Field	Value ID	Value	Description
A	RW	QSPIKEY			QSPI.KEY state
B	RW	MAC0ADDRESS			MAC0.ADDRESS state
C	RW	MAC1ADDRESS			MAC1.ADDRESS state
D	RW	XO			CALIB.XO state
E	RW	MAXPOW2G4			CALIB.MAXPOW2G state
F	RW	MAXPOW5G0MCS7			CALIB.MAXPOW5G0MCS7 state
G	RW	MAXPOW5G0MCS0			CALIB.MAXPOW5G0MCS0 state

5 Recommended operating conditions

The operating conditions are the physical parameters that the chip can operate within.

Symbol	Parameter	Min.	Nom.	Max.	Units
VBAT	VDD supply voltage	2.9	3.6	4.5	V
IOVDD	VDD supply voltage for IO pins	1.62	1.8	3.6	V
OTPVDD	VDD supply voltage for OTP (read mode)	1.62	1.8	1.98	V
OTPVDD	VDD supply voltage for OTP (write mode)	2.25	2.5	2.75	V
TA	Operating temperature	-40	25	85	°C

Table 9: Recommended operating conditions

6 Absolute maximum ratings

Maximum ratings are the extreme limits to which the chip can be exposed for a limited amount of time without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the device.

	Min.	Max.	Unit
Supply voltages			
VBAT	-0.3	4.5	V
IOVDD	-0.3	3.6	V
I/O pin voltage			
$V_{I/O}$, IOVDD ≤3.3 V	-0.3	IOVDD + 0.3	V
$V_{I/O}$, IOVDD >3.3 V	-0.3	3.6	V
BUCKEN	-0.3	VBAT + 0.3	V
Environmental QFN package			
Storage temperature	-40	125	°C
Moisture Sensitivity Level (MSL)		2	
ESD Human Body Model (HBM)		750	V
ESD Charged Device Model (CDM)		1000	V

Table 10: Absolute maximum ratings

7 Electrical specification

This section provides a summary of nRF7002 electrical specifications.

VDD is 3.6 V, 25 C unless otherwise noted.

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$f_{OP,2.4GHz}$	Operating frequencies 2.4 GHz	2401		2495	MHz	
$f_{OP,5GHz}$	Operating frequencies 5 GHz	5170		5330	MHz	U-NII-1/U-NII-2A sub-bands
		5490		5730		U-NII-2C sub-band
		5735		5895		U-NII-3/U-NII-4 sub-bands
$f_{MOD,MIN}$	Minimum modulation rate		1DSSS			2.4 GHz
			MCS0			5 GHz
$f_{MOD,MAX}$	Maximum modulation rate		MCS7			
f_{TOL}	Crystal frequency tolerance at 25C[1]			20	ppm	
$f_{STA,TEMP}$	Crystal frequency stability over temperature and aging			13	ppm	
C_{L_XO}	XO load capacitance		8		pF	
ESR_{XO}	Equivalent Series Resistance			100	ohm	
$t_{SHUTDOWN→ACTIVE}$	Startup time from shutdown state		414		ms	
$t_{SLEEP→ACTIVE}$	Startup time from sleep state		6.7		ms	

Table 11: General characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$I_{TX,1DSSS,2.4GHz}$	Transmit current (2.4 GHz, 1DSSS, max output power)		252		mA	
$I_{TX,MSC0,2.4GHz}$	Transmit current (2.4 GHz, MSC0, max output power)		187		mA	
$I_{TX,MCS7,2.4GHz}$	Transmit current (2.4 GHz, MCS7, max output power)		191		mA	
$I_{TX,MCS0,5GHz}$	Transmit current (5 GHz, MCS0, max output power)		260		mA	
$I_{TX,MCS7,5GHz}$	Transmit current (5 GHz, MCS7, max output power)		260		mA	
$I_{RX,2.4GHz}$	Receive current listen (2.4 GHz)		60		mA	
$I_{RX,5GHz}$	Receive current listen (5 GHz)		56		mA	
$I_{2.4GHz,DTIM1}$	Average current consumption (2.4GHz,DTIM=1, beacon duration 3.8 ms)		3.47		mA	
$I_{2.4GHz,DTIM3}$	Average current consumption (2.4GHz,DTIM=3, beacon duration 3.8 ms)		1.12		mA	
$I_{2.4GHz,DTIM10}$	Average current consumption (2.4GHz,DTIM=10, beacon duration 3.8 ms)		0.34		mA	
$I_{5GHz,DTIM1}$	Average current consumption (5GHz,DTIM=1, beacon duration 0.7 ms)		1.70		mA	
$I_{5GHz,DTIM3}$	Average current consumption (5GHz,DTIM=3, beacon duration 0.7 ms)		0.56		mA	
$I_{5GHz,DTIM10}$	Average current consumption (5GHz,DTIM=10, beacon duration 0.7 ms)		0.19		mA	
$I_{2.4GHz,TWT,1\ min}$	Average current consumption (2.4GHz, TWT, target wake interval 1 min)[2]		29.5		uA	
$I_{2.4GHz,TWT,1\ hour}$	Average current consumption (2.4GHz, TWT, target wake interval 1 hour)[2]		18.4		uA	
$I_{2.4GHz,TWT,1\ day}$	Average current consumption (2.4GHz, TWT, target wake interval 1 day)[2]		18.2		uA	
$I_{5GHz,TWT,1\ min}$	Average current consumption (5GHz, TWT, target wake interval 1 min)[2]		28.9		uA	
$I_{5GHz,TWT,1\ hour}$	Average current consumption (5GHz, TWT, target wake interval 1 hour)[2]		18.2		uA	
$I_{5GHz,TWT,1\ day}$	Average current consumption (5GHz, TWT, target wake interval 1 day)[2]		18.0		uA	
I_{OFF}	Shutdown current		1.7		µA	
I_{SLEEP}	Sleep current (with RTC)		15		µA	

Table 12: Current consumption

[1]Tolerance before calibration. See Clock accuracy considerations chapter.

[2]Min wake duration 8.192 ms, transmit packet duration 100 µs.

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$P_{TXMAX,2.4GHz,DSSS/CCK}$	Maximum transmit power 2.4 GHz (DSSS/CCK)		21		dBm	
$P_{TXMAX,2.4GHz,MCS0}$	Maximum transmit power 2.4 GHz (6 Mbps/HT-MCS0/HE-MCS0)		16		dBm	
$P_{TXMAX,2.4GHz,MCS7}$	Maximum transmit power 2.4 GHz (54 Mbps/HT-MCS7/HE-MCS7)		16		dBm	
$P_{TXMAX,5GHz,MCS0}$	Maximum transmit power 5 GHz (6 Mbps/HT-MCS0/VHT-MCS0/HE-MCS0)		15		dBm	
$P_{TXMAX,5GHz,MCS7}$	Maximum transmit power 5 GHz (54 Mbps/HT-MCS7/VHT-MCS7/HE-MCS7)		15		dBm	

Table 13: Transmitter characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Note
$P_{SENS,2.4GHz,1DSSS}$	Sensitivity 2.4GHz (1 Mbps DSSS)		-98.6		dBm	
$P_{SENS,2.4GHz,11CCK}$	Sensitivity 2.4GHz (11 Mbps CCK)		-90.4		dBm	
$P_{SENS,2.4GHz,6MBPS}$	Sensitivity 2.4GHz (6 Mbps)		-91.6		dBm	
$P_{SENS,2.4GHz,54MBPS}$	Sensitivity 2.4GHz (54 Mbps)		-75.4		dBm	
$P_{SENS,2.4GHz,HT-MCS0}$	Sensitivity 2.4GHz (HT-MCS0)		-90.0		dBm	
$P_{SENS,2.4GHz,HT-MCS7}$	Sensitivity 2.4GHz (HT-MCS7)		-71.5		dBm	
$P_{SENS,5GHz,VHT-MCS0}$	Sensitivity 5.0GHz (VHT-MCS0)		-89.3		dBm	
$P_{SENS,5GHz,VHT-MCS7}$	Sensitivity 5.0GHz (VHT-MCS7)		-71.0		dBm	
$P_{SENS,5GHz,HE-MCS0}$	Sensitivity 5.0GHz (HE-MCS0)		-89.3		dBm	
$P_{SENS,5GHz,HE-MCS7}$	Sensitivity 5.0GHz (HE-MCS7)		-70.6		dBm	

Table 14: Receiver characteristics

8 Hardware and layout

This section describes nRF7002 hardware and layout specifications.

8.1 Pin assignments

The pin assignment figure and tables describe the pinouts for the device. There are also recommendations for how the GPIO pins should be configured, in addition to any usage restrictions.

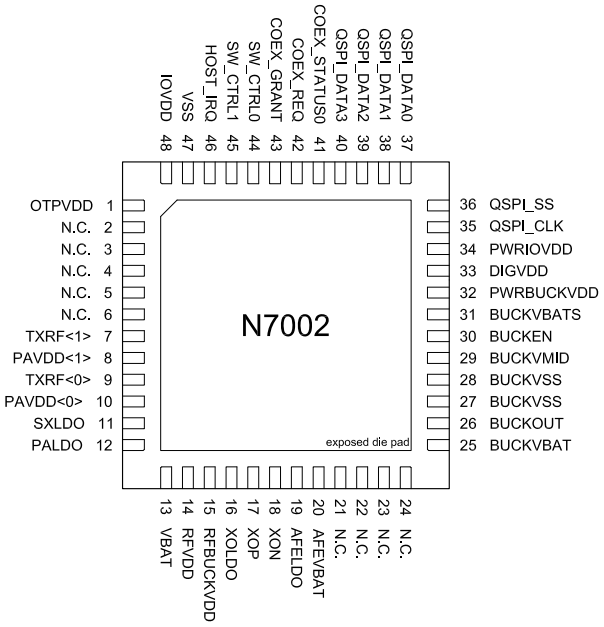


Figure 11: Pin assignments

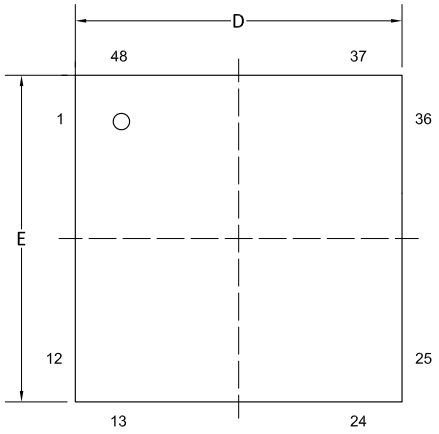
Pin	Name	Function	Description
1	OTPVDD	Power	
2	N.C.		Do not connect
3	N.C.		Do not connect
4	N.C.		Do not connect
5	N.C.		Do not connect
6	N.C.		Do not connect
7	TXRF<1>	RF	
8	PAVDD<1>	Power	
9	TXRF<0>	RF	
10	PAVDD<0>	Power	
11	SXLDO	Power	
12	PALDO	Power	
13	VBAT	Power	
14	RFVDD	Power	
15	RFBUCKVDD	Power	
16	XOLDO	Power	
17	XOP	Analog input	40MHz crystal
18	XON	Analog input	40MHz crystal
19	AFELDO	Power	
20	AFEVBAT	Power	
21	N.C.		Do not connect
22	N.C.		Do not connect
23	N.C.		Do not connect
24	N.C.		Do not connect
25	BUCKVBAT	Power	
26	BUCKOUT	Power	DCDC output
27	BUCKVSS	Power	DCDC GND
28	BUCKVSS	Power	DCDC GND
29	BUCKVMID	Power	Voltage reference decoupling pin
30	BUCKEN	Digital I/O	PWR IP enable pin
31	BUCKVBATS	Power	
32	PWRBUCKVDD	Power	
33	DIGVDD	Power	
34	PWRIOVDD	Power	

Pin	Name	Function	Description
35	QSPI_CLK	Digital I/O	QSPI Clock
36	QSPI_SS	Digital I/O	QSPI Slave select
37	QSPI_DATA0	Digital I/O	QSPI data
38	QSPI_DATA1	Digital I/O	QSPI data
39	QSPI_DATA2	Digital I/O	QSPI data
40	QSPI_DATA3	Digital I/O	QSPI data
41	COEX_STATUS0	Digital I/O	Coex interface
42	COEX_REQ	Digital I/O	Coex interface
43	COEX_GRANT	Digital I/O	Coex interface
44	SW_CTRL0	Digital I/O	External switch control
45	SW_CTRL1	Digital I/O	External switch control
46	HOST_IRQ	Digital I/O	Host processor interrupt request
47	VSS	Power	
48	IOVDD	Power	
Die pad	VSS	Power	Ground pad. Exposed die pad must be connected to ground (VSS) for proper device operation.

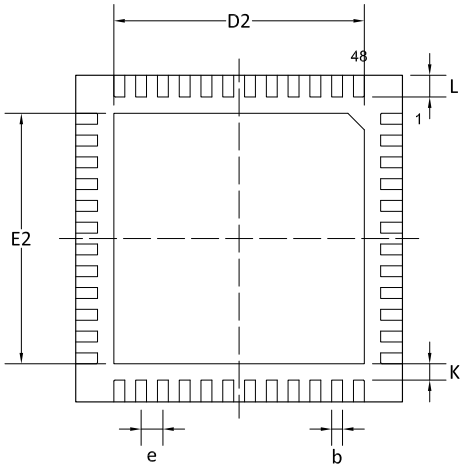
Table 15: Pin assignments

8.2 Mechanical specifications

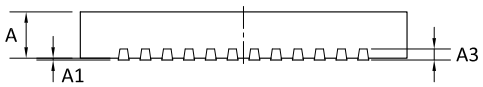
Dimensions in millimeters for the QFN 6 x 6 mm package.



TOP VIEW



BOTTOM VIEW



SIDE VIEW

	A	A1	A2	b	D	E	D2	E2	e	K	L
Min.	0.8			0.15	5.9	5.9				0.2	0.2
Nom.	0.85	0.035	0.65	0.2	6	6	4.6	4.6	0.4		
Max.	0.9	0.05		0.25	6.1	6.1					

Table 16: Package dimensions in millimeters

8.3 Reference circuitry

To ensure good RF performance when designing PCBs, it is highly recommended to use the PCB layouts and component values provided by Nordic Semiconductor.

8.3.1 Reference schematic

Circuit configuration, showing the schematic and Bill of Materials (BOM) table for nRF7002.

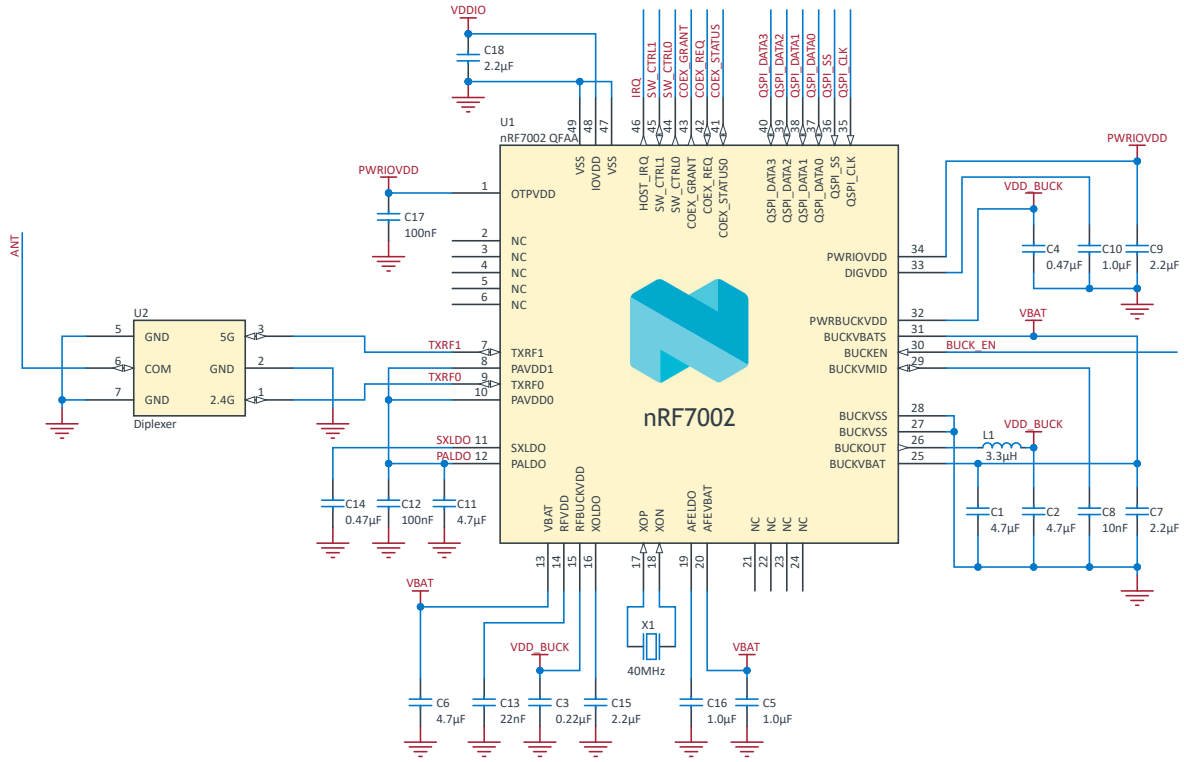


Figure 12: nRF7002 reference schematic

Designator	Value	Description	Note
U1	nRF7002	Wi-Fi 6 Dual Band companion chip	
U2	2.4 / 5 GHz	WLAN Dual Band Diplexer	
X1	40 MHz	XTAL SMD 1612, 40MHz, Cl=8pF	ESR max 100 ohm
L1	3.3µH	Inductor, 1A, ±20%, 200mOhm	
C1, C2, C6, C11	4.7µF	Capacitor, Ceramic, 4.7µF 25V X6S 0603,±10%	Place C1 close to BUCKVBAT pin Place C2 close to L1 Place C11 close to PALDO pin
C3	0.22uF	Capacitor, Ceramic, 0.22µF 10V X5R 0201, ±10%	Place C3 close to RFBUCKVDD pin
C4, C14	0.47uF	Capacitor, Ceramic, 0.47µF 6.3V X5R 0201,±10%	Place C4 close to PWRBUCKVDD pin
C5	1.0µF	Capacitor, Ceramic, 1.0µF 35V X5R 0402,±10%	
C7, C18	2.2µF	Capacitor, Ceramic, 2.2µF 16V X7S 0603,±10%	Place C7 close to BUCKVBATS pin
C8	10nF	Capacitor, Ceramic, 10nF 16V X7R 0201,±10%	
C9	2.2µF	Capacitor, Ceramic, 2.2µF 25V X5R 0201,±10%	
C10	1.0µF	Capacitor, Ceramic, 1.0µF 16V X6S 0402,±10%	
C12	100nF	Capacitor, Ceramic, 100nF 16V X7S 0201,±10%	Place C12 close to PAVDD0 pin
C13	22nF	Capacitor, Ceramic, 22nF 10V X5R 0201,±10%	
C15, C17	2.2µF	Capacitor, Ceramic, 2.2µF 10V X5R 0201,±10%	
C16	1.0µF	Capacitor, Ceramic, 1.0µF 10V X7S 0402,±10%	

Table 17: BOM for nRF7002

8.3.2 Supply sequencing requirements

The various supplies and BUCKEN need to be sequenced in order with delay requirements.

The power up sequence and requirements are:

- Supply VBAT/BUCKVBAT/BUCKVBATS/AFEVBAT
- Wait ≥ 6 ms
- Assert BUCKEN
- Wait ≥ 1 ms
- Supply IOVDD

PWRIOVDD is an internally generated supply, used for supplying OTPVDD via an external connection. It cannot be used for anything else. This supply is automatically controlled in the device.

The power down sequence and requirements are:

- De-assert BUCKEN and power down IOVDD
- Power down VBAT

There are no specific timing delay requirements as long as the sequence is correct.

8.3.3 Supply system alternatives

There are two options (high voltage and normal voltage) for connecting nRF7002 to an nRF5340 host, supporting dynamic powerup/powerdown of the nRF7002. This dynamic control utilises an external switch to control the IOVDD supply.

The following figure shows the recommended connection between nRF7002 and the host MCU (nRF5340).

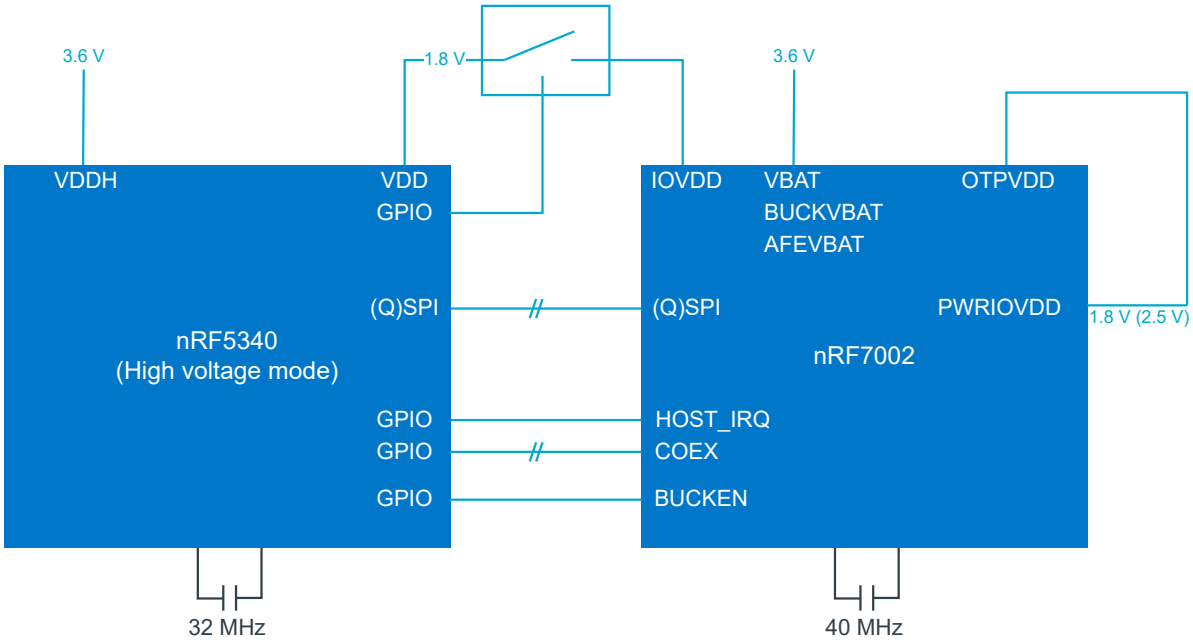


Figure 13: Supply system - high voltage mode

Both nRF5340 (used in high voltage mode) and nRF7002 can be supplied from a single 3.6 V supply.

nRF5340 can provide a 1.8 V supply used for the IO supply on nRF7002. An external switch is used to disconnect IOVDD on nRF7002 when not in use. The control of the switch is handled by the Wi-Fi driver on nRF5340.

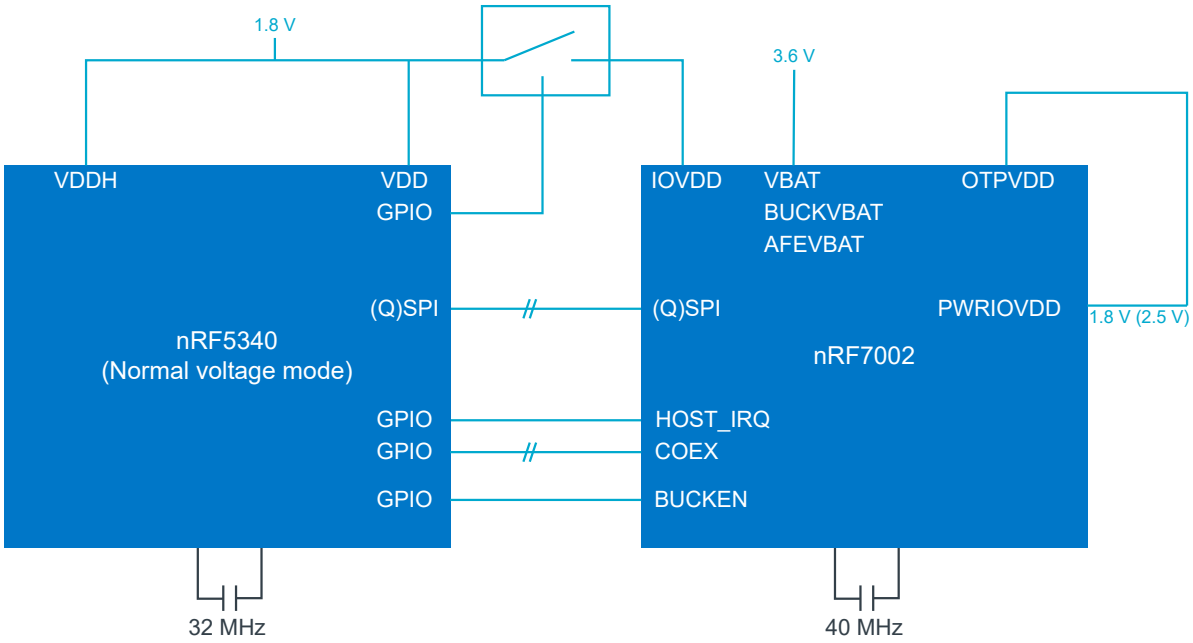


Figure 14: Supply system - normal voltage mode

8.3.4 PCB layout example

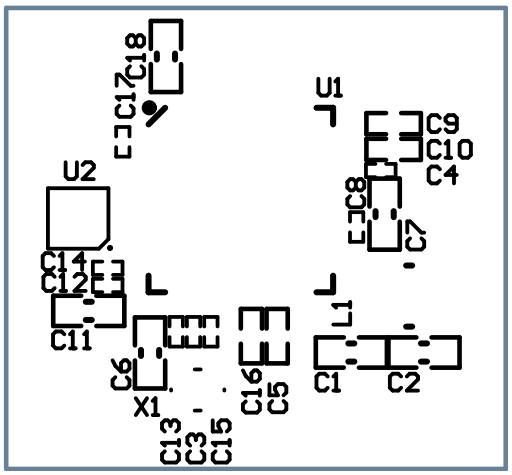


Figure 15: Top silk layer

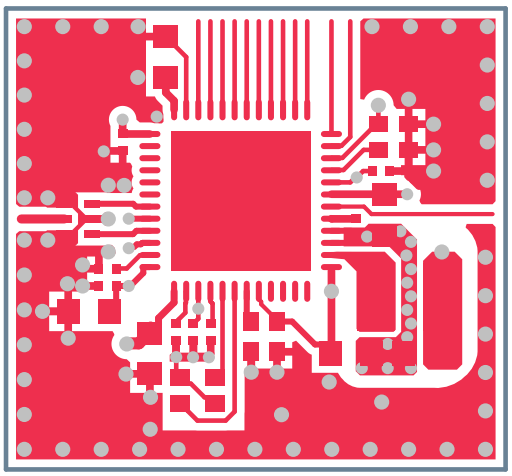


Figure 16: Top layer

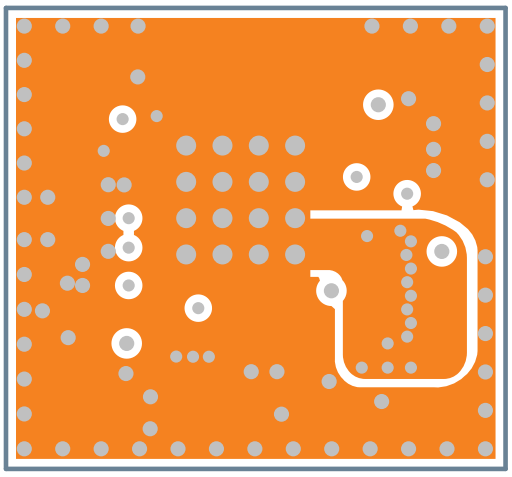


Figure 17: Mid layer 1

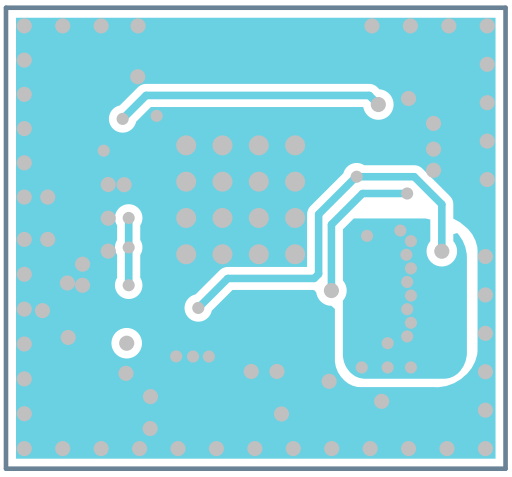


Figure 18: Mid layer 2

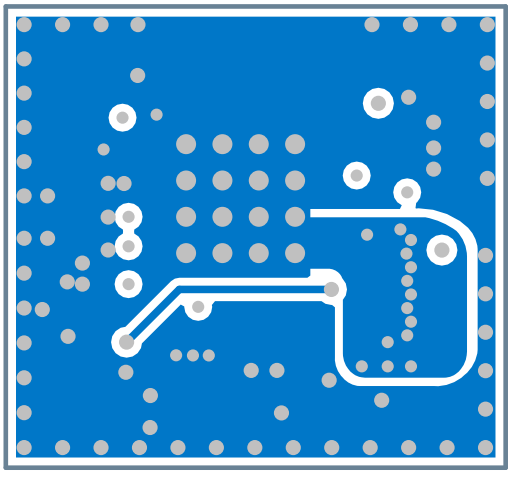


Figure 19: Bottom layer

9 Ordering information

This chapter contains information on IC marking, ordering codes, and container sizes.

9.1 Device marking

The nRF7002 package is marked as shown in the following figure.

N	7	0	0	2	
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Figure 20: IC marking

9.2 Box labels

The following figures define the box labels used for the nRF7002.

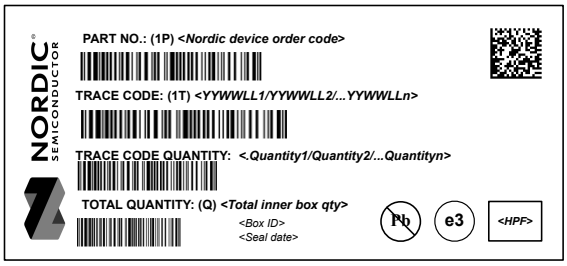


Figure 21: Inner box label

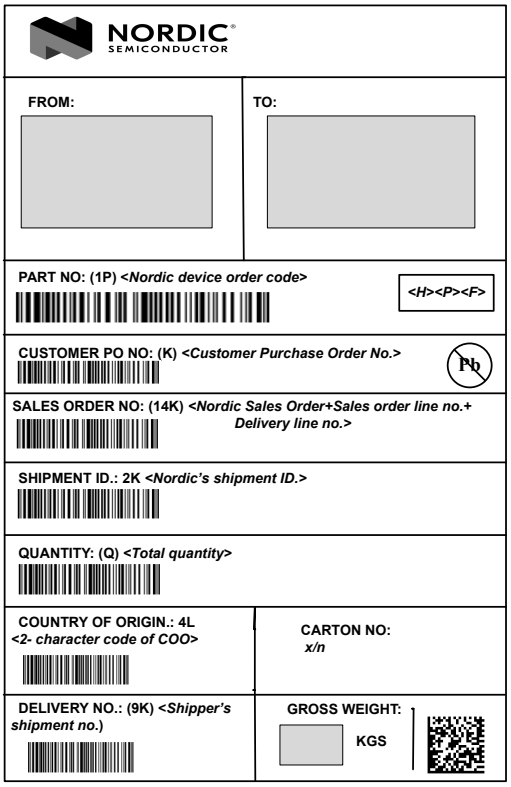


Figure 22: Outer box label

9.3 Order code

The following tables define the nRF7002 order codes and definitions.

n	R	F	7	0	0	2	-	<P	P>	<V	V>	-	<C	C>

Figure 23: Order code

Abbreviation	Definition and implemented codes
N70/nRF70	nRF70 series product
02	Part code
<PP>	Package variant code
<VV>	Function variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version code (only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 18: Abbreviations

9.4 Code ranges and values

The following tables define the nRF7002 code ranges and values.

<PP>	Package	Size (mm)	Pin/Ball count	Pitch (mm)
QF	QFN	6 x 6	48	0.4

Table 19: Package variant codes

<VV>	Variant
AA	Base functionality

Table 20: Function variant codes

<H>	Description
[A . . Z]	Hardware version/revision identifier (incremental)

Table 21: Hardware version codes

<P>	Description
[0 . . 9]	Production device identifier (incremental)
[A . . Z]	Engineering device identifier (incremental)

Table 22: Production configuration codes

<F>	Description
[A . . N, P . . Z]	Version of preprogrammed firmware
[0]	Delivered without preprogrammed firmware

Table 23: Production version codes

<YY>	Description
[16 . . 99]	Production year: 2016 to 2099

Table 24: Year codes

<WW>	Description
[1 . . 52]	Week of production

Table 25: Week codes

<LL>	Description
[AA . . ZZ]	Wafer production lot identifier

Table 26: Lot codes

<CC>	Description
R7	7" Reel
R	13" Reel

Table 27: Container codes

9.5 Product options

The following tables define the nRF7002 product options.

Order code	MOQ[1]	Comment
nRF7002-QFAA-R7	1000	Availability to be announced.
nRF7002-QFAA-R	3000	

Table 28: nRF7002 order codes

Order code	Description
nRF7002-DK	nRF7002 Development Kit

Table 29: Development tools order code

[1] Minimum Ordering Quantity

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