Lattice Embedded Vision Development Kit

User Guide

FPGA-UG-02015-1.2

February 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
CSI	Camera Serial Interface
EVDK	Embedded Vision Development Kit
GPIO	General Purpose Input/Output
HDMI	High Definition Multimedia Interface
I^2C	Inter-Integrated Circuit
MIPI	Mobile Industry Processing Interface
VIP	Video Interface Platform
USB	Universal Serial Bus

1. Introduction

This document describes the design and setup procedure for the Lattice Embedded Vision Development Kit (EVDK) to demonstrate dual CSI-2 camera to High Definition Multimedia Interface (HDMI®) bridging that features the CrossLink™, FPGA, ECP5™ FPGA and SiI1136 transmitter devices.

Figure 2.1 shows the Lattice Embedded Vision Development Kit that is designed as a stackable modular architecture with 80 mm × 80 mm form factor. The Lattice Embedded Vision Development Kit consists of three boards:

- CrossLink Video Interface Platform (VIP) Input Bridge Board
- ECP5 VIP Processor Board
- HDMI VIP Output Bridge Board

The figures shown in this document are of the Revision C version of the Embedded Vision Development Kit, for earlier versions refer to the individual evaluation board's user guide. For more information on Embedded Vision Development Kit, visit www.latticesemi.com/en/Products/DevelopmentBoardsAndKits/EmbeddedVisionDevelopmentKit.aspx

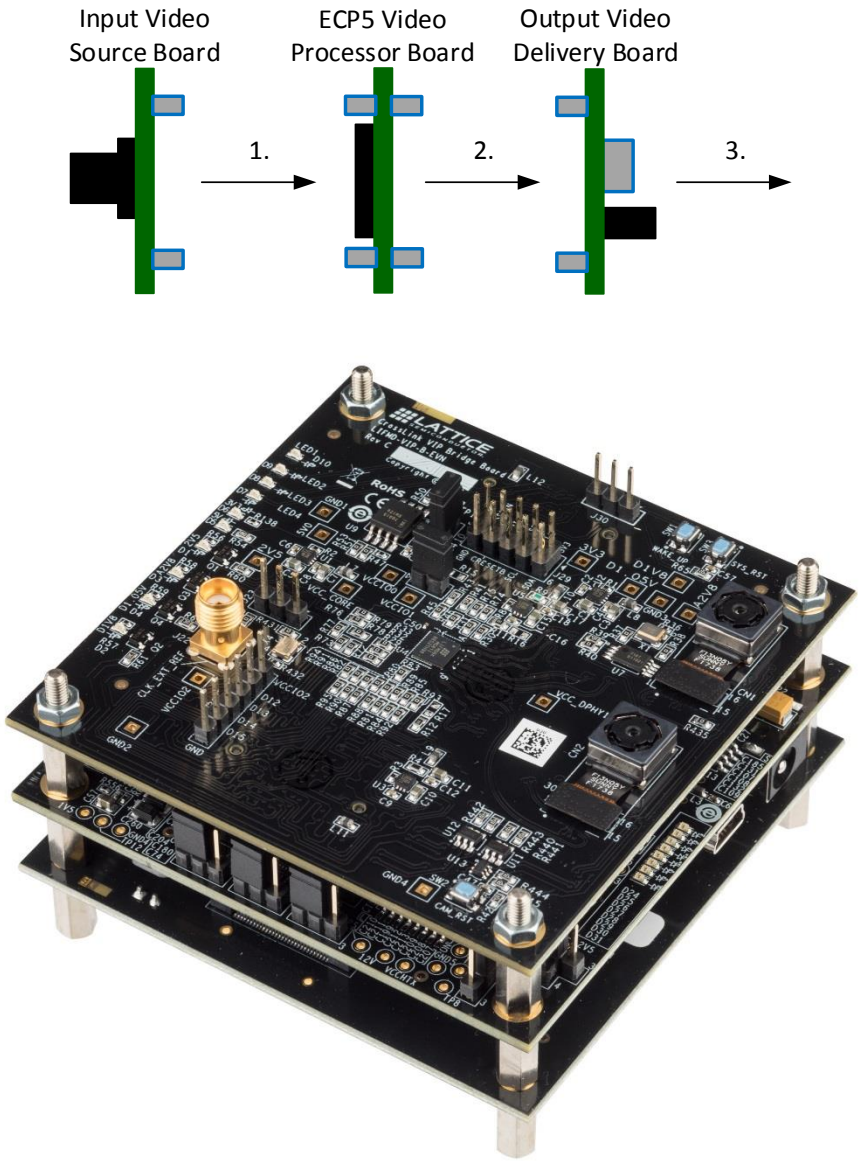


Figure 1.1. 2:1 MIPI CSI-2 to HDMI Bridge

2. Functional Description

The dual camera Mobile Industry Processing Interface (MIPI®) CSI-2 to HDMI demo uses a Sony IMX214 camera to output 1080p video over four MIPI data lanes, each running at 371.25 Mb/s. CrossLink VIP input bridge board receives the MIPI video stream from onboard camera sensor and extracts the video pixels. These video pixels from two cameras are merged side by side and the combined image data is transmitted to ECP5 in the form of parallel CMOS interface on the ECP5 video processor board through board-to-board connectors.

The ECP5 FPGA processes the merged sensor image and sends processed parallel image data to the Sil1136 HDMI transmitter on the HDMI VIP output bridge board through board to board connectors. The Sil1136 chip transmits the video data via HDMI to the 1080p display.

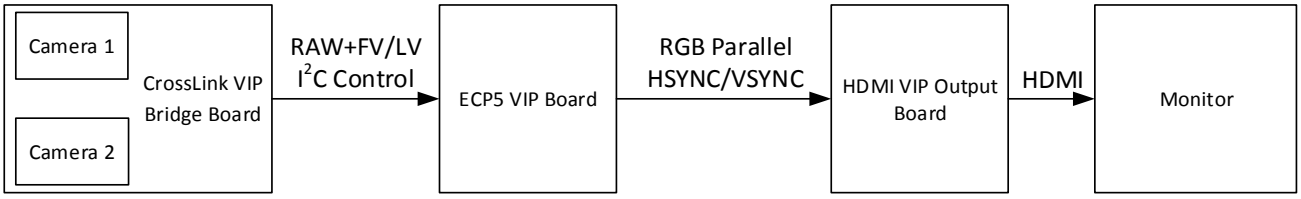


Figure 2.1. 2:1 MIPI CSI-2 to HDMI Bridge System Diagram

2.1. CrossLink

The dual-camera-to-parallel design receives the serial, source-synchronous MIPI data from two MPI CSI-2 cameras, reserializes the serial data into bytes and extracts the control signal from MIPI data packets. The byte data is sent to Byte to Pixel module which converts the byte data into RAW10 data. The two streams of RAW data are sent to the Image merger logic which combines the parallel data from both data streams and sends it to the ECP5 board. The onboard CSI-2 cameras are configured through the I2C master interface on ECP5 VIP processor board. Figure 2.2 shows the CrossLink functional block diagram.

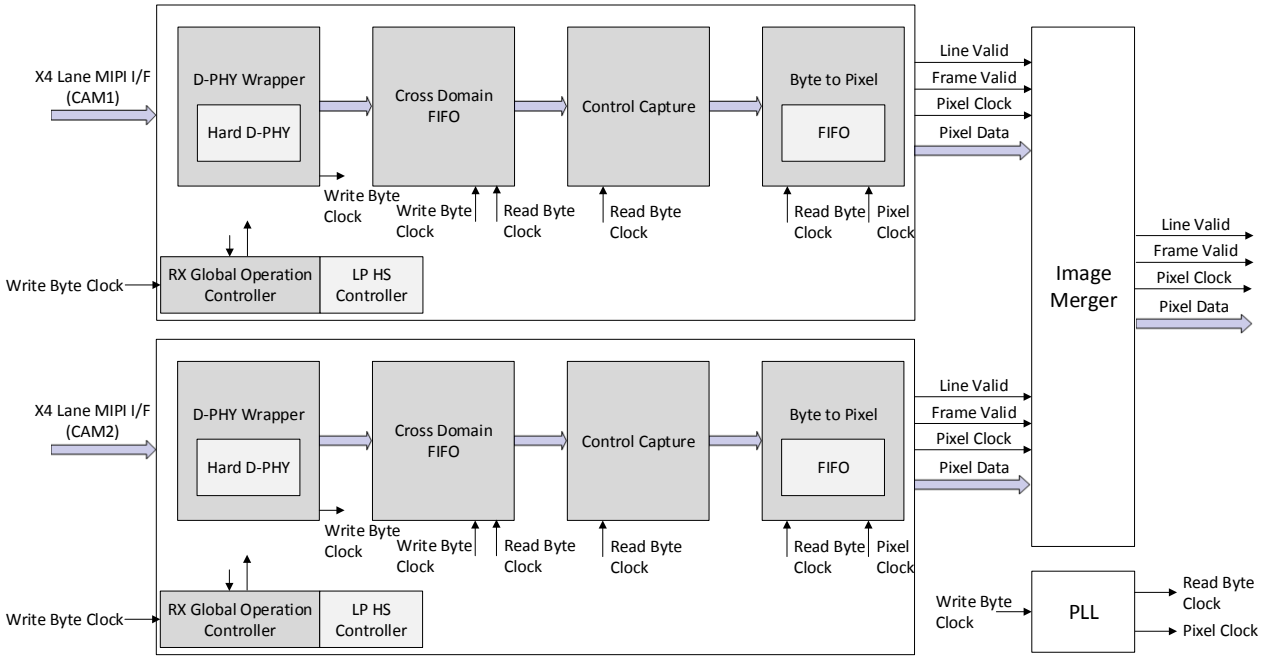


Figure 2.2. CrossLink Functional Block Diagram

2.2. ECP5

The ECP5 FPGA receives RAW10 data from CrossLink, does the fundamental image processing, and sends it to the HDMI board. Figure 2.3 shows the Lattice Programmable Image Processing Module. This module improves the quality of an image from a sensor by:

Auto Brightness – The Auto Brightness module adjusts the intensity of incoming sensor data.

Debayer – The Debayer converts the RAW10 Bayer data into separate red, green and blue pixels per clock cycle.

Color Space Converter – Colors directly from an image sensor do not match the real world by default. The Color Space Converter matrix corrects this issue. There are gain and offset controls for each color, as well as the influence of one color on the other.

Gamma Correction – Gamma Correction is a type of pre-distortion correction made to video frames to offset the non-linear behavior of display systems.

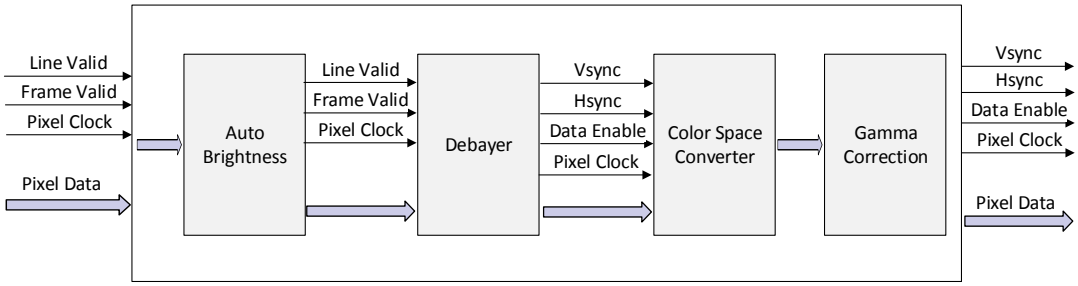


Figure 2.3. ECP5 Functional Block Diagram

2.3. Sil1136

Figure 2.4 shows the functional block diagram of the Sil1136 HDMI transmitter. This transmitter device is configured to output 1080p60 through the ECP5 I^2C Master interface on ECP5 VIP processor board. It receives 36-bit RGB data and control signals from ECP5 and converts it to HDMI format that is displayed on the HDMI monitor.

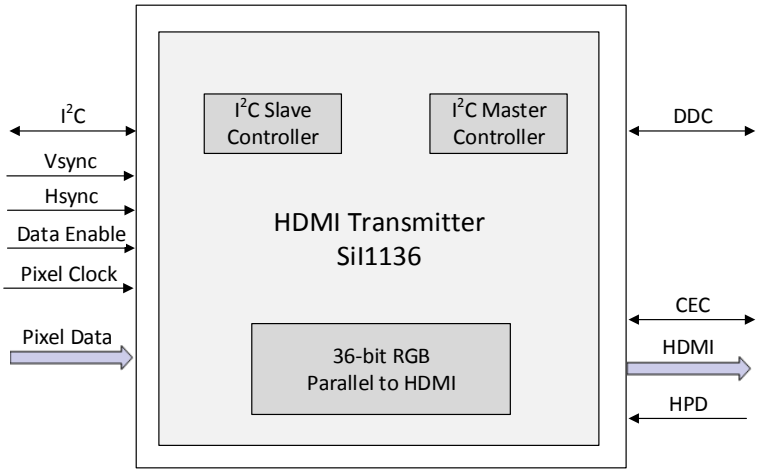


Figure 2.4. Sil1136 Functional Block Diagram

3. Demo Requirements

The following equipment is required for the demo:

- LF-EVDK1-EVN Demo Kit
- HDMI monitor
- HDMI cable
- DC power adapter (12 V)
- Laptop/PC
- Bit/JED file
- USB 2.0 Type A to Mini-B cable*
- Lattice Diamond® Programmer version 3.7 or higher*

***Note**: Required only in re-programming.

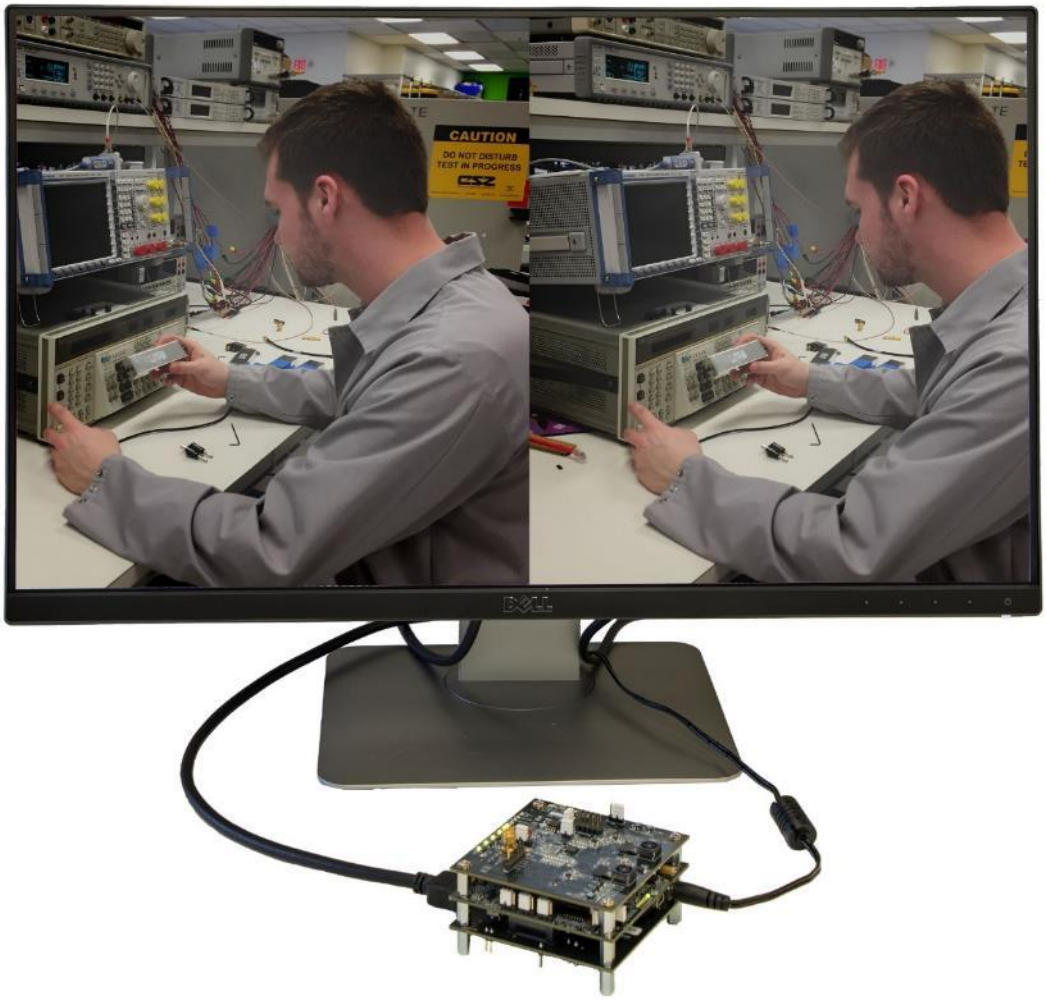
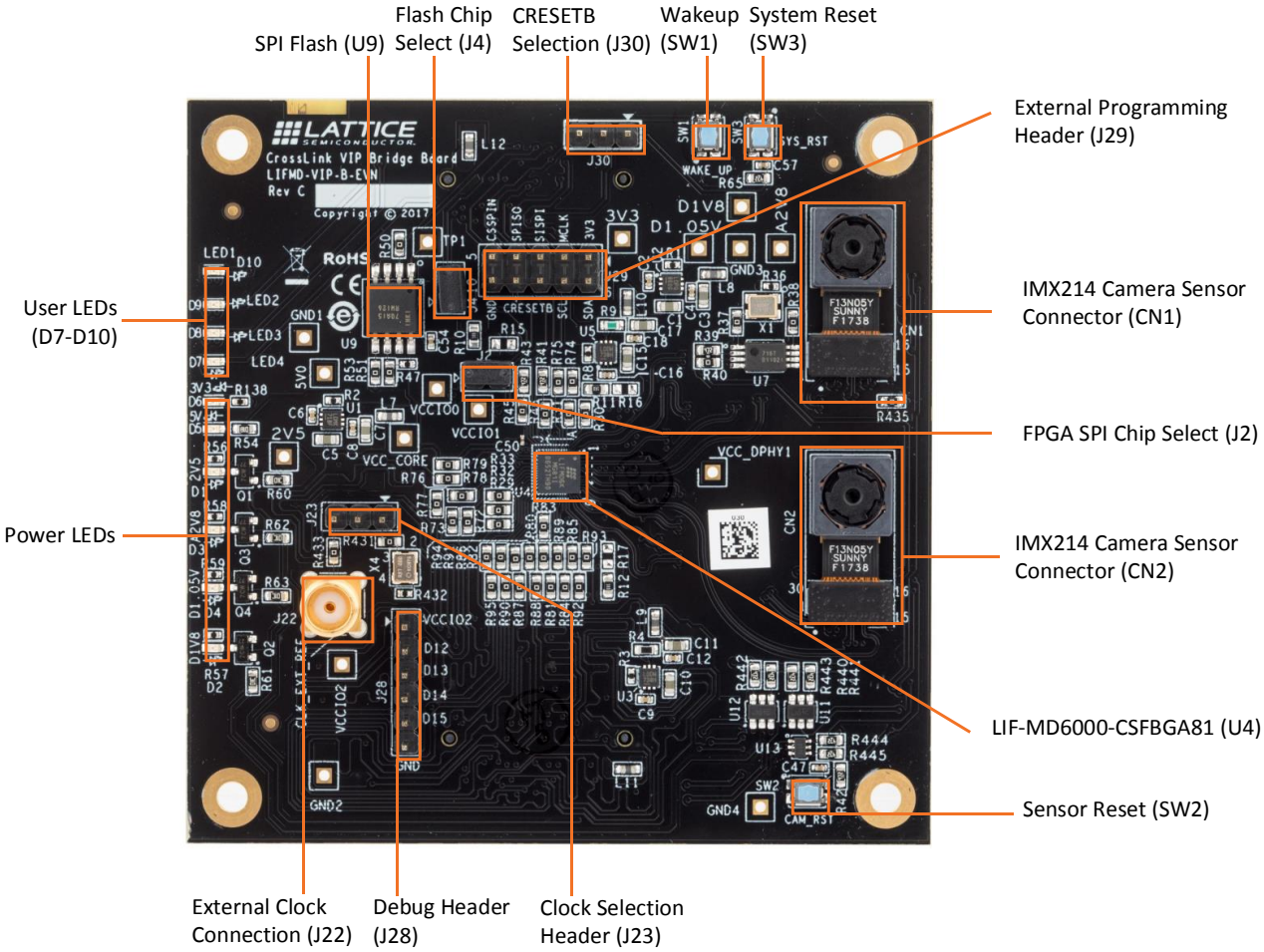


Figure 3.1. Dual Camera to HDMI Setup

3.1. CrossLink VIP Input Bridge Board



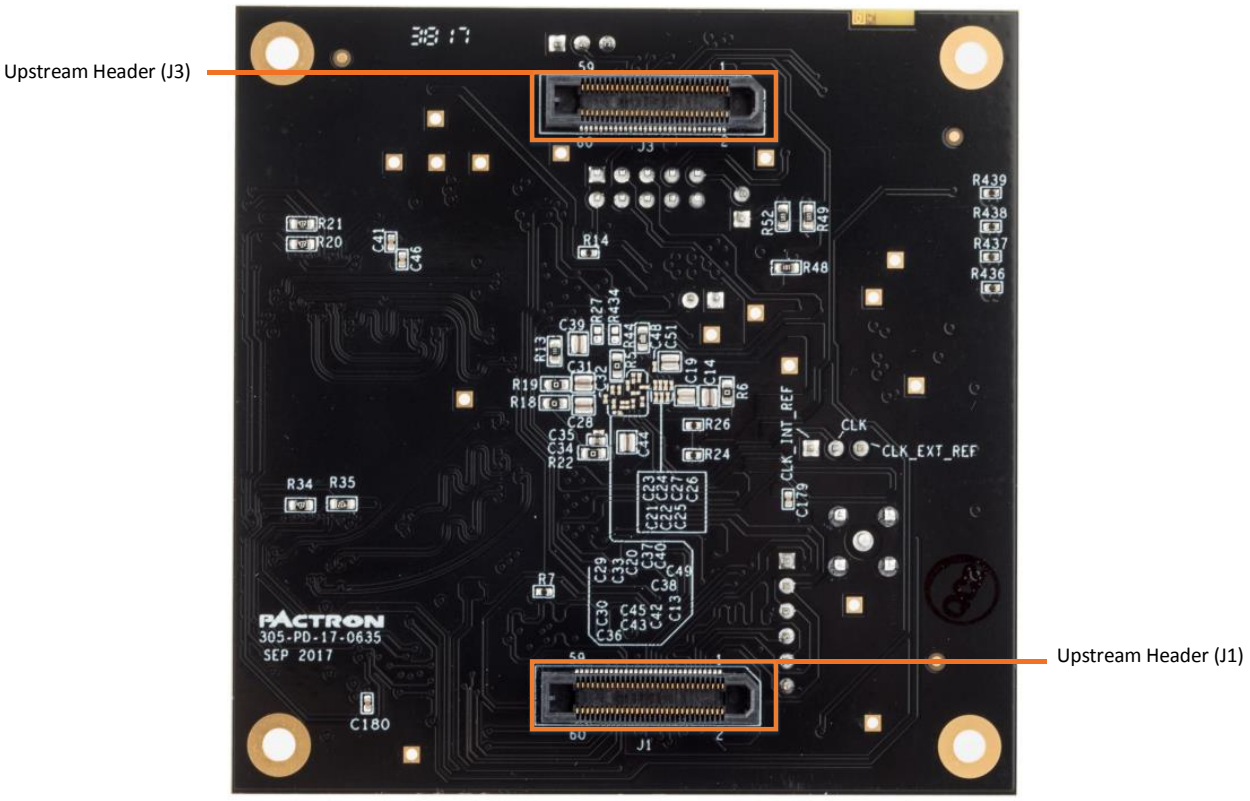
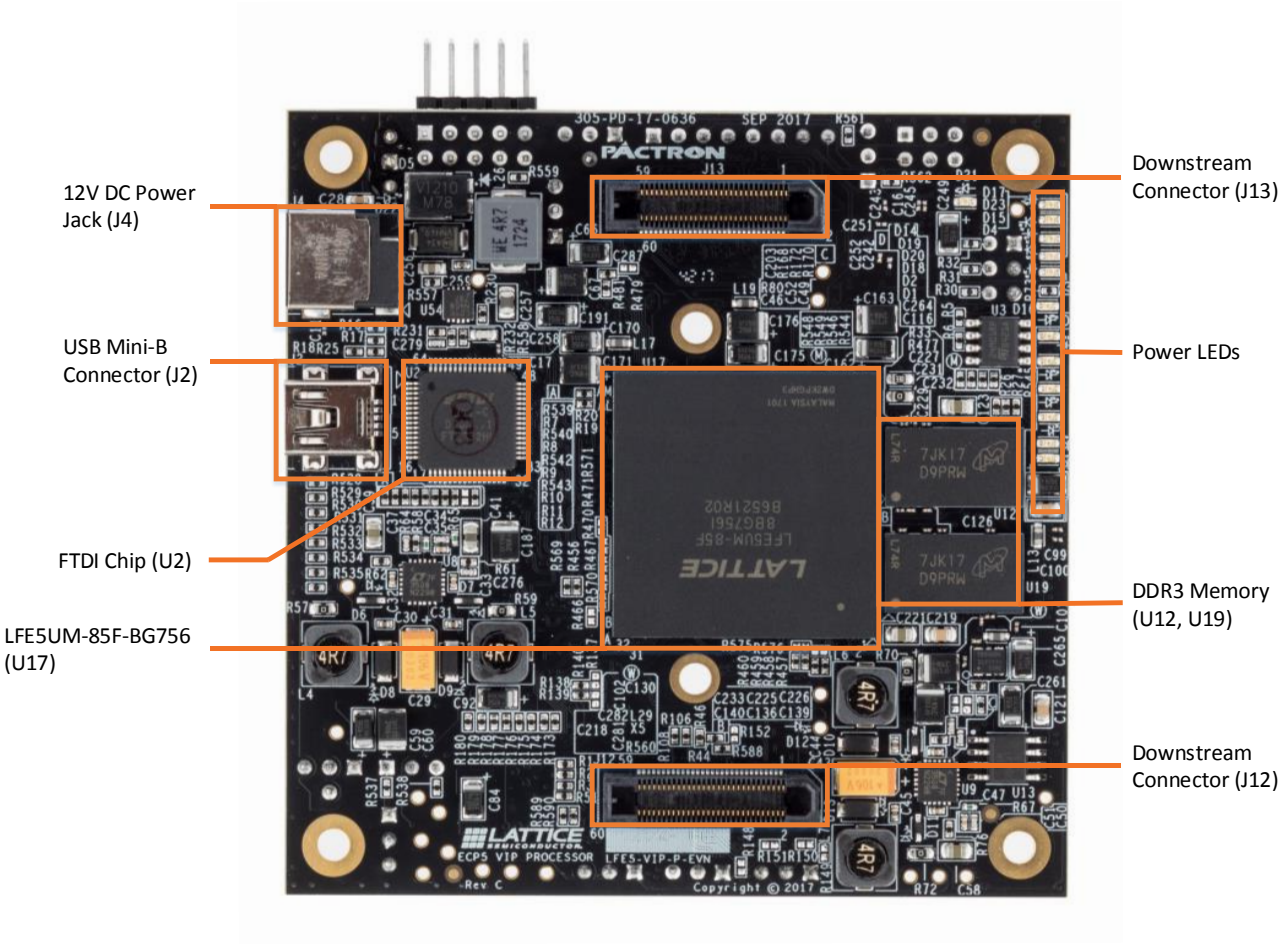


Figure 3.2.Top and Bottom View of Crosslink VIP Input Bridge Board

3.2. ECP5 VIP Processor Board



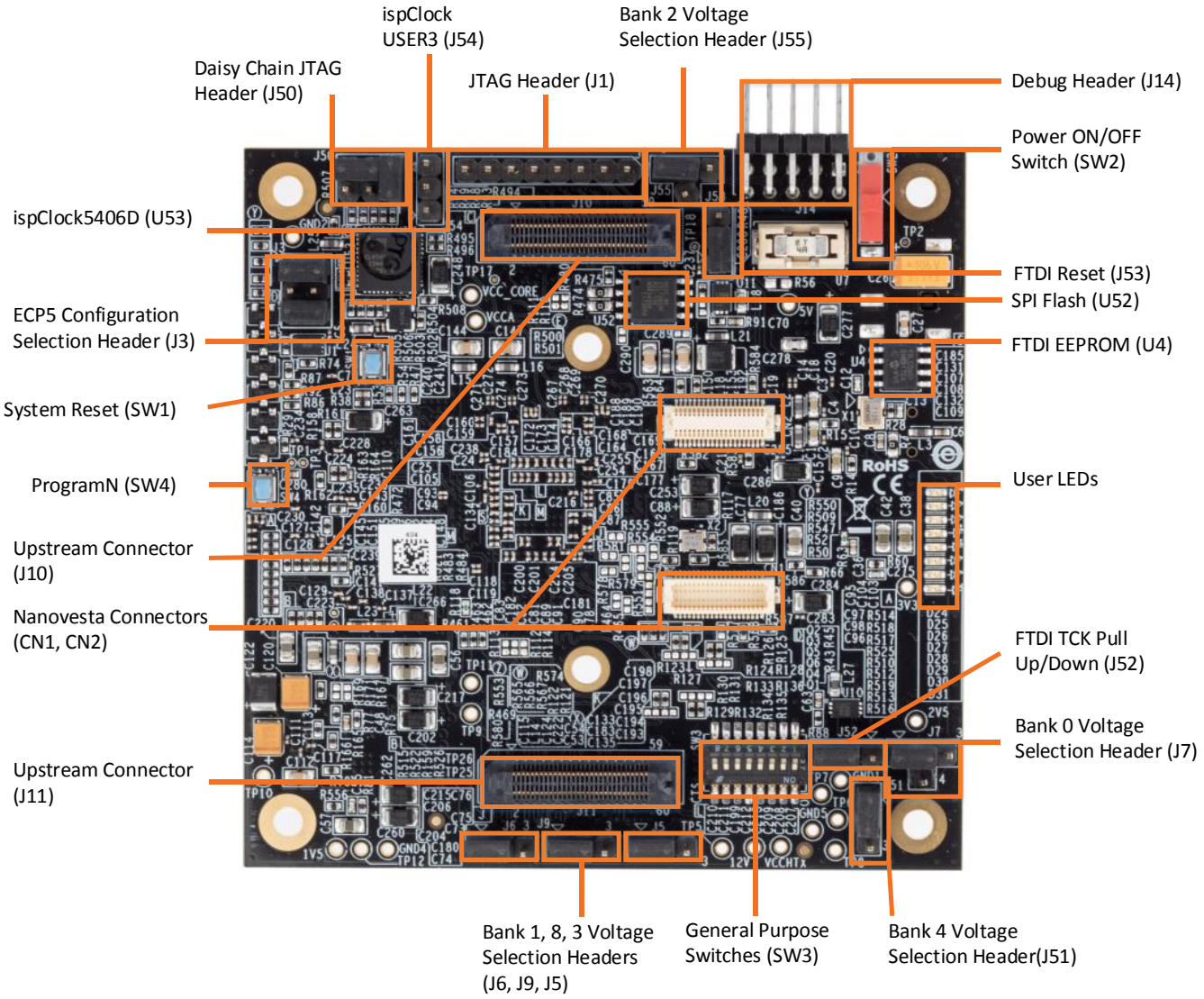
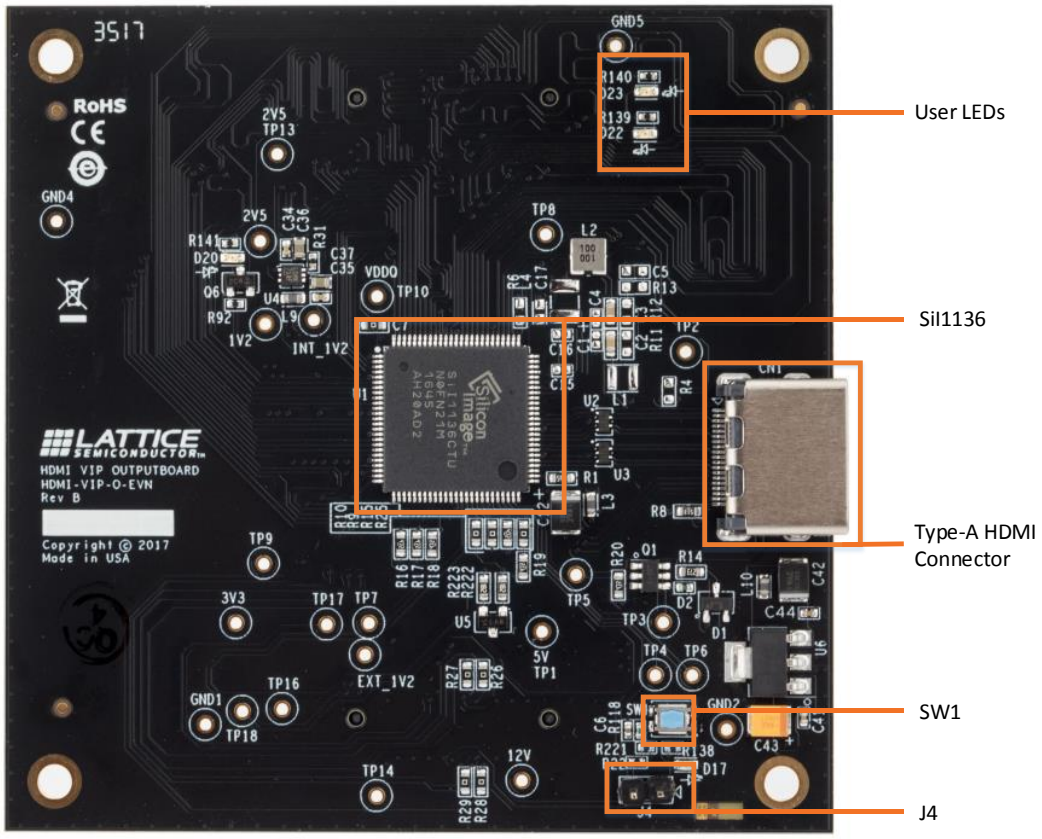


Figure 3.3. Top and Bottom View of ECP5 VIP Processor Board

3.3. HDMI VIP Output Bridge Board



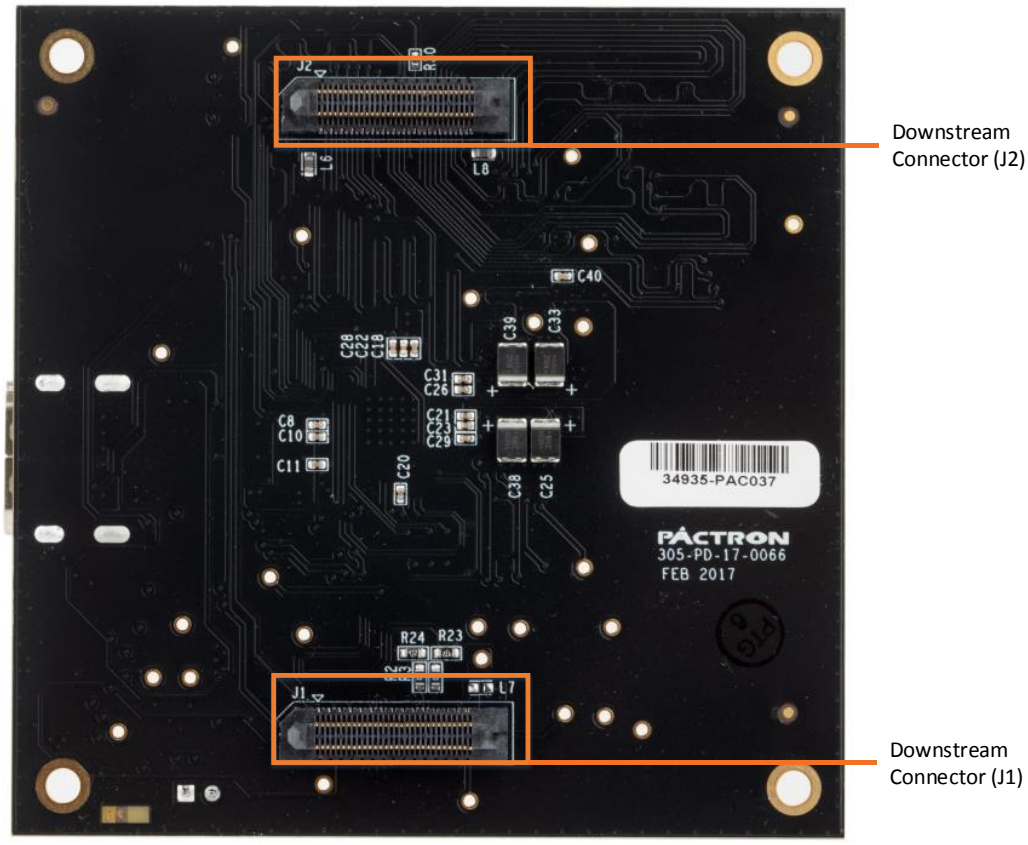


Figure 3.4. Top and Bottom View of HDMI VIP Output Board

4. Jumper Settings

Table 4.1. CrossLink VIP Input Bridge Board

Jumper	Description	Default
J2	Crosslink SPI Chip Select	Short
J4	SPI Flash Chip Select	Short
J30	CRESETB selection	Open
—	—	All other headers should be kept open.

Table 4.2. ECP5 VIP Processor Board

Jumper	Description	Default
J3	ECP5 Configuration Selection	Connect 1 and 2 and connect 5 and 6 (Master SPI)
J5	Bank 3 Voltage Selection	Connect 1 and 2 (3.3 V)
J6	Bank 1 Voltage Selection	Connect 1 and 2 (3.3 V)
J7	Bank 0 Voltage Selection	Connect 2 and 3 (3.3 V)
J9	Bank 8 Voltage Selection	Connect 1 and 2 (3.3 V)
J50	JTAG Daisy Chain	Connect 1 and 2 and connect 3 and 5 (ECP5 Only)
J51	Bank 4 Voltage Selection	Connect 1 and 2 (3.3 V)
J52	FTDI TCK Pull Up/Down	Connect 2 and 3 (JTAG)
J53	FTDI Reset	Connect 1 and 2 (Pulled High)
J55	Bank 2 Voltage	Connect 2 and 3 (3.3 V)
—	—	All other headers should be kept open.

5. Demo Procedure

To set up the demonstration:

1. Connect the ECP5 VIP processor board to the wall socket using 12 V power adapter.
2. Power up the demo kit by turning on SW2 on ECP5 VIP processor board.
3. Connect the HDMI cable from CN1 of HDMI VIP output board to the HDMI display/monitor. The monitor displays the dual camera merged image as shown in Figure 5.1.

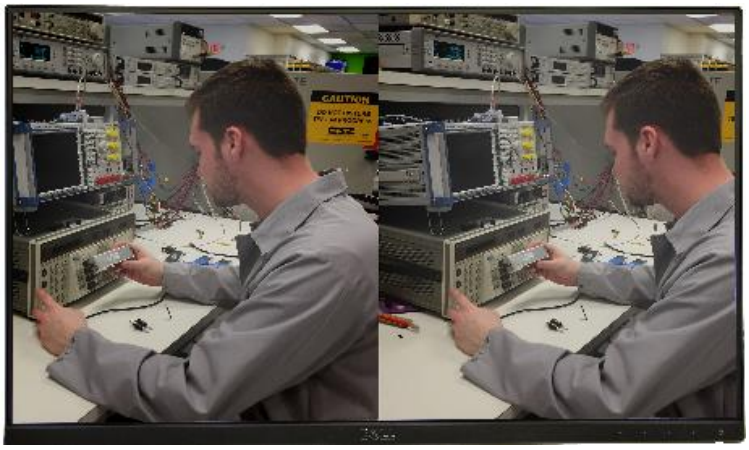


Figure 5.1. Dual Camera Merged Image

6. Demo Package Directory Structure

The key files and directories are listed below:

- Dual_CSI-2_Camera_to_HDMI_Bridge_Demo (Main directory)
  - Crosslink_DualCSI2toRaw10 (Crosslink design directory)
    - bitstream
      - DualCSI2toRaw10.bit (Crosslink bitstream)
    - source (Crosslink source files)
    - DualCSI2toRaw10.ldf (Crosslink Diamond Project File)
    - DualCSI2toRaw10.lpf (Crosslink Project Settings File)
    - DualCSI2toRaw101.sty (Crosslink Project Strategy File)
  - ECP5_Raw10toParallel (ECP5 design directory)
    - bitstream
      - Raw10toParallel.bit (ECP5 bitstream)
    - source (ECP5 source files)
    - Raw10toParallel.ldf (ECP5 Diamond Project File)
    - Raw10toParallel.lpf (ECP5 Project Settings File)
    - Raw10toParallel1.sty (ECP5 Project Strategy File)

7. Pinout Information

7.1. CrossLink

Table 7.1 lists the CrossLink pinouts used for the demo.

Table 7.1. CrossLink Pinouts

Port Name	Pin	Bank	Buffer Type	Site	Properties
reset_n_i	J4	1	LVCMOS33_IN	PB38C	Pull: Up, Clamp: On, Hysteresis: On
Camera Sensor Interface					
clk_p_i	A1	61	DPHY_BIDI	DPHY1_CKP	—
clk_n_i	A2	61	DPHY_BIDI	DPHY1_CKN	—
d0_p_i	B1	61	DPHY_BIDI	DPHY1_DP0	—
d0_n_i	B2	61	DPHY_BIDI	DPHY1_DN0	—
d1_p_i	A3	61	DPHY_BIDI	DPHY1_DP1	—
d1_n_i	B3	61	DPHY_BIDI	DPHY1_DN1	—
d2_p_i	C1	61	DPHY_BIDI	DPHY1_DP2	—
d2_n_i	C2	61	DPHY_BIDI	DPHY1_DN2	—
d3_p_i	A4	61	DPHY_BIDI	DPHY1_DP3	—
d3_n_i	B4	61	DPHY_BIDI	DPHY1_DN3	—
clk_p_i_s	A8	60	DPHY_BIDI	DPHY0_CKP	—
clk_n_i_s	A9	60	DPHY_BIDI	DPHY0_CKN	—
d0_p_i_s	B7	60	DPHY_BIDI	DPHY0_DP0	—
d0_n_i_s	A7	60	DPHY_BIDI	DPHY0_DN0	—
d1_p_i_s	B8	60	DPHY_BIDI	DPHY0_DP1	—
d1_n_i_s	B9	60	DPHY_BIDI	DPHY0_DN1	—
d2_p_i_s	B6	60	DPHY_BIDI	DPHY0_DP2	—
d2_n_i_s	A6	60	DPHY_BIDI	DPHY0_DN2	—
d3_p_i_s	C8	60	DPHY_BIDI	DPHY0_DP3	—
d3_n_i_s	C9	60	DPHY_BIDI	DPHY0_DN3	—
ECP5 Interface					
pixel_clk	J6	1	LVCMOS33_OUT	PB29C	Drive: 6 mA, Clamp: On
fv	J3	1	LVCMOS33_OUT	PB43C	Drive: 6 mA, Clamp: On
lv	H3	1	LVCMOS33_OUT	PB43D	Drive: 6 mA, Clamp: On
pixdata[0]	F9	2	LVCMOS33_OUT	PB2A	Drive: 6 mA, Clamp: On
pixdata[1]	F8	2	LVCMOS33_OUT	PB2B	Drive: 6 mA, Clamp: On
pixdata[2]	G9	2	LVCMOS33_OUT	PB2C	Drive: 6 mA, Clamp: On
pixdata[3]	G8	2	LVCMOS33_OUT	PB2D	Drive: 6 mA, Clamp: On
pixdata[4]	E9	2	LVCMOS33_OUT	PB6A	Drive: 6 mA, Clamp: On
pixdata[5]	E8	2	LVCMOS33_OUT	PB6B	Drive: 6 mA, Clamp: On
pixdata[6]	H9	2	LVCMOS33_OUT	PB6C	Drive: 6 mA, Clamp: On
pixdata[7]	H8	2	LVCMOS33_OUT	PB6D	Drive: 6 mA, Clamp: On
pixdata[8]	F7	2	LVCMOS33_OUT	PB12A	Drive: 6 mA, Clamp: On
pixdata[9]	E7	2	LVCMOS33_OUT	PB12B	Drive: 6 mA, Clamp: On

7.2. ECP5

Table 7.2 lists the ECP5 pinouts used for the demo.

Table 7.2. ECP5 Pinouts

Port Name	Pin	Bank	Buffer Type	Site	Properties
clk_i	E17	1	LVCMOS33_IN	—	—
reset_n	AH1	8	LVCMOS33_IN	PB4B	Pull: Down, Clamp: On, Hysteresis: On
q	AG30	4	LVCMOS33_OUT	PB114B	Drive:8 mA, Clamp: On, Slew: Slow
Crosslink Interface					
CSI2_sens_clk	P27	2	LVCMOS33_IN	PR44C	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_fv	K27	2	LVCMOS33_IN	PR38A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_lv	K26	2	LVCMOS33_IN	PR38B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[0]	A13	0	LVCMOS33_IN	PT42B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[1]	A8	0	LVCMOS33_IN	PT20B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[2]	F9	0	LVCMOS33_IN	PT22A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[3]	D9	0	LVCMOS33_IN	PT22B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[4]	C9	0	LVCMOS33_IN	PT24A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[5]	A9	0	LVCMOS33_IN	PT24B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[6]	C10	0	LVCMOS33_IN	PT29B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[7]	B10	0	LVCMOS33_IN	PT31A	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[8]	A10	0	LVCMOS33_IN	PT31B	Pull: Down, Clamp: On, Hysteresis: On
CSI2_sens_data[9]	E11	0	LVCMOS33_IN	PT33B	Pull: Down, Clamp: On, Hysteresis: On
reset_crosslink	D13	0	LVCMOS33_OUT	PT40B	Drive:8 mA, Clamp: On, Slew: Slow
Camera Sensor Interface					
scl	D15	0	LVCMOS33_OUT	PT51B	Drive:8 mA, Clamp: On, Slew: Slow
scl2	A14	0	LVCMOS33_OUT	PT49B	Drive:8 mA, Clamp: On, Slew: Slow
sda	F15	0	LVCMOS33_OUT	PT51A	Drive:8 mA, Clamp: On, Slew: Slow
sda2	B14	0	LVCMOS33_OUT	PT49A	Drive:8 mA, Clamp: On, Slew: Slow
reset_sensor	B4	0	LVCMOS33_OUT	PT4B	Drive:8 mA, Clamp: On, Slew: Slow
SiI1136 Interface					
HDMI_scl	AG1	8	LVCMOS33_OUT	PB4A	Drive:8 mA, Clamp: On, Slew: Slow
HDMI_sda	AJ1	8	LVCMOS33_OUT	PB6A	Drive:8 mA, Clamp: On, Slew: Slow
pixclk_out	E25	1	LVCMOS33_OUT	PT110A	Drive:8 mA, Clamp: On, Slew: Slow
data_enable	C25	1	LVCMOS33_OUT	PT107A	Drive:8 mA, Clamp: On, Slew: Slow
hsync	D25	1	LVCMOS33_OUT	PT107B	Drive:8 mA, Clamp: On, Slew: Slow
vsync	A25	1	LVCMOS33_OUT	PT105A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[0]	T31	3	LVCMOS33_OUT	PR65B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[1]	R32	3	LVCMOS33_OUT	PR65A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[2]	Y32	3	LVCMOS33_OUT	PR86B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[3]	W31	3	LVCMOS33_OUT	PR86A	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[4]	T29	3	LVCMOS33_OUT	PR53C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[5]	U28	3	LVCMOS33_OUT	PR53D	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[6]	V27	3	LVCMOS33_OUT	PR56C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[7]	V26	3	LVCMOS33_OUT	PR56D	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[8]	AC31	3	LVCMOS33_OUT	PR89C	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[9]	AB32	3	LVCMOS33_OUT	PR92A	Drive:8 mA, Clamp: On, Slew: Slow

Table 7.2. ECP5 Pinouts *(Continued)*

Port Name	Pin/Bank		Buffer Type	Site	Properties
pix_blue[10]	AC32	3	LVCMOS33_OUT	PR92B	Drive:8 mA, Clamp: On, Slew: Slow
pix_blue[11]	AD32	3	LVCMOS33_OUT	PR92C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[0]	AD26	3	LVCMOS33_OUT	PR77D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[1]	T26	3	LVCMOS33_OUT	PR47D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[2]	R26	3	LVCMOS33_OUT	PR47C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[3]	A24	1	LVCMOS33_OUT	PT101A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[4]	T32	3	LVCMOS33_OUT	PR68A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[5]	AC30	3	LVCMOS33_OUT	PR89A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[6]	AB31	3	LVCMOS33_OUT	PR89B	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[7]	V32	3	LVCMOS33_OUT	PR68C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[8]	W32	3	LVCMOS33_OUT	PR68D	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[9]	Y26	3	LVCMOS33_OUT	PR71A	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[10]	W30	3	LVCMOS33_OUT	PR65C	Drive:8 mA, Clamp: On, Slew: Slow
pix_green[11]	T30	3	LVCMOS33_OUT	PR59D	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[0]	AE27	3	LVCMOS33_OUT	PR80B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[1]	AD27	3	LVCMOS33_OUT	PR80A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[2]	AB29	3	LVCMOS33_OUT	PR83B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[3]	AB30	3	LVCMOS33_OUT	PR83A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[4]	AB28	3	LVCMOS33_OUT	PR77A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[5]	AB27	3	LVCMOS33_OUT	PR77B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[6]	AC26	3	LVCMOS33_OUT	PR77C	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[7]	Y27	3	LVCMOS33_OUT	PR71B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[8]	D24	1	LVCMOS33_OUT	PT103A	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[9]	W28	3	LVCMOS33_OUT	PR71D	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[10]	F25	1	LVCMOS33_OUT	PT110B	Drive:8 mA, Clamp: On, Slew: Slow
pix_red[11]	F17	1	LVCMOS33_OUT	PT69B	Drive:8 mA, Clamp: On, Slew: Slow

8. Ordering Information

Table 8.1. Ordering Information

Description	Ordering Part Number
Lattice Embedded Vision Development Kit	LF-EVDK1-EVN

References

For more information, refer to:

- ECP5 and ECP5-5G Family Data Sheet (FPGA-DS-02012, previously DS1044)
- CrossLink Family Data Sheet (FPGA-DS-02007)
- SiI9136-3/SiI1136 HDMI Deep Color Transmitter (SiI-DS-1084)

For schematics, refer to:

- ECP5 VIP Processor Board Evaluation Board User Guide (FPGA-EB-02001)
- CrossLink VIP Input Bridge Board Evaluation Board User Guide (FPGA-EB-02002)
- HDMI VIP Output Bridge Board Evaluation Board User Guide (FPGA-EB-02003)

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Appendix A. Lattice Embedded Vision Development Kit Setup

To set up the display demo boards:

1. Connect the J3 and J1 connectors of CrossLink VIP input bridge board to the J10 and J11 connectors of the ECP5 VIP board.
2. Connect the J13 and J12 connectors of ECP5 VIP board to the J2 and J1 connectors of the HDMI VIP output board.
3. Connect one end of the HDMI cable to the C1 connector of the HDMI VIP output board and the other end to the monitor.
4. Connect the 12 V wall power adapter cable to the J4 connector of the ECP5 VIP board.
5. The Dual CSI-2 camera to HDMI Bridge design should be programmed into the SPI Flash on the EVDK, this loads the reference design on power up. Refer to Appendix B. Programming the Lattice Embedded Vision Development Kit, to update or change the FPGA or SPI Flash images.

Appendix B. Programming the Lattice Embedded Vision Development Kit

Using Diamond Programmer with the EVDK

The EVDK has a built in download controller for programming. It uses an FT2232H Future Technology Devices International (FTDI) part to convert USB to JTAG. To use the built-in download controller, connect the USB cable from J2 of the ECP5 VIP Processor Board to your PC (with Diamond programming software installed). A mini USB to USB-A cable is included in the EVDK. The USB hub on the PC detects the cable of the USB function on Port 0, making the built-in download controller available for use with the Diamond programming software.

In order to provide a single programming interface for the EVDK, the ECP5 VIP Processor Board's JTAG interface is shared with the Crosslink VIP Input Bridge Board's SPI programming interface. During a JTAG scan, the Diamond Programmer will only see one of the devices:

- LFE5UM-85F, if the Crosslink device is currently programmed
- LIF-MD6000, if the Crosslink device is not programmed

A JTAG scan also erases both ECP5 and Crosslink SRAM images, requiring you to reprogram both devices. When using the Diamond Programmer, selecting **Create a new blank project** and manually selecting the device family and device prevents the erasure of both devices.

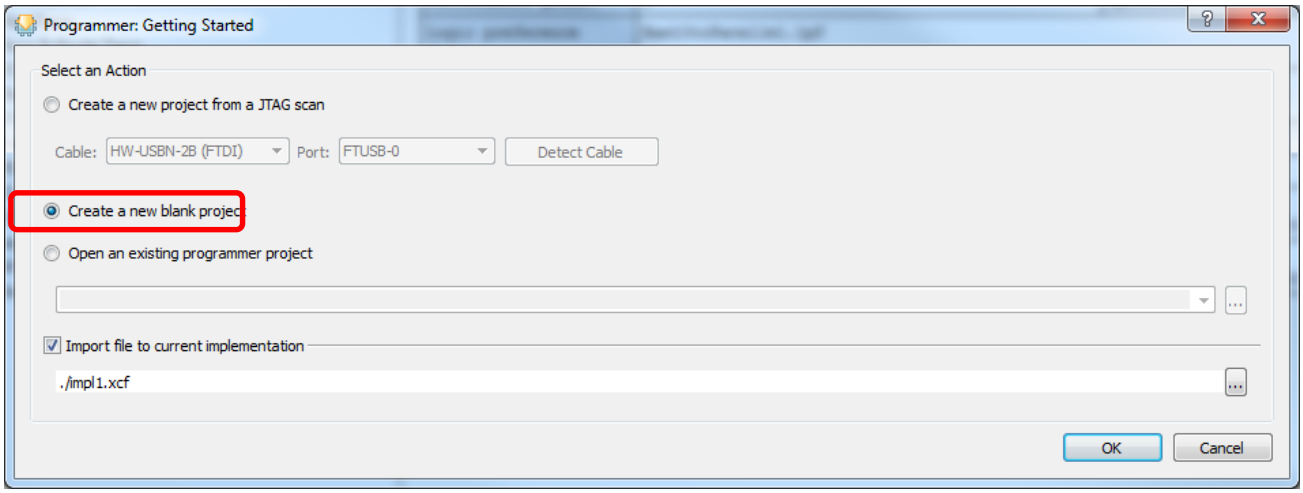


Figure B.1. Create a New Blank Project

ECP5 SPI Flash Programming

Erasing the ECP5 Prior to Reprogramming

If the ECP5 is already programmed (either directly, or loaded from SPI Flash), erase first the ECP5 SRAM memory, then program the ECP5's SPI Flash in the next section. Keep the board powered when re-programming the SPI Flash in the next section.

To erase the ECP5:

1. Launch Diamond Programmer with **Create a new blank project**.
2. Select **ECP5UM** for **Device Family** and **LFE5UM-85F** for **Device**.

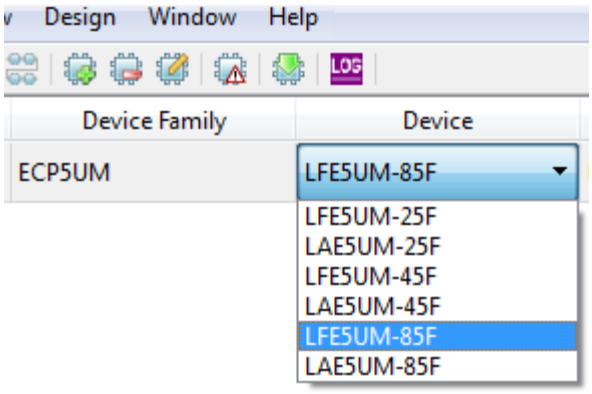


Figure B.2. Selecting Device

3. Right-click and select **Device Properties**.
4. Select **JTAG 1532 Mode** for **Access Mode** and **Erase Only** for **Operation**.

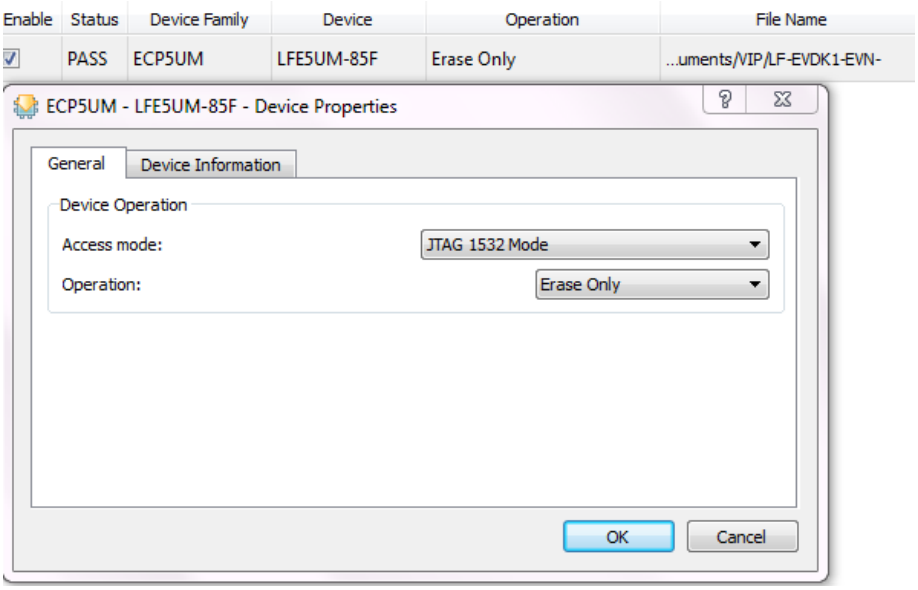


Figure B.3. Device Operation

5. Click **OK** to close the Device Properties window.
6. Click the **Program** button in Diamond Programmer to start the Erase sequence.

Programming the SPI on the ECP5 VIP Processor Board

To program the SPI:

1. Ensure the ECP5 device is erased by performing Steps 1-6.
2. Right-click and select **Device Properties**.
3. Select **SPI Flash Background Programming** for **Access mode** and make the following selections:
   a. For **Programming File**, browse and select the ECP5 bitfile (*.bit)
   b. For **SPI Flash Options**, refer to the table below.

Table B.1. SPI Flash Options Selection Guide

Item	Rev A/B	Rev C
Family	SPI Serial Flash	SPI Serial Flash
Vendor	Micron	Macronix
Device	SPI-N25Q128A	MX25L12805

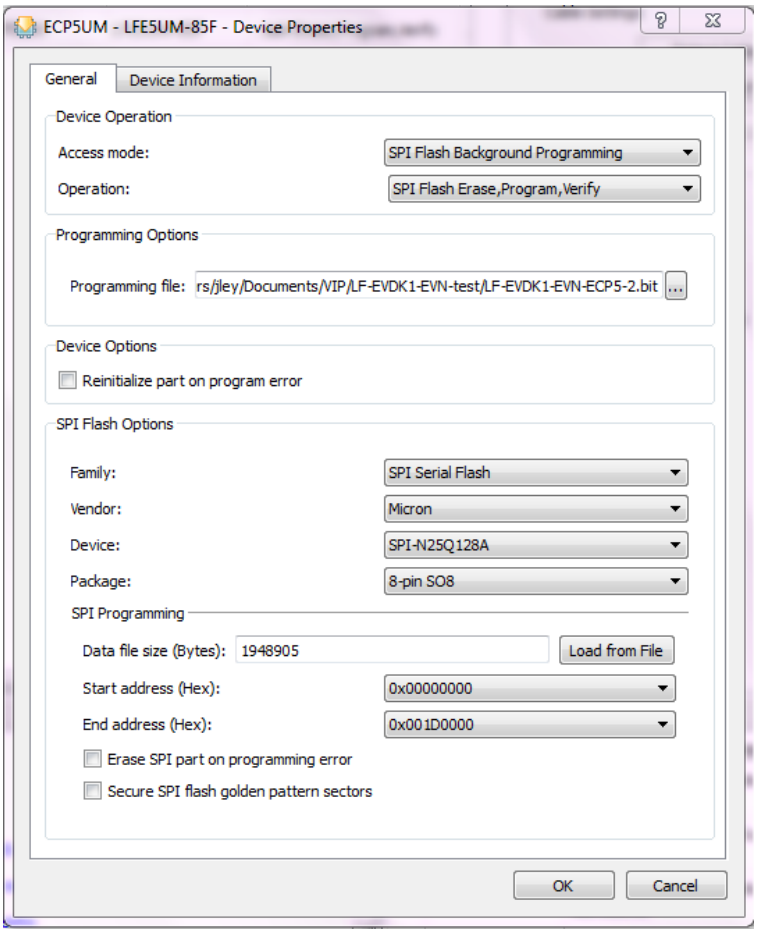


Figure B.4. Device Properties

4. Click **OK** to close the Device Properties window.
5. Click the **Program** button  in Diamond Programmer to start the programming sequence.
6. After successful programming, the Output console displays the results as shown in Figure B.5

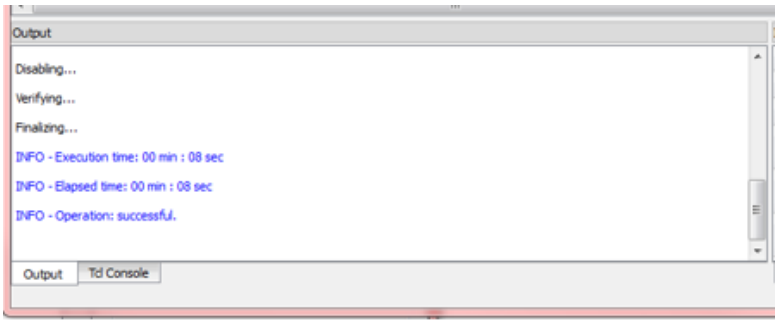


Figure B.5. Output Console

Crosslink SPI Flash Programming

Erasing the CrossLink FPGA Prior to Reprogramming

If the CrossLink is already programmed (either directly, or loaded from SPI Flash), you'll need to follow this procedure to first erase the CrossLink SRAM memory before re-programming the CrossLink's SPI Flash. If you are doing this, you need to keep the board powered when re-programming the SPI Flash (so it doesn't re-load on re-boot).

To erase CrossLink:

1. Launch Diamond Programmer with **Create a new blank project**.
2. Select **LIFMD** for **Device Family** and **LIF-MD6000** for **Device**.

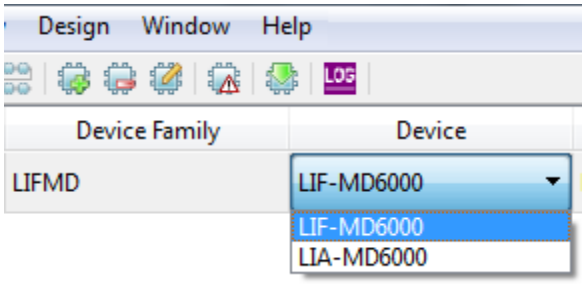


Figure B.6. Select Device

3. Right-click and select **Device Properties**.
4. Select SSPI SRAM Programming for Access Mode and Erase Only for Operation.

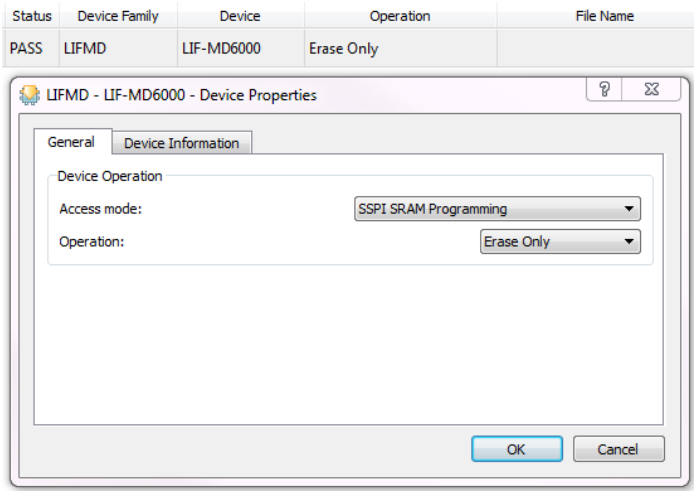


Figure B.7. Device Operation

5. Click **OK** to close the Device Properties window
6. Click the **Program** button  in Diamond Programmer to start the Erase sequence.

Programming the SPI on the CrossLink VIP Input Bridge Board

To program the SPI:

1. Ensure the Crosslink device is erased by performing Steps 1-6.
2. Right-Click and select Device Properties.
3. Select SPI Flash Programming for Access mode and make the following selections:
   a. For “Programming File”, browse and select the Crosslink bitfile (*.bit)
   b. For **SPI Flash Options**, refer to the table below.

Table B.2. SPI Flash Options Selection Guide

Item	Rev A/B	Rev C
Family	SPI Serial Flash	SPI Serial Flash Beta
Vendor	Micron	Micron
Device	SPI-M25PX16	SPI-MT25QL128A

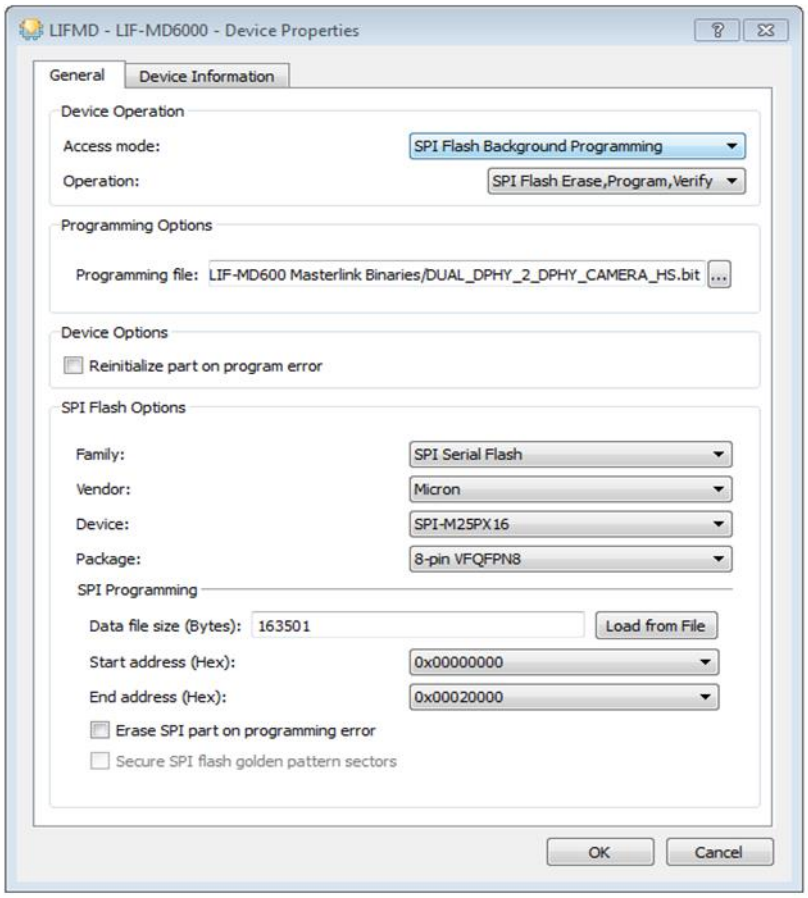


Figure B.8. Device Properties

4. Click **OK** to close the Device Properties window.
5. Click the **Program** button in Diamond Programmer to start the programming sequence.
6. After successful programming, the Output console displays the results as shown in Figure B.5

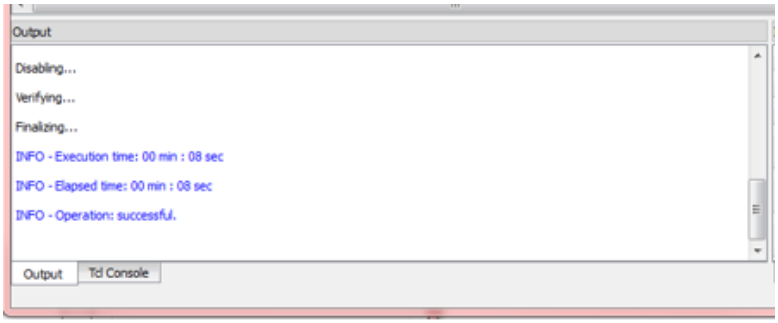


Figure B.9. Output Console

Revision History

Date	Version	Change Summary
February 2018	1.2	• Updated figures for Rev C board. • Updated ECP5 section for ECP5 Design. • Updated Demo Package Directory Structure. • Added Appendix B. Programming the Lattice Embedded Vision Development Kit.
January 2018	1.1	• Changed pASSP to FPGA in the Introduction Section and the Lattice Embedded Vision Development Kit section. • Updated Lattice Semiconductor Logo on the cover pages, headers, and footers of this document.
April 2017	1.0	Initial release.

7th Floor, 111 SW 5th Avenue
Portland, OR 97204, USA
T 503.268.8000
www.latticesemi.com